

Overview

The IObundle SPI Flash Controller core is a configurable spi master interface core for communication with flash memories. It supports automatic controller configuration, Execute-in-Place (XiP) mode, simple and multi-line dual/quad communication protocols and STR (Single Transfer Rates)/DTR (Double Transfer Rates) modes. The IP is currently supported for use in ASICs and FPGAs.

Features

- Iob Native interface support
- Configurable spi data lanes: 1, 2 (dual) or 4 (quad) lane modes
- Supports eXecute-In-Place (XiP) mode for low latency memory reads, requiring only memory address. Allows for code execution directly on flash access
- Supports STR (Single Data Rate) and DTR (Double Data Rate) for increased throughput in low frequency systems
- Flexible configurable frame format

Benefits

- Easy hardware and software integration
- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption

Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code
- Software driver and example user software
- User documentation for easy system integration
- Example integration in IOB-SoC (optional)

Block Diagram

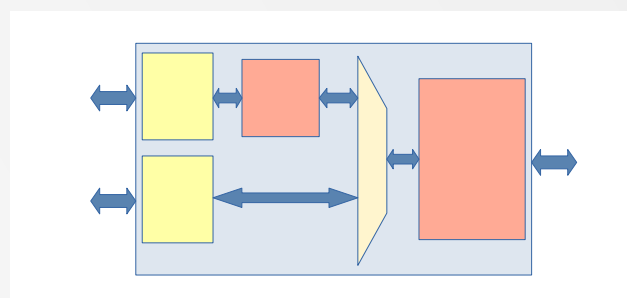


Figure 1: High-level block diagram

FPGA Results

The following are FPGA implementation results for Xilinx FPGA device on the Kintex Ultrascale board and for the Intel FPGA device on the Cyclone V GT FPGA board.

Resource	Used	Resource	Used
LUTs	575	ALM	375
Registers	519	FF	561
DSPs	0	DSP	0
BRAM	0	BRAM blocks	0
		BRAM bits	

Table 1: Kintex Ultrascale (left) and Cyclone V GT (right)

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.