IObundle IOb SPI Flash Controller User Guide

User Guide

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1 Introduction

The IObundle SPI Flash Controller core is a configurable spi master interface core for communication with flash memories. It supports automatic controller configuration, Execute-in-Place (XiP) mode, simple and multi-line dual/quad communication protocols and STR (Single Transfer Rates)/DTR (Double Transfer Rates) modes. The IP is currently supported for use in ASICs and FPGAs.

2 Symbol

Figure 1: IP Core Symbol

3 Features

- Iob Native interface support
- Configurable spi data lanes: 1, 2 (dual) or 4 (quad) lane modes
- Supports eXecute-In-Place (XIP) mode for low latency memory reads, requiring only memory address. Allows for code execution directly on flash access
- Supports STR (Single Data Rate) and DTR (Double Data Rate) for increased throughput in low frequency systems
- Flexible configurable frame format

4 Benefits

- Easy hardware and software integration
- Compact hardware implementation

- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption

5 Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code
- Software driver and example user software
- User documentation for easy system integration
- Example integration in IOb-SoC (optional)

Block Diagram

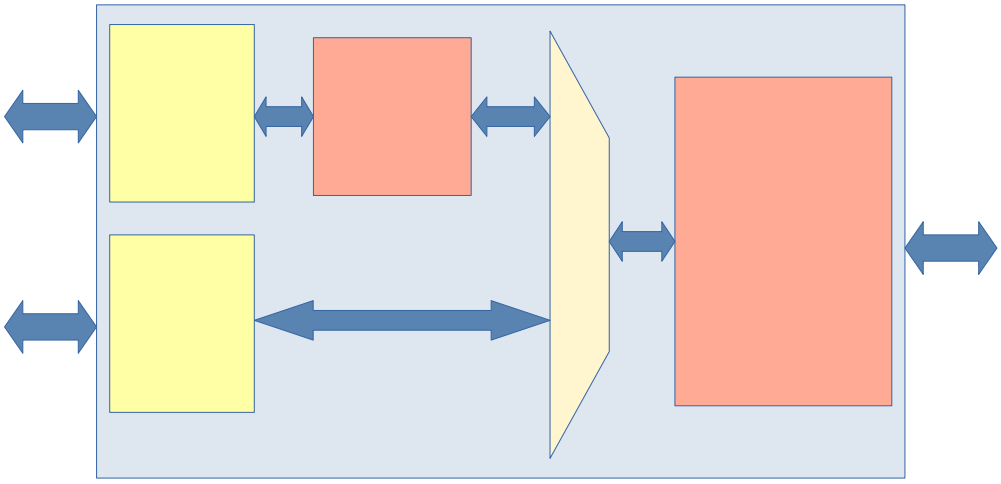

Figure 2: High-level block diagram

6 Interface Signals

Signal	Direction	Description
clk	Input	system clock signal
rst	Input	system reset signal
valid	Input	1-bit
address	Input	4-bit select SW Register
wdata	Input	32-bit data to write to SW Register
wstrb	Input	4-bit byte to write
rdata	Output	32-bit data to read
ready	Output	1-bit idle state
valid_cache	Input	1-bit instructions i/f
address_cache	Input	24-bit instructions i/f flash address
wdata_cache	Input	32-bit instructions i/f UNUSED
wstrb_cache	Input	4-bit intructions i/f byte to write
rdata_cache	Output	2-bit intructions i/f data read
ready_cache	Output	1-bit instructions i/f
SS	Output	SPI i/f
SCLK	Output	SPI i/f serial clock
MOSI	Bidir	SPI i/f DQ0
MISO	Bidir	SPI i/f DQ1
WP_N	Bidir	SPI i/f DQ2
HOLD_N	Bidir	SPI i/f DQ3

Table 1: General interface signals

7 Timing Diagrams

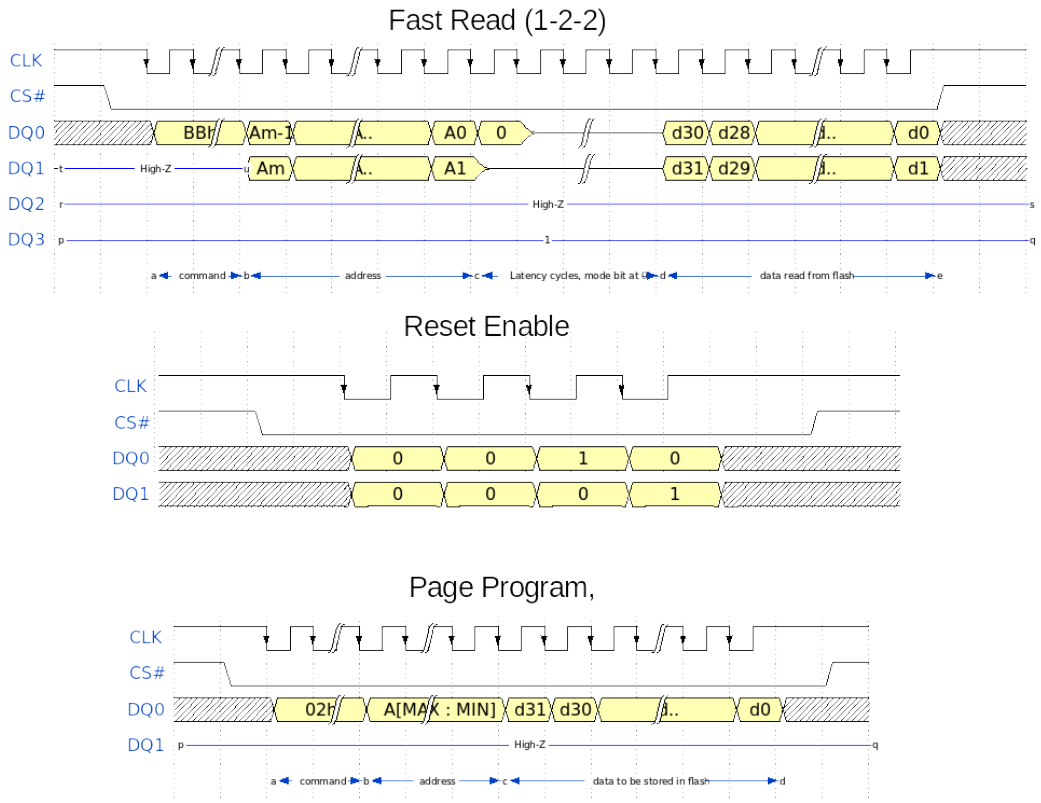

Figure 3: SPI slave interface timing diagram

8 Software Components

A set of SW accessible Registers interacting basic functions (platform functions) are provided. Higher level functions can be built on top of the platform functions, with several already provided which implement support for select flash commands.

FPGA Resources

The following are FPGA implementation results for Xilinx FPGA device on the Kintex Ultrascale board.

Resource	Used
LUTs	558
Registers	518
DSPs	0

Table 2: FPGA results for Kintex Ultrascale