Overview

The IObundle xSPI Flash Controller core is a configurable spi/xspi master interface core for communication with flash memories. It supports automatic controller configuration, Execute-in-Place (XiP) mode, simple and multi-line dual/quad communication protocols and STR (Single Transfer Rates)/DDR (Double Data Rates) modes. The IP is currently supported for use in ASICs and FPGAs.

Features

- f1
- f2

Benefits

- Easy hardware and software integration
- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption

Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code
- Software driver and example user software
- User documentation for easy system integration
- Example integration in IOb-SoC (optional)

Block Diagram

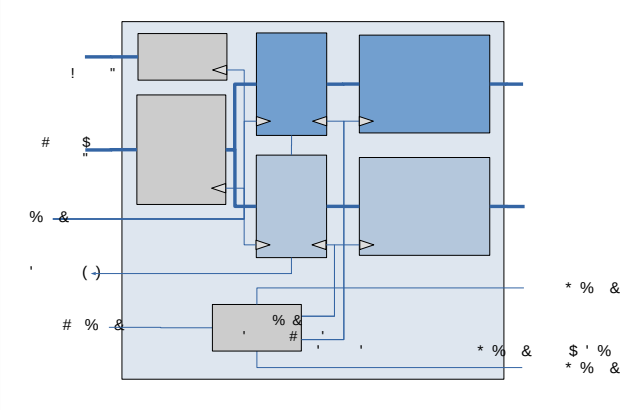

Figure 1: High-level block diagram

FPGA Results

The following are FPGA implementation results for two FPGA device families. BRAM usage results depend on the configured size of the RX and TX FIFOs, as well as the number of TX/RX pins, and the number of bits for the DMA. The below results use the as configurations 10 address bits for both FIFOs, 10 pins for TX and RX, and 32 bits for the DMA.

Resource	Used
LUTs	223
Registers	344
DSPs	0
BRAM	0

Table 1: Kintex Ultrascale (left) and Cyclone V GT (right)

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.