IObundle Example User Guide

User Guide

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1   Introduction

The IObundle xSPI Flash Controller core is a configurable spi/xspi master interface core for communication with flash memories. It supports automatic controller configuration, Execute-in-Place (XiP) mode, simple and multi-line dual/quad communication protocols and STR (Single Transfer Rates)/DDR (Double Data Rates) modes. The IP is currently supported for use in ASICs and FPGAs.
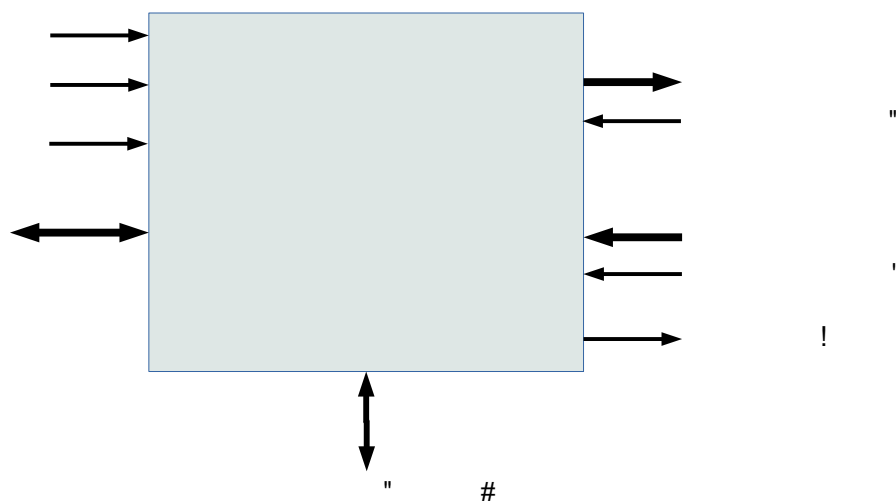
2   Symbol

Figure 1: IP Core Symbol

3   Features

- f1

- f2

4   Benefits

- Easy hardware and software integration

- Compact hardware implementation

- Can fit many instances in low cost FPGAs

- Can fit many instances in small ASICs

- Low power consumption

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5 Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code

- Software driver and example user software

- User documentation for easy system integration
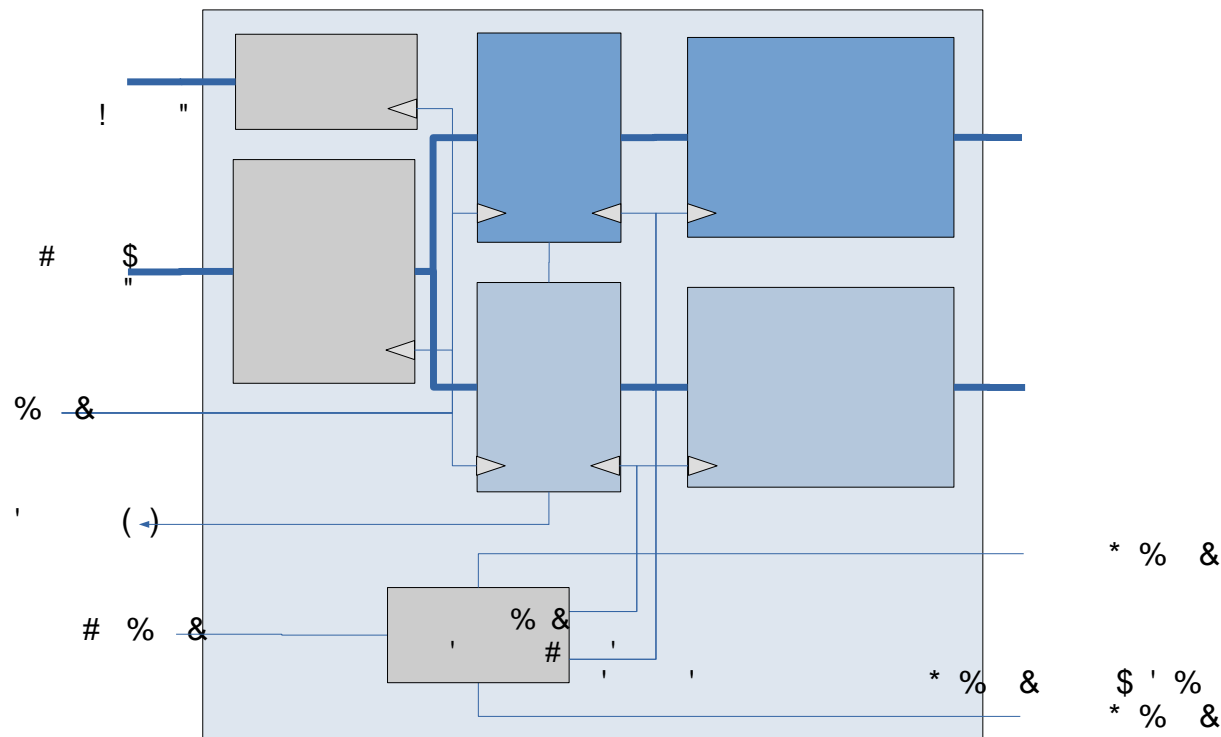
- Example integration in IOb-SoC (optional)

Block Diagram

Figure 2: High-level block diagram

6 Interface Signals

Signal	Direction	Description

Table 1: General interface signals

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7 Timing Diagrams

spi.png
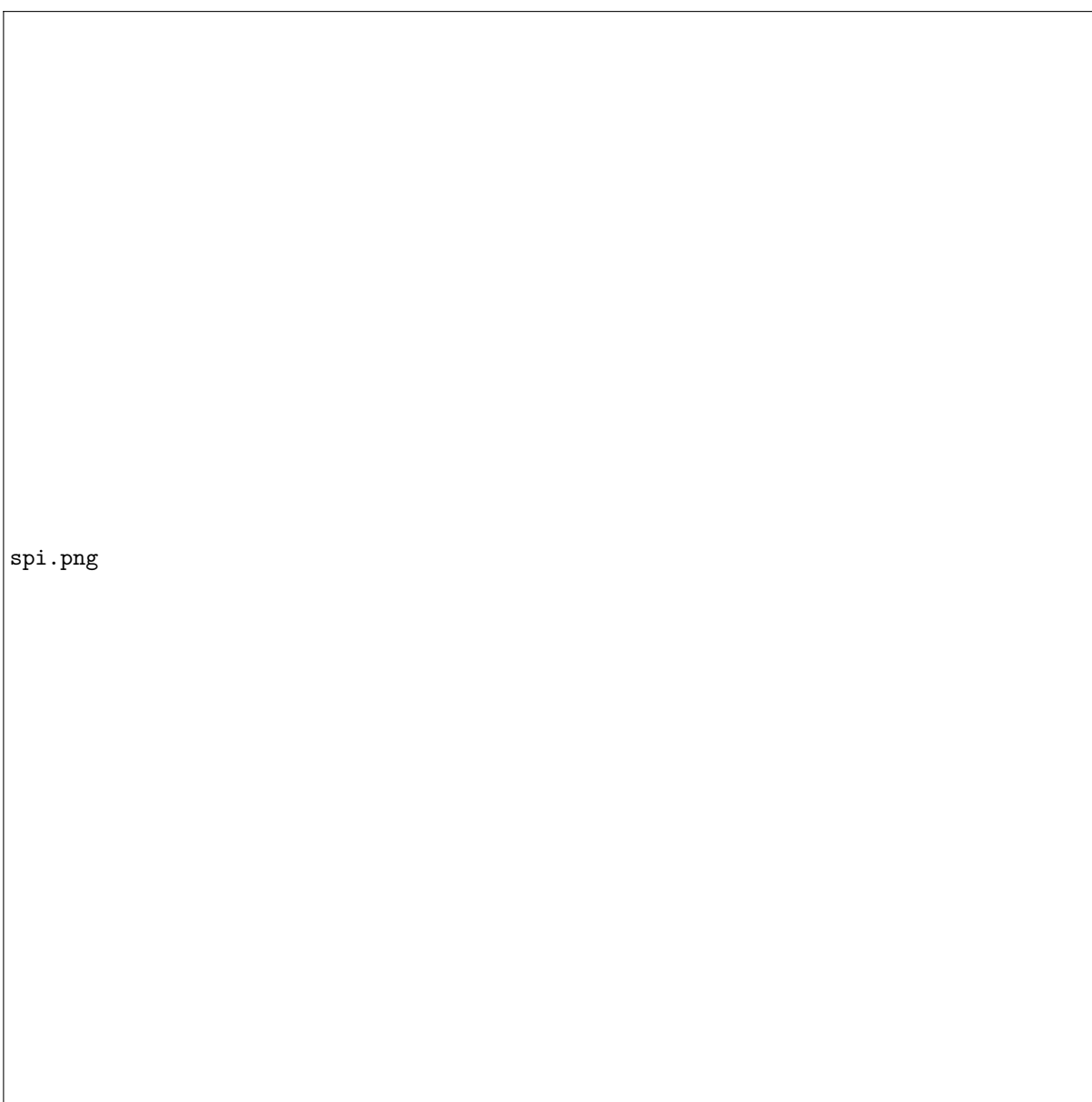
Figure 3: SPI slave interface timing diagram

8   Software Components

FPGA Resources

Resource	Used
LUTs	223
Registers	344
DSPs	0
BRAM	0

Table 2: Kintex Ultrascale (left) and Cyclone V GT (right)

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