IObundle Example User Guide

User Guide

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1 Introduction

The IObundle xSPI Flash Controller core is a configurable spi/xspi master interface core for communication with flash memories. It supports automatic controller configuration, Execute-in-Place (XiP) mode, simple and multi-line dual/quad communication protocols and STR (Single Transfer Rates)/DDR (Double Data Rates) modes. The IP is currently supported for use in ASICs and FPGAs.

2 Symbol

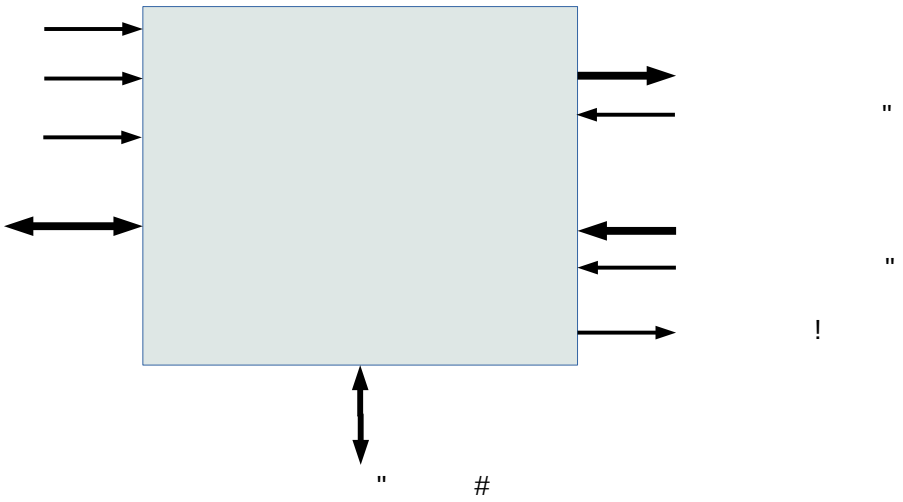

Figure 1: IP Core Symbol

3 Features

- Iob Native interface support
- Configurable spi data lanes: 1, 2 (dual) or 4 (quad) lane modes
- Supports eXecute-In-Place (XIP) mode for low latency memory reads, requiring only memory address. Allows for code execution directly on flash
- Direct access capability (minimum overhead) for flash registers access
- Supports SDR (Single Data Rate) and DDR (Double Data Rate) for increased throughput in low frequency systems
- Fully configurable frame format

4 Benefits

- Easy hardware and software integration

- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption

5 Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code
- Software driver and example user software
- User documentation for easy system integration
- Example integration in IOb-SoC (optional)

Block Diagram

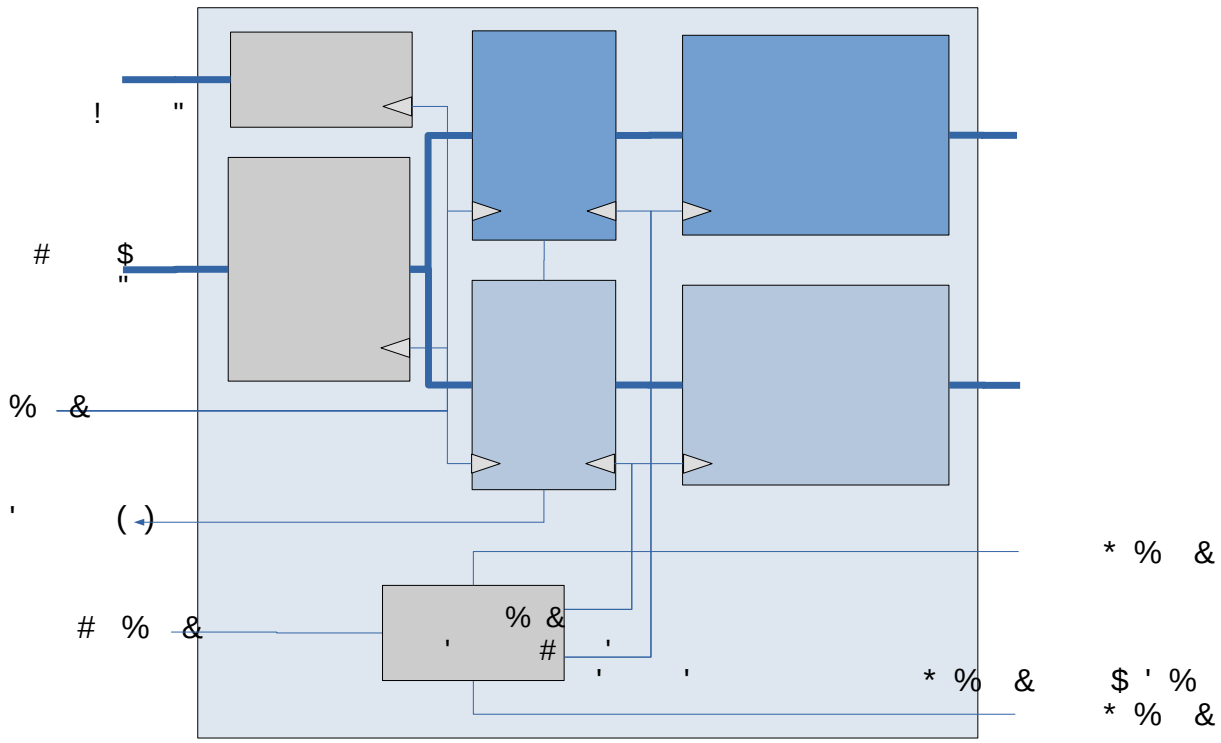

Figure 2: High-level block diagram

6 Interface Signals

Signal	Direction	Description

Table 1: General interface signals

7 Timing Diagrams

spi.png

Figure 3: SPI slave interface timing diagram

8 Software Components

FPGA Resources

The following are FPGA implementation results for two FPGA device families.

Resource	Used
LUTs	223
Registers	344
DSPs	0
BRAM	0

Table 2: Kintex Ultrascale (left) and Cyclone V GT (right)