Overview

The IOb-SoC-Yolo is an IP core for running the Tiny Yolo V3 object detection and classification software based on Convolutional Neural Networks (CNNs). The IP is currently supported in ASICs and FPGAs.

Features

- Runs the Tiny Yolo V3 object detection software
- 1 CNN reconfigurable accelerator (Versat)
- 832 MACC units embedded in the vectorized Functional Units (FUs)
- 13x16 FU matrix organization for massive parallelism
- Each FU performs convolution, maxpool and memory writes
- 256-bit wide data memory accesses
- 30 parallel memory read units
- 208 parallel memory write units
- 1 DMA unit for wide and fast DDR4 access
- 1 RISC-V control and reconfiguration CPU
- Instruction and data caches
- RS232 interfaces for viewing runtime messages
- 16-bit convolution data size
- 15 FPS execution speed (scalable upon availability of bandwidth and compute resources)
- 2-frame latency (from first pixel in to first classification set out)
- Frequency of operation at 125MHz
- Needs external DDR4 memory controller IP

Benefits

- Compact hardware implementation
- Can fit in low cost FPGAs
- Can fit in small ASICs
- Very low power consumption

Block Diagrams

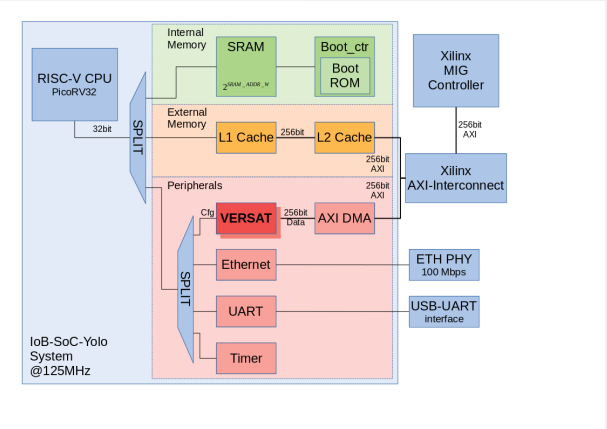

Figure 1: IOb-SoC-Yolo high-level block diagram

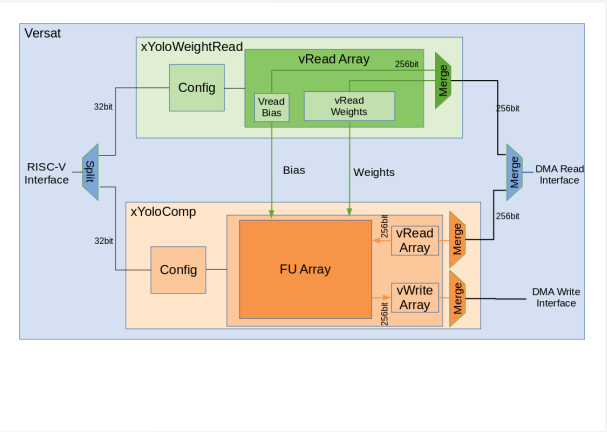

Figure 2: Versat CNN accelerator high-level block diagram

FPGA Resources

Resource	Used
LUTs	69564
Registers	41415
DSPs	254
BRAM	84
PIN	84

Table 1: Implementation Resources for Xilinx Kintex Ultrascale Devices

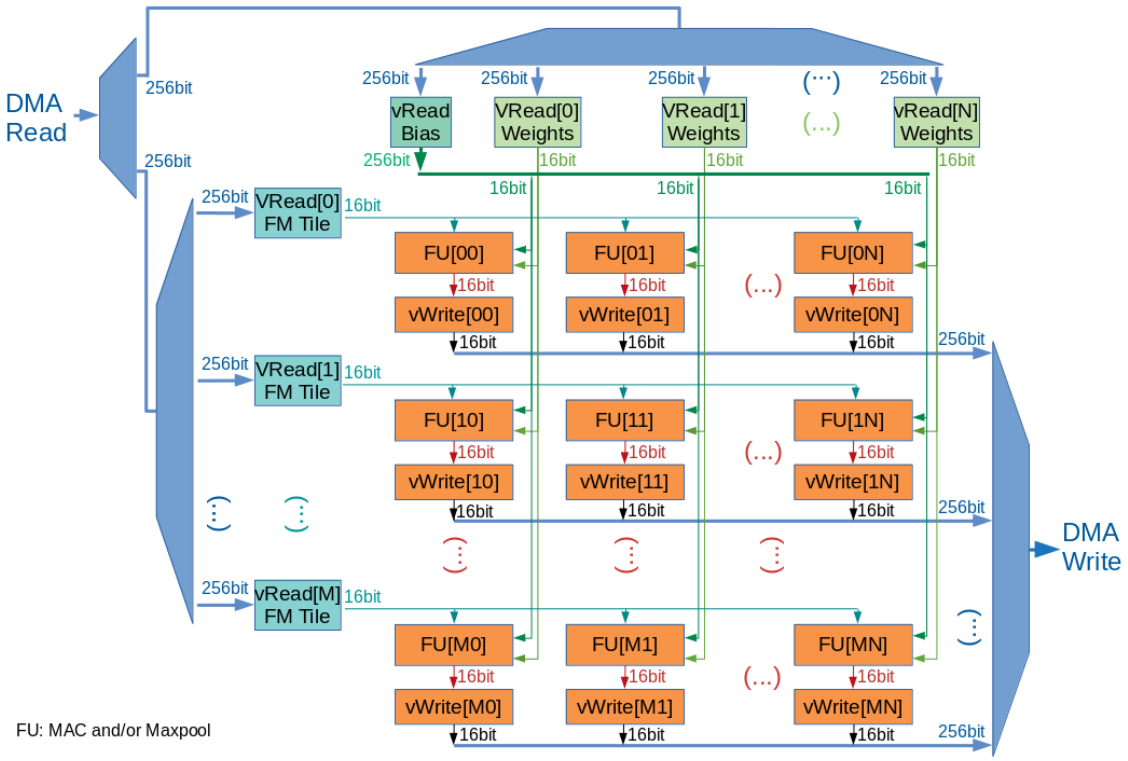

Figure 3: Versat CNN accelerator detailed block diagram

Deliverables

- HDL netlist or source code optionally
- Software object or C++ source code optionally
- Simulation testbench
- Implementation constraints for map, place and route
- Demo files for commercial FPGA board with Ethernet connectivity
- User documentation for system integration

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.