HK32F030M Data Sheet

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foreword

purpose of writing

This document introduces the functional block diagram, memory map, peripheral interface, electrical characteristics, pin package, etc. of the HK32F030M series chips. It is designed to help users quickly understand the features and functions of this series of chips.

Readers

This article is intended for the following readers:

- Development Engineer
- Chip test engineer
- Chip selection engineer

Release Notes

The product series corresponding to this document is HK32F030M series chips.

revision history

Version	date	modify the content
1.0	2020/02/21	Initial Release.
1.0.1	2020/03/04	Updated Section 3.9 “Low Power Modes”.
1.0.2	2020/03/09	Updated Section 4.2.5 "Operating Current Characteristics".
1.0.3	2020/6/19	Updated Section 3.7.2 “Clock Tree”.
1.0.4	2020/7/3	Updated Flash erase time in Section 4.2.9 “Flash memory characteristics”.
1.0.5	2020/10/12	Updated ADC Effective Accuracy in Section 3.23 “ADC”.
1.0.6	2020/10/16	Updated Section 6.4 “QFN20 Package”.
1.1.0	2021/03/18	Updated the ADC characteristics parameters in Section 4.2.14 “ADC Characteristics”.
1.1.1	2021/04/19	Updated Section 4.2.14 “ADC Features”.
1.2.0	2021/11/23	Updated Section 2.1 "Product Features", Section 3.1 "Block Diagram" and Section 3.21 "Flash Features", etc.
1.3	2021/12/20	Updated Section 3.7.2 "Clock Tree", Chapter 6 "Pin Definition", etc.
1.4	2022/09/16	1. Added new models in "1 Introduction", "2.2 Parts List" and "8 Ordering Information": HK32F030MF4N6; 2. Added the package information of the new model HK32F030MF4N6 in "7 Package Parameters"; 3. Corrected the number of counter bits of TIM2, and also corrected some minor
1.4.1	2022/09/22	errors in the full text. 1. Updated "2 Product Overview". 2. Modified Table 1-1 Entry/Wakeup Conditions
1.5	2022/10/09	of Low Power Mode. Updated "3.1 Block Diagram", "3.2 Memory Map", "3.6 Reset", "7.4 QFN20 Package", etc.
1.6	2022/10/14	Updated "8 Ordering Information".
1.7	2023/05/17	1. Modify FLITFCLK in "4.2.9 Flash memory characteristics" and "3.7.2 Clock tree" to 2MHz; 2. Refine the test conditions in the electrical parameter table of "4.2.5 Operating current characteristics".

Version	date	modify the content
		3. Added "7.2 Silkscreen Information" and "8.1 Order Code". 4. Corrected some minor errors in the full text.

Table of contents

1 Introduction

This document is the data sheet of HK32F030M series chips. HK32F030M series chips are developed by Shenzhen Hangshun Chip Technology Co., Ltd. The economical MCU chips developed by Co., Ltd. include the following models:

- HK32F030MF4U6
- HK32F030MF4N6
- HK32F030MF4P6
- HK32F030MD4P6
- HK32F030MJ4M6

Users can refer to the "HK32F030M User Manual" to learn more about the functions of the HK32F030M MCU.

2 Product Overview

HK32F030M MCU uses ARM® Cortex® -M0 core with a maximum operating frequency of 32 MHz, built-in 16 KByte Flash, 448 Byte EEPROM and 2 KByte SRAM. By configuring the Flash controller registers, the remapping of the interrupt vector in the 16 KByte space can be realized.

All pins of HK32F030M MCU except power supply and ground can be used as GPIO, peripheral IO or external interrupt input; In the quantity-constrained application scenarios, the MCU provides as many pin signals as possible.

HK32F030M MCU has a variety of built-in communication interfaces:

- 1-way high-speed (up to 4 Mbit/s) USART USART

  supports synchronous and asynchronous full-duplex or half-duplex communication, multi-host communication, LIN protocol, SmartCard protocol, IrDA SIR codec; RX and TX pins can be interchanged by software position; in the MCU shutdown mode (Stop), it supports data receiving wake-up.

- 1 high-speed (up to 16 Mbit/s) SPI/I2S

  SPI/I2S supports full-duplex or half-duplex communication with 4 ~ 16-bit data length, master/slave mode, TI mode, NSS pulse mode, automatic CRC check and I2S protocol.

- 1 high-speed (up to 1 Mbit/s) I2C

  I2C supports 1 Mbit/s, 400 Kbit/s, 100 Kbit/s transfer rate, master/slave mode, multi-master mode, 7/10-bit addressing and SMBus protocol. In MCU stop mode (Stop), it supports data receiving wake-up.

The HK32F030M MCU has a built-in 16-bit advanced PWM timer (a total of 4 PWM outputs, of which 3 are complementary outputs with dead zone), a 16-bit general-purpose PWM timer (a total of 4 PWM outputs) and a 16-bit basic Timer (timing output CPU interrupt).

HK32F030M MCU has built-in analog circuits: 1 12-bit 1MSPS ADC (8-bit effective precision), 1 power-on/down reset (POR/PDR) circuit and 1 internal reference voltage (obtained through on-chip ADC sampling).

HK32F030M MCU supports rich power consumption modes. In low power consumption mode, HK32F030M can be automatically woken up by the internal low power consumption timer.

HK32F030M MCU works in the temperature range of -40°C ~ +85°C, and the power supply voltage is 1.8 V ~ 3.6 V, which can meet the requirements of most application environments.

Due to its rich peripheral configuration, HK32F030M MCU can be applied to a variety of application scenarios:

• Programmable controllers, printers, scanners

• Motor drive and speed control

• IoT low-power sensor terminal • UAV flight control, PTZ control

• Toy products

• Household appliances

• smart robot

• Smart watches, sports bracelets

2.1 Product Features

• CPU cores

ÿ ARM® Cortex® -M0

ÿ Maximum clock frequency: 32 MHz

ÿ 24-bit System Tick timer ÿ Supports interrupt vector remapping (configured through registers of the Flash controller)

• Operating voltage range: 1.8 V ~ 3.6 V

• Operating temperature range: -40°C ~ +85°C

• Typical operating current

ÿ Run mode: 2.338mA@32 MHz@3.3V (73 ÿA/MHz) ÿ Sleep mode: 1.197mA@32 MHz@3.3V

(35 ÿA/MHz), wake-up time 21 ns ÿ Deep Sleep (DeepSleep) mode: 0.613mA@114 kHz@3.3V, wake-up time 7.8 ÿs

ÿ Stop (Stop) mode: 30.12ÿA@3.3V, wake-up time 10 ÿs (can be woken up by external pin or internal timer)

• CPU tracing and debugging

ÿ SWD debug interface

ÿ ARM® CoreSightTM debug components (ROM-Table, DWT, BPU) ÿ Custom

DBGMCU debug controller (low power mode emulation control, debug peripheral clock control, debug and trace interface distribute)

• memory

ÿ 16 KByte Flash (128 pages, 128 Byte per page; 32-bit data read, 16-bit data write)

ÿ Flash has data security protection function, which can set read protection and write protection separately

ÿ 448 Byte EEPROM

ÿ 2 KByte SRAM

• Data Security

ÿ CRC check hardware unit

• clock

ÿ External GPIO input clock: support 1 ~ 32 MHz

ÿ On-chip high-speed HSI clock: 32 MHz

ÿ On-chip slow LSI clock: 114 kHz

• reset

ÿ External pin reset

ÿ Power on/off reset (POR/PDR)

ÿ Software reset

ÿ Watchdog (IWDG and WWDG) timer reset

• GPIO port

ÿ Support up to 16 GPIO ports (TSSOP20, QFN20 package products)

ÿ Each GPIO can be used as an external interrupt input

ÿ Built-in switchable pull-up and pull-down resistors

ÿ Support open-drain (Open-Drain) output ÿ

Output drive capability is optional

• IOMUX pin function multiple mapping controller

ÿ For small package (such as SOP8) products, a single pin can correspond to multiple GPIOs or peripheral IOs through IOMUX Mapping controls.

• Data communication interface

ÿ 1 high-speed (up to 4 Mbit/s) USART (MCU in stop (Stop) mode, support data receiving wake-up) 1 high-speed (up to

ÿ 1MHz) I2C (MCU in stop (Stop) mode, support data receiving wake-up)

- 1 high-speed (up to 16 Mbit/s) SPI (support I2S protocol)

• Timer and PWM generator

- 1 x 16-bit advanced PWM timer (total of 4 PWM outputs, 3 of which are complementary outputs with dead zone)
- 1 16-bit general-purpose PWM timer (total 4 PWM outputs) 1 16-bit basic
- timer (support CPU interrupt)
- 1 automatic wake-up timer (AWU), which can be used to work in MCU stop (Stop) mode.

• Buzzer

- 1 buzzer, can output 1, 2, 4 or 8 kHz frequency pulse.

ÿ In MCU stop mode, the buzzer can continue to work and trigger ADC sampling regularly.

• On-chip analog circuitry

- 1 12-bit 1 MSPS ADC (a total of 6 internal and external analog signal input channels, support differential pair input)
- 1 power-on/power-down reset circuit
- 1 x 0.8 V internal reference voltage (internal reference voltage is sampled by ADC on-chip)

• ID identification

ÿ 64-bit chip unique ID identification

ÿ Each chip provides a unique 64-bit ID.

• Reliability

ÿ Passed HBM6000V/CDM500V/LU700mA level test.

2.2 Device list

Table 2-1 HK32F030M series chip features

Product Features	HK32F030MJ4M6	HK32F030MD4P6	HK32F030MF4P6	HK32F030MF4U6/ HK32F030MF4N6
Operating Voltage	1.8V ~ 3.6V			
Operating temperature	-40°C ~ +85°C			
CPU operating frequency	32 MHz			
System Tick	1			
Flash	16 KBytes			
EEPROM	448 Bytes			
SRAM	2 KBytes			
CRC	1			
IWDG	1			
WWDG	1			
USART	1			
I2C	1			
SPI/I2S	1			
Advanced Timer 1				
General purpose timer 1				
Basic Timer 1				
AWU timer 1				
buzzer	1			

Product Features	HK32F030MJ4M6	HK32F030MD4P6	HK32F030MF4P6	HK32F030MF4U6/ HK32F030MF4N6
ADC (number of external channels)	1(3)	1(4)	1(5)	1(5)
POR/PDR	1			
Internal reference voltage 1				
64-bit ID identification 1				
External Interrupt	6	14	16	16
GPIOs	6	14	16	16
encapsulation	SOP8	TSSOP16	TSSOP20	QFN20

3 Function Introduction

3.1 Structural block diagram

The ARM® Cortex® -M0 processor is an embedded 32-bit RISC processor, which is a low-cost, low-power MCU platform that provides excellent computing performance and advanced interrupt system response. The HK32F030M MCU has a built-in Cortex® -M0 core, which is compatible with ARM tools and software.

Now take HK32F030MF4U6 as an example to illustrate the functional block diagram of HK32F030M MCU.

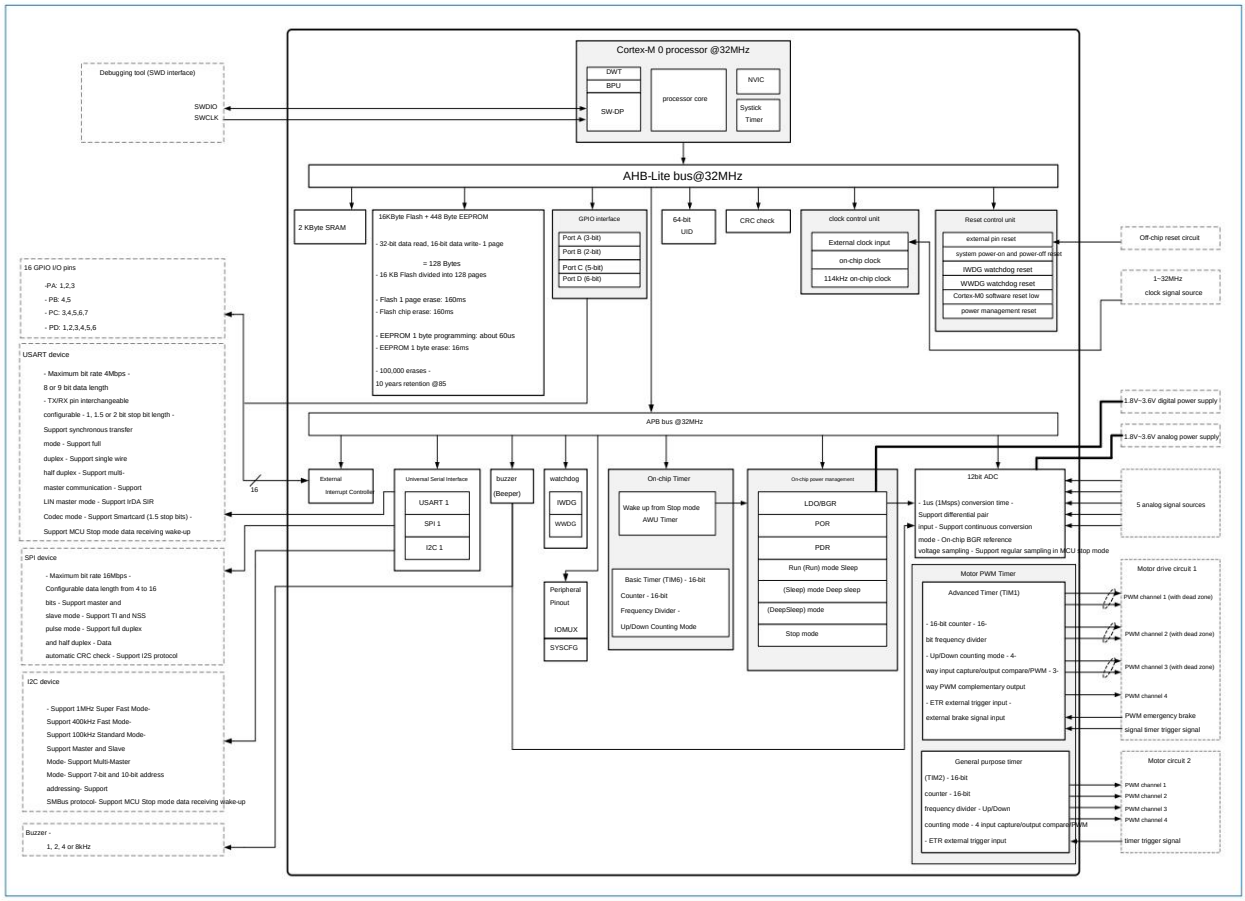

Figure 3-1 Functional block diagram of HK32F030MF4U6

3.2 Memory Mapping

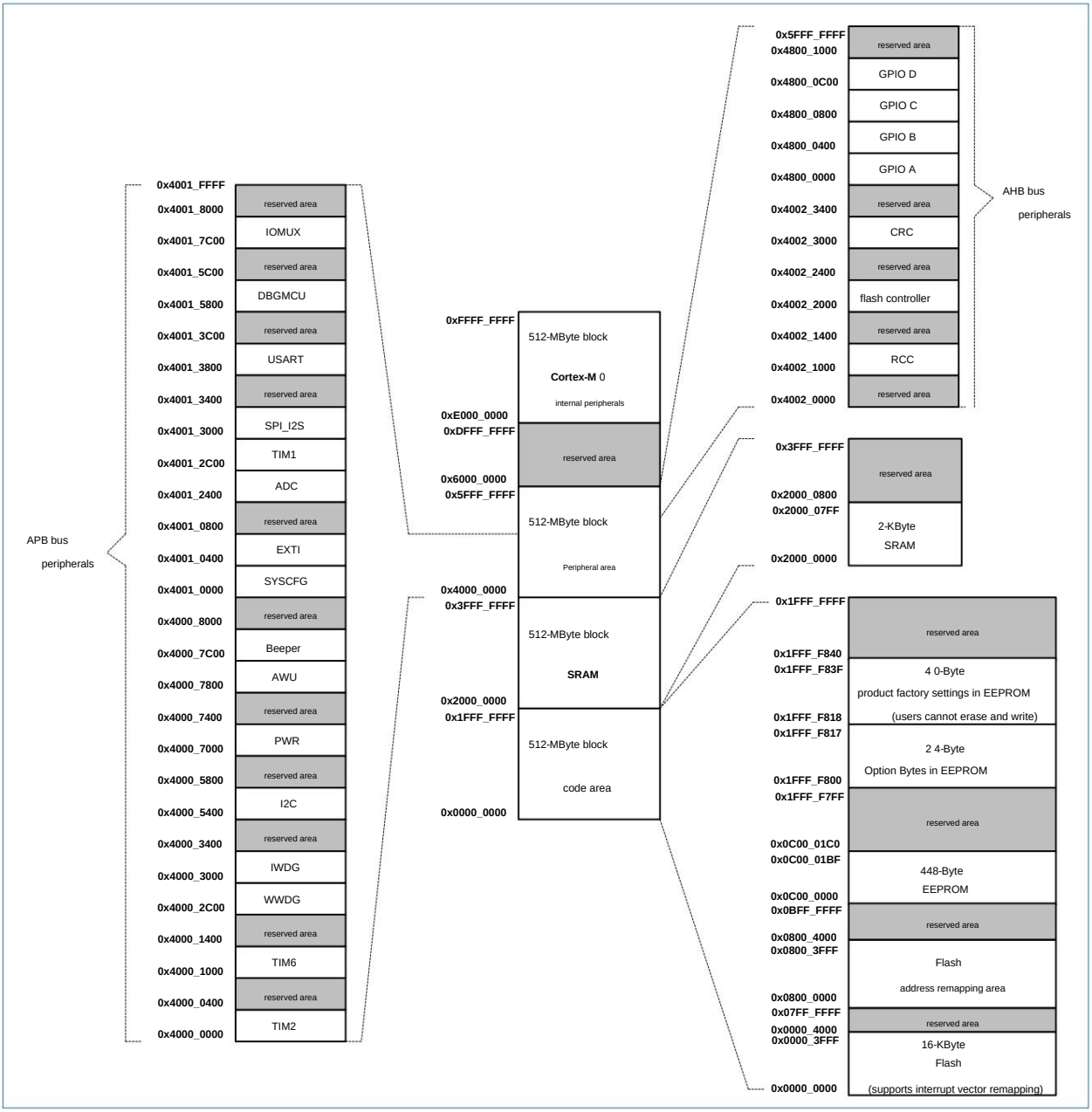

Figure 3-2 HK32F030M MCU memory map

3.2.1 Flash Features

- Flash data width: 32 bits for reading, 16 bits for writing.
- Page size: 128 Byte.
- Flash access bit width: support half-word (16-bit) write; 32-bit read.
- Support Flash read/write protection access control.
- Supports interrupt vector table remapping through configuration registers.

Table 3-1 Flash features

operating time	read operation	Erase and Program Operations
	When 1.8V ÿ VDD ÿ 2.4V: • LATENCY=000 and HCLK ÿ 16 MHz, 0 clock wait cycle.	• Half-word write operation: about 60 ÿs • Flash page erase: about 160 ms (terase = 1/fFLITFCLK*320000) • Flash chip erase: about 160 ms (terase =

	• LATENCY=001 and 16 MHz <HCLK ÿ 32 MHz, 1 clock wait period.	1/fFLITFCLK*320000)
	When 2.4V < VDD ÿ 3.6V: • LATENCY=000 and HCLK ÿ 24 MHz: 0 clock wait cycle. • LATENCY=001 and 24 MHz < HCLK ÿ 48 MHz: 1 clock wait period.	
The service life supports about 100,000 times of erasing and reading and writing.		

3.2.2 Flash option word

Table 3-2 Structure of Flash Option Word

address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF F800	nUSER	USER	nRDP	RDP
0x1FFF F804	nDATA1	DATA1	nDATA0	DATA0
0x1FFF F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF F80C	wRP3	WRP3	wRP2	WRP2
0x1FFF F810	IWDG_INI_KEY[15:0]		reserve	IWDG_RL_IV[11:0]
0x1FFF F814	DBG_CLK_CTL[15:0]		LSI_LP_CTL[15:0]	

• IWDG_RL_IV[11:0]: Store the initial value of the IWDG_RLR register. When IWDG is a hardware watchdog, it can be configured IWDG_RL_IV register to set the reset interval of IWDG.

• IWDG_INI_KEY[15:0]: Determine whether IWDG_RL_IV is valid or not. When the IWDG_INI_KEY register is equal to 0x5B1E, IWDG_RL_IV configuration takes effect, otherwise it is invalid.

• LSI_LP_CTL[15:0]: After enabling the IWDG and then entering the stop (Stop) mode, set whether the system needs to be cycled by the IWDG wake.

ÿ If the value of LSI_LP_CTL is configured as 0x369C, after the MCU enters the Stop mode, the LSI can The setting of the LSI is turned off; after the MCU is woken up, the LSI returns to the state before entering the mode.

ÿ If LSI_LP_CTL is not configured, after enabling IWDG and then entering Stop mode, the system will be woken up periodically by IWDG.

• DBG_CLK_CTL[15:0]: When the stored value is 0x12DE, turn off the CPU internal DEBUG clock, otherwise keep The DEBUG clock is on.

illustrate:

table 3-2 the Address *0x1FFF_F800 ~ 0x1FFF_F80C* For bit field definitions, please refer to *HK32F030M* "User Manual" in " *Flash* Option Byte Register" section.

3.2.3 SRAMs

HK32F030M MCU integrates 2 KByte SRAM inside, which supports word, half word and byte read and write access. The CPU provides fast read and write access to the SRAM with zero wait cycles, meeting the needs of most applications.

3.2.4 EEPROM

HK32F030M MCU integrates 448 Byte EEPROM inside.

Table 3-3 EEPROM characteristics

Operation Time	Read Operation	Erase and Program Operations
	When 1.8V ÿ VDD ÿ 2.4V: • LATENCY=000 and HCLK ÿ 16 MHz, 0 clock wait period. • LATENCY=001 and 16 MHz <HCLK ÿ 32 MHz, 1 clock wait period.	• Byte programming: about 60 ÿs (terase_byte= 1/fFLITFCLK*120)

	When 2.4V < VDD ÿ 3.6V: • LATENCY=000 and HCLK ÿ 24 MHz: 0 clock wait period. • LATENCY=001 and 24 MHz < HCLK ÿ 48 MHz: 1 clock wait period.	• Byte erase: about 16 ms (terase_byte= 1/fFLITFCLK*32000)
The service life supports about 100,000 times of erasing and reading and writing, or a service life of 10 years (whichever comes first).		

3.3 CRC calculation unit

A cyclic redundancy check (CRC) is used to verify the integrity of data transmission or data storage. HK32F030M integrates an independent The CRC hardware calculation unit reduces the burden for user applications and provides accelerated processing capabilities.

The CRC calculation unit calculates the signature of the software during operation, and combines it with the reference generated at link time and stored in the specified storage address signatures for comparison.

3.4 NVICs

HK32F030M has a built-in nested vectored interrupt controller (NVIC), which provides flexible interrupt management functions with minimal interrupt latency. HK32F030M has a total of 21 external interrupts.

- Tightly coupled NVIC enables low-latency interrupt response processing.
- The interrupt vector entry address goes directly to the core.
- Provides a tightly coupled NVIC interface. • Allows early handling of interrupts.
- Handle late arriving higher priority interrupts.
- Supports interrupt tail chaining functionality.
- Automatically save processor state.
- Automatic recovery on return from interrupt without additional instruction overhead.

Table 3-4 NVIC table

location priority			name	describe	address
-	-	-	-	reserve	0x0000 0000
-	-3	fixed	Reset	reset	0x0000 0004
-	-2	fixed	NMI	NMI	0x0000 0008
-	-1	fixed	Hard Fault	all type errors	0x0000 000C
-	3	Configurable SVCall		System service scheduling via SWI command 0x0000 002C	
-	5	Configurable PendSV		Pending System Service Requests	0x0000 0038
-	6	Configurable SysTick		System tick timer	0x0000 003C
0	7	Configurable WWDG		Window watchdog interrupt	0x0000 0040
1	8	Configurable-		-	0x0000 0044
2	9	Configurable EXTI11		Auto Wakeup Interrupt on EXTI Line 11 (AWU_WKP) 0x0000 0048	
3	10	Configurable Flash		Flash global interrupt	0x0000 004C
4	11	Configurable RCC		RCC global interrupt	0x0000 0050
5	12	Configurable EXTI0		EXTI line 0 interrupt	0x0000 0054
6	13	Configurable EXTI1		EXTI line 1 interrupt	0x0000 0058
7	14	Configurable EXTI2		EXTI line 2 interrupt	0x0000 005C
8	15	Configurable EXTI3		EXTI line 3 interrupt	0x0000 0060
9	16	Configurable EXTI4		EXTI line 4 interrupt	0x0000 0064

location priority		name	describe	address
10	17	Configurable EXTI5	EXTI line 5 interrupt	0x0000 0068
11	18	Configurable TIM1_BRK	TIM1 brake interrupt	0x0000 006C
12	19	Configurable ADC	ADC interrupt (shared with EXTI line 8)	0x0000 0070
13	20	Configurable TIM1_UP_TRG_COM TIM1 update, trigger and Com interrupt		0x0000 0074
14	twenty one	Configurable TIM1_CC	TIM1 capture compare interrupt	0x0000 0078
15	twenty two	Configurable TIM2	TIM2 global interrupt	0x0000 007C
16	twenty three	Configurable-	-	0x0000 0080
17	twenty four	Configurable TIM6	TIM6 global interrupt	0x0000 0084
18	25	Configurable-	-	0x0000 0088
19	26	Configurable-	-	0x0000 008C
20	27	Configurable-	-	0x0000 0090
twenty one	28	Configurable EXTI6	EXTI line 6 interrupt	0x0000 0094
twenty two	29	Configurable EXTI7	EXTI line 7 interrupt	0x0000 0098
twenty three	30	Configurable I2C	I2C global interrupt (shared with EXTI line 10)	0x0000 009C
twenty four	31	Configurable-	-	0x0000 00A0
25	32	Configurable SPI	SPI global interrupt	0x0000 00A4
26	33	Configurable-	-	0x0000 00A8
27	34	Configurable USART	USART global interrupt (shared with EXTI line 9) 0x0000 00AC	
28	35	Configurable-	-	0x0000 00B0
29	36	Configurable-	-	0x0000 00B4
30	37	Configurable-	-	0x0000 00B8
31	38	Configurable-	-	0x0000 00BC

3.5 EXTI

HK32F030M MCU has built-in 12 external interrupt (EXTI) ports. Among them, EXTI 0 ~ EXTI 7 are connected to IO, and the remaining EXTI ports are connected to the following events:

- EXTI 8 AWD event connected to ADC
- EXTI 9 Wake-up event connected to USART
- EXTI 10 Wake-up event connected to I2C
- EXTI 11 Wake up event connected to AWU

EXTI8 ~ 10 as internal events, without RTSR, FTSR, SWIER and PR registers, can only be collected in stop (Stop) mode The rising edge of the event generates ERQ and IRQ signals to wake up the system.

3.6 Reset

HK32F030M MCU supports two reset methods: system reset and power reset.

3.6.1 System reset

A system reset resets all have registers to their reset state. A system reset is generated when any of the following events occur:

- Low on NRST pin (external reset)
- Window watchdog count terminated (WWDG reset)

• Independent watchdog count terminated (IWDG reset)

• Software reset (SW reset): By setting the Cortex® -M0 interrupt application and reset the SYSRESETREQ bit in the control register
Set to '1' for software reset.

• Low power management reset

Users can identify the source of reset events by viewing the reset status flags in the RCC_CSR control status register.

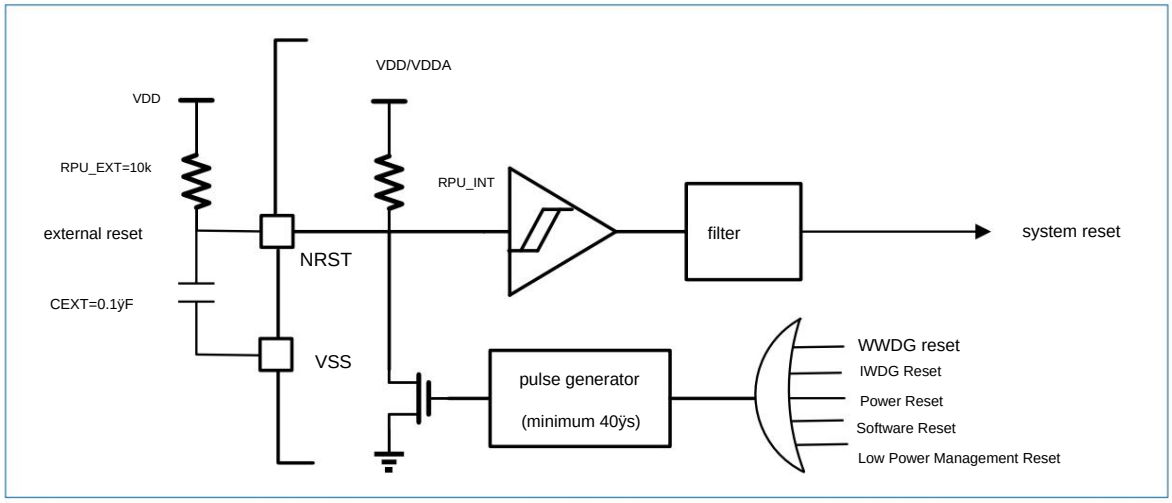

Figure 3-3 Reset circuit

The reset source will eventually act on the NRST pin and keep it low during the reset process. The reset entry vector is fixed at address 0x0000 0004.

The reset signal inside the chip will be output on the NRST pin. The pulse generator guarantees at least 40 ÿs of each internal reset source pulse delay. When the NRST pin is pulled low to generate an external reset, it will generate a reset pulse.

3.6.2 Power reset

A power reset is generated when the following events occur:

• Power-on/power-down reset (POR/PDR) A power

reset will reset all registers except the backup area.

The HK32F030M MCU integrates a power-on reset (POR)/power-down reset (PDR) circuit. This circuit is always active to ensure that the system operates normally when the power supply exceeds the POR/PDR threshold. When VDD is less than POR/PDR threshold, MCU will be reset without using external reset circuit.

3.7 Clock

HK32F030M MCU selects the system clock at startup. When reset, the internal 32 MHz HSI RC is the default CPU clock, which can then be Select the LSI clock as the CPU clock.

HK32F030M MCU also provides LSI, GPIO input as the clock source, making it suitable for low-power, low-cost design solutions.

3.7.1 Clock source

Table 3-5 Clock sources

HSI clock	• Output frequency 32 MHz • Accuracy: full temperature range ± 1%
LSI clock	• Output frequency 114 kHz • Accuracy: ± 4% of full temperature range
GPIO input clock	EXTCLK1/EXTCLK2/EXTCLK3/EXTCLK4, supports input up to 32 MHz

3.7.2 Clock tree

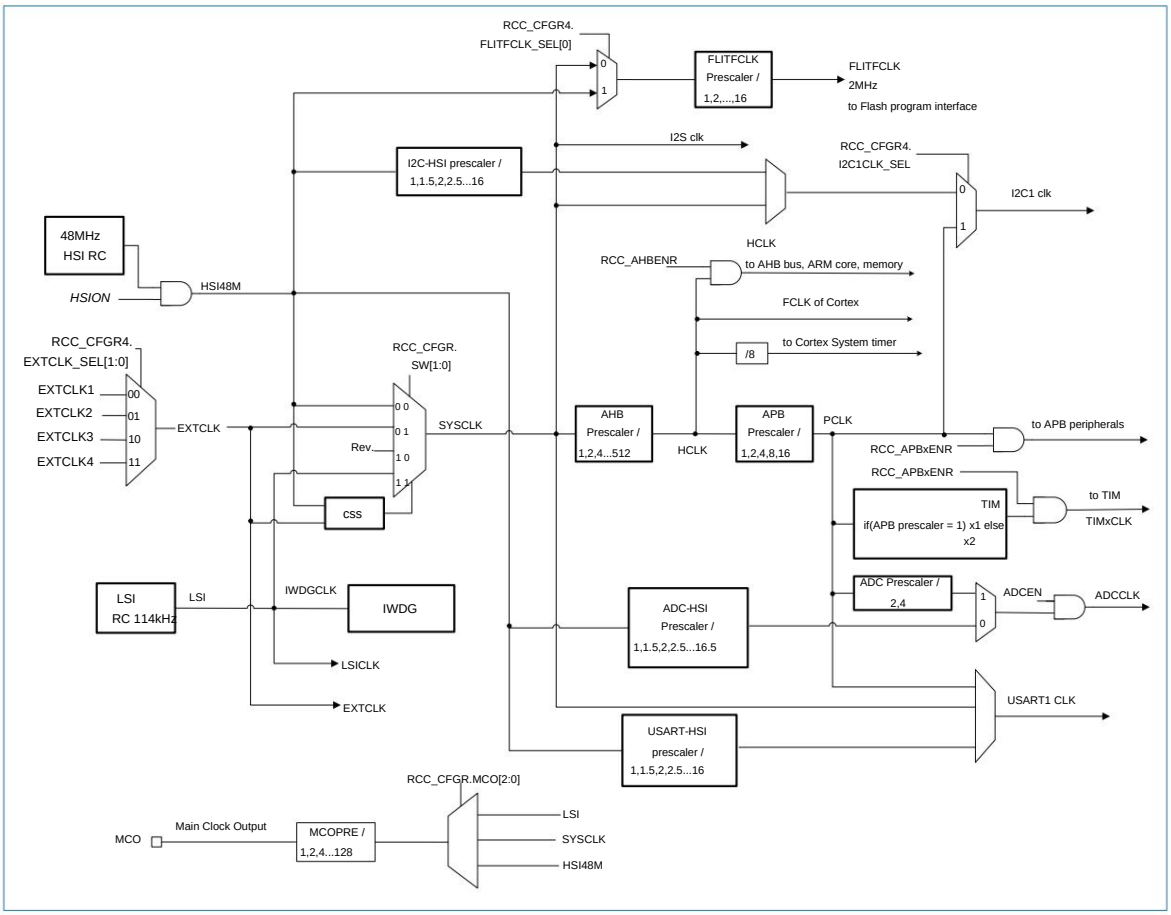

Figure 3-4 Clock tree

- SYSCLK: Optional HSI32M, LSI and GPIO input clock, the default is HSI32M clock.
- HCLK: Default AHB prescaler is divide by 6.
- FLITFCLK: Selectable HSI32M and SYSCLK clock.
- GPIO input clock frequency threshold adjustable for CSS detection.

3.8 Power supply scheme

HK32F030M MCU adopts single power supply, and VDD and VDDA share the same pin to supply power for digital and analog circuits of MCU. VDD/VDDA ranges from 1.8 to 3.6 V.

3.9 Low Power Mode

HK32F030M MCU supports multiple power consumption modes, which can achieve the best balance between low power consumption, short startup time and multiple wake-up events Balance.

- Sleep mode

  In sleep mode, only the CPU is stopped, all peripherals are active and can wake up on interrupts/events CPU.

- Deep Sleep mode

  In Deep-sleep mode, the system clock is reduced to 114 kHz to save power. In this mode, only the CPU stops working, all peripherals are working and interrupts/events can occur to wake up the CPU. Deep-sleep mode consumes more power than Stop mode.

- Stop mode

Shutdown mode achieves the lowest power consumption while maintaining the contents of SRAM and registers. In stop mode, all clocks to the core domain are turned off, and the RC oscillator of the HSI is turned off.

The MCU can be woken up from shutdown mode by any signal configured as EXTI. The EXTI signal can be any external I/O port.

Table 3-6 Working modes and power consumption

Operating mode	Power consumption index	wake up time
operating mode	Dynamic power consumption: 2.338mA@32 MHz@3.3V (73 ÿA/MHz)	-
sleep mode	Dynamic power consumption: 1.197mA@32 MHz@3.3V (35 ÿA/MHz)	21 ns
deep sleep mode	Static power consumption: 0.613mA@114 kHz@3.3V	Fastest 7.8 ÿs wake-up
shutdown mode	Static power consumption: 30.12ÿA@3.3V	10ÿs

The entry and wake-up conditions of low-power mode are as follows.

Table 3-7 Entry/Wakeup Conditions of Low Power Mode

Working mode entry condition		wake up condition	Internal Core Power Clock Status	VDD main area clock status	Voltage Regulator Status
sleep mode (Sleep)	1. Set PWR_CR:LPDS = 0; 2. The software executes WFI/WFE instruction to enter.	Wake up by any normal IRQ interrupt event, including System ticker.	CPU clock off, no effect on other clocks and ADC clock	open open	
deep sleep mode (Deep Sleep)	1. Switch the clock to LSI; 2. Set PWR_CR:LPDS = 0; 3. The software executes WFI/WFE instruction to	Wake up by any normal IRQ interrupt event, including System ticker.	CPU clock off, no effect on other clocks and ADC clock	open open	
shutdown mode (Stop)	enter. 1. Set PWR_CR:LPDS = 0; 2. Set the SLEEPDEEP bit of the CM0 system control register; 3. The software executes the WFI/WFE instruction to enter.	• Support any EXTI external interrupt line call Awake. • If executing WFI to enter stop mode: set any external interrupt line to interrupt mode (the corresponding external interrupt vector must be enabled in NVIC). " • If executing WFE to enter shutdown mode: Set any external interrupt line to event mode. " • Support Beeper to drive ADC sampling pre-wake-up. When the conditions are met, it will really wake up. • Support automatic wake-up timer (AWU) to wake up Awake.	all clocks stop	HSI off on or in low power (in set in PWR_CR)	

3.10 Independent watchdog

The independent watchdog is clocked by an internal independent 114 kHz RC oscillator with a 12-bit down counter and a 8-bit prescaler. Since the RC oscillator is independent of the main clock, it can run in stop mode. The IWDG can be used as a watchdog to reset the entire system when a problem occurs or as a freewheeling timer to provide timeout management for applications. Through the option byte field, it can be configured as a software or hardware start watchdog. In debug mode, this counter can be frozen.

3.11 Window watchdog

The window watchdog has a 7-bit down counter inside. The counter can be set to free-running mode, or used as a watchdog to reset the entire system in the event of a system crash. The window watchdog is driven by the main clock and has an early warning interrupt function. In debug mode, this counter can be frozen.

3.12 System Tick Timer The System Tick

timer is dedicated to the operating system and can be used as a standard down counter with the following characteristics.

• 24-bit down counter • Reload function

• A maskable interrupt can be generated when the counter reaches 0

• Programmable clock source

3.13 Basic Timer

HK32F030M MCU integrates a basic timer TIM6.

The basic timer has a built-in 16-bit counter and 16-bit prescaler, and supports increment, decrement, and increment/decrement counting modes. basic timer Used to generate CPU timing interrupt requests. In debug mode, this counter can be frozen.

3.14 General purpose timer

HK32F030M MCU integrates a synchronous 4-channel general-purpose timer TIM2.

A general purpose timer can generate a PWM output, or serve as a simple time reference. TIM2 with a 16-bit auto-reload up/down count register and a 16-bit prescaler. In debug mode, this counter can be frozen.

TIM2 can work with advanced control timers through the timer chaining function, providing synchronous or event chaining functions and can handle quadrature (incremental) encoder signal and digital output from 1 to 3 Hall effect sensors.

3.15 Advanced Timers

HK32F030M MCU integrates an advanced timer TIM1.

The advanced timer (TIM1) can be used as a three-phase PWM generator distributed to 6 channels, or as a complete general-purpose timer. Four independent channels can be used for:

• input capture

• output compare

• Generate PWM (edge or center-aligned mode)

• Single pulse output •

Complementary PWM output with programmable dead-band insertion.

When the Advanced Timer is configured as a 16-bit Basic Timer, it has the same functionality as the Basic Timer. It has full modulation capability (0 ~ 100%) when configured as a 16-bit PWM generator. Since the internal structure and most of the functions are the same as the general-purpose timer, the advanced timer can cooperate with the general-purpose timer through the timer link function to provide synchronization or event link function.

In debug mode, the counters can be frozen.

3.16 AWU timer

HK32F030M MCU integrates an automatic wake-up (AWU) timer. The AWU timer is used to time the timer in Stop mode and generate an interrupt to wake up the MCU. AWU has a built-in ultra-low power consumption 22-bit timer, and its operating clock can be configured as 1 ~ 32 MHz GPIO input clock or 114 kHz on-chip slow clock (LSI). The AWU timer uses a countdown method.

3.17 Buzzer (Beeper)

The buzzer has a built-in ultra-low power 7-bit timer, and the working clock of the timer can be configured as 1 ~ 32 MHz GPIO external input clock or 114 kHz on-chip slow clock (LSI). The timer uses a decremental counting method and can output 1, 2, 4 or 8 kHz frequency pulses.

In MCU shutdown (Stop) mode, the buzzer can continue to work and trigger ADC sampling regularly. Timing trigger ADC sampling frequency

1/1024 of the pulse frequency of the buzzer output. For example: if the buzzer pulse currently output by the buzzer is 1 kHz, the timing trigger ADC sampling frequency is 1 kHz/1024 ÿ 0.98 Hz (period is about 1.02 seconds).

3.18 I2C bus

A single I2C-bus interface, capable of operating in master and slave modes, supports standard, fast and ultra-fast modes. The I2C interface supports 7-bit or 10-bit addressing, and supports dual-slave addressing when working in 7-bit slave mode. The I2C interface has a built-in hardware CRC generator/checker and supports SMBus V2.0/PMBus bus.

3.19 USARTs

HK32F030M MCU has a built-in universal synchronous/asynchronous transceiver (USART), and the interface communication rate can reach 4 Mbit/s.

The USART supports multiprocessor communication, master synchronous communication, and single-wire half-duplex communication modes. USART interface also supports smart card communication (ISO 7816) protocol, IrDA SIR ENDEC specification, LIN master/slave functional mode, and auto-baud rate detection feature.

The USART interface can wake up the MCU from Stop mode using a clock domain independent of the CPU clock.

Table 3-8 USART features

USART Modes/Features	USART
DMA transfer	not support
multiprocessor communication	support
synchronous mode	support
Single-wire half-duplex communication	support
Dual Clock Domains and Wake-up from Stop	support
Auto baud rate detection	support
Modbus communication	support
RS232 hardware flow control	not support
RS485 driver enable	not support
IrDA SIR ENDEC Module	support
LIN mode	support
smart card mode	support

3.20 SPI

HK32F030M MCU has 1 SPI interface, up to 16 Mbit/s communication, supports slave and master mode, full-duplex and half-duplex communication model. The SPI can use a 3-bit prescaler to generate 8 master-mode frequencies, and each frame can be configured as 4-bit to 16-bit data.

The standard I2S interface (multiplexed with SPI) supports four different audio standards and supports master or slave half-duplex communication modes. The I2S interface is synchronized by dedicated signals and can be configured for 16-bit, 24-bit or 32-bit transfers, providing 16-bit or 32-bit data resolution. The I2S interface can be set to an audio sampling frequency from 8 kHz to 192 kHz by an 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components.

Table 3-9 SPI features

SPI characteristics	Whether to support
Hardware CRC calculation	support
RX/TX FIFOs	support
NSS pulse mode	support
I2S mode	support
TI mode	support

3.21 GPIOs

Each GPIO pin can be configured by software as an output (push-pull or open), an input (dangling input, pull-up input or pull-down input) or other peripheral function ports. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins have high current capability. Peripheral functions for I/O pins can be locked on demand to avoid accidental writes to I/O registers.

3.22 ADCs

ADC features of the HK32F030M MCU include:

- There are only 6 channels in total. Among them, AIN0 ~ AIN4 are connected to IO for external channels, and AIN5 is connected to internal reference voltage for internal channels. pressure.
- Support differential input mode, AIN0 and AIN1, AIN2 and AIN3 form two sets of differential input (when the ADC is configured as differential input mode, AIN4 and the internal ADC channel for sampling BGR voltage are not available).
- Only 12-bit ADC sampling resolution is supported.

3.22.1 ADC external trigger source

Table 3-10 ADC external trigger source

name	source	External trigger selection mode (EXTSEL[2:0])
TRG0	TIM1_TRGO	000
TRG1	TIM1_CC4	001
TRG2	TIM2_TRGO	010
TRG3	TIM6_TRGO	011
TRG4	TIM1_CC1	100
TRG5	TIM1_CC2	101
TRG6	TIM1_CC3	110
TRG7	IO_TRIG	111

IO_TRIG can be triggered by any IO, and the user needs to set the MODER and AFR registers corresponding to the IO. For details, refer to "HK32F030M "GPIO Registers" chapter of User Manual.

3.22.2 AWD wake-up function

In Stop (Stop) mode, the system can time the buzzer and send a signal to the ADC; the ADC collects the signal to wake up the ADC clock; the ADC clock is ready to trigger the ADC conversion, and generate an AWD event according to the ADC conversion result; the AWD event Output to EXTI to wake up the system.

To use this function, in addition to configuring AWD-related thresholds and channels, you also need to configure the ADC_CR2.WAKE_EN register, including the corresponding timing control inside the buzzer and the ADC wake-up function enable register.

3.23 64 -bit UIDs

The reference number provided by the 64-bit product unique identifier (UID) is unique to any HK32F030M chip under any circumstances. Users cannot modify this ID. Depending on usage, the 64-bit UID can be read in bytes (8 bits), halfwords (16 bits), or fullwords (32 bits). 64-bit UIDs are suitable for the following applications:

- Used as a serial number (eg USB character serial number or other terminal applications).
- Used as a password. When writing flash memory, use this UID in combination with software encryption and decryption algorithms to improve code security within.
- Used to activate the bootstrap process with security mechanisms.

3.24 Debug interface

Embedded with ARM's SWJ-DP interface, it combines the single-wire debug interface to realize the connection of the serial single-wire debug interface (SWDIO and SWCLK).

4 Electrical performance indicators

4.1 Absolute Maximum Ratings

Maximum ratings are pressure values for short periods of time only. Notice:

- Do not use the chip at this value or any other conditions exceeding this recommended value.
- Please refer to the table for the maximum rating of the chip *4-1* to table *4-19*, Exceeding the maximum ratings may cause permanent damage to the chip.
- Operating at maximum ratings for extended periods of time may affect chip reliability.

4.1.1 Limiting voltage characteristics

Table 4-1 Limit voltage characteristics

symbol	describe	minimum value	maximum value	unit
VDD-VSS	External main supply voltage (including VDDA and VDD)	-0.5	4.0	V
VIN	The input voltage on the pin	VSS - 0.3	VDD + 4.0	
|ÿVDDx|	Voltage difference between different supply pins	-	50	mV
|VSSX ÿ VSS|	The voltage difference between different ground pins	-	50	

4.1.2 Limiting current characteristics

Table 4-2 Limiting current characteristics

symbol	describe	maximum value	unit
IVDD	Total current through VDD/VDDA power lines (supply current)(1)	150	mA
IVSS	Total current through VSS ground (source current)(1)	150	
IIO	Output current sink on any I/O and control pin	25	
	Output Sourcing Current on Any I/O and Control Pins	-25	
IINJ(PIN) (2)	Injected current on pin (3)	±5	
ÿIINJ(PIN)	Total injected current on all I/O and control pins (4)	±25	

(1). All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply system within the allowable range.

(2). The reverse injection current will disturb the analog performance of the device.

(3). When VIN >VDD, there is a positive injection current; when VIN < VSS , there is a reverse injection current, and the injection current must not exceed the specified range.

(4). When several I/O ports have injection current at the same time, the maximum value of ÿIINJ (PIN) is the sum of the immediate absolute values of forward injection current and reverse injection current.

4.1.3 Extreme temperature characteristics

Table 4-3 Extreme temperature characteristics

symbol	describe	parameter value	unit
TSTG	storage temperature range	-45 ~ +150	°C
TJ	maximum junction temperature	125	

4.2 Working parameters

4.2.1 Recommended working conditions

Table 4-4 Recommended working conditions

symbol	describe	minimum value	maximum value	unit
wxya	Internal AHB clock frequency 0		32	MHz
fPCLK	Internal APB clock frequency 0		32	
VDD/VDDA	Working Voltage (1)	1.8	3.6	V
T	Operating temperature	-40	85	°C

(1). VDD and VDDA are combined inside the chip and powered by a single external power supply. It is recommended to increase the filter capacitor.

4.2.2 Reset and low voltage detection

Table 4-5 Power-on reset characteristics

symbol	parameter	condition	minimum value	typical value	maximum value	unit
Tdelay	rstn build time -		-	40		ÿs
VThreshold	Reset Threshold -		-	1.75		V

4.2.3 Power-on/power-off reset characteristics

Table 4-6 Power-on/power-off reset characteristics

symbol	parameter	condition	minimum value	typical value	maximum value	unit
VPOR/PDR(1) power-on reset threshold falling edge(2)			1.8	1.88	1.96(3)	V
		rising edge	1.84(3)	1.92	2.00	V
VPDRhyst	PDR hysteresis	-	-	40	-	mV
tRSTTEMPO(3) reset time		-	1.50	2.50	4.50	ms

(1) PDR monitors VDD and VDDA, POR monitors only VDD.

(2) The measured value of the product can be guaranteed to be lower than the minimum value of VPOR/PDR.

(3) The data are theoretical design values, not actual test values.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

symbol	parameter	condition	minimum value	typical value	maximum value	unit
VREFINT	Internal reference voltage	-40 ~ 85°C	-	0.8	-	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

model	condition	VDD=3.3V			unit
		-40°C	25°C	85°C	
Run mode SYSCLK = HSI (32 MHz);	All IOs are configured as high- impedance state; except Flash, SRAM and RCC, other peripherals are turned off;	2.572	2.599	2.704	mA

model	condition	VDD=3.3V			unit
		-40°C	25°C	85°C	
	APB clock enable; get value from Flash, and read from Flash for 2 wait cycles.				
	SYSCLK = HSI(32MHz); All IOs are configured as high-impedance state; Except Flash, SRAM and RCC, other peripherals are turned off; APB clock is disabled; read value from Flash, and read 2 wait cycles from Flash.	2.326	2.338	2.501	mA
	SYSCLK = LSI(114kHz); All IOs are configured as high-impedance state; except Flash, SRAM and RCC, other peripherals are turned off; APB clock is disabled; read values from Flash, and read from Flash with 0 wait cycles.	1.802	1.711	1.822	mA
Sleep mode SYSCLK= 32MHz; AHB/	APB off; core clock off; all IOs configured as high-impedance; except SRAM, Flash data retention, all other peripherals off.	1.097	1.197	1.477	mA
Deep Sleep mode	SYSCLK = 114kHz; AHB/APB is closed; core clock is closed; all IOs are configured as high-impedance state; except for SRAM and Flash data retention, all other peripherals are closed.	0.548	0.613	0.728	mA
All clocks are stopped in Stop mode;	HSI, LSI oscillator off; LDO operates in low power mode; All IOs are configured as high impedance; AWU peripherals are enabled and all other peripherals are disabled.	21.83	34.08	213.6	ÿA
	all clocks stop; HSI, LSI oscillator off; LDO operates in low power mode; All IOs are configured as high-impedance; AWU peripherals are disabled and all other peripherals are turned off.	18.02	30.12	210.44	ÿA

4.2.6 HSI clock characteristics

Table 4-9 Internal fast clock (HSI) characteristics

symbol	parameter	condition	Min	Typ	Max	Unit
wxya	Clock frequency-		-	32	-	MHz
DuCy (HSI) Duty Cycle -			45	-	55	%
ACC	Oscillator Accuracy	After user calibration of the RCC_CR register -		-	1	
		Factory calibrated, TA= -40 ~ +85°C	-1	-	1	%
Tsu (HSI) oscillator start-up time		VSS ÿ VIN ÿ VDD	1	-	2	ÿs
IDD (HSI)	Oscillator Power Consumption -		-	80	100	ÿA

4.2.7 **LSI** clock characteristics

Table 4-10 Internal slow clock (LSI) characteristics

Symbolic parameters		condition	Min Typ Max Unit			
fLSI	Clock frequency	-	-	114	-	kHz
DuCy (LSI) duty cycle		-	45	-	55	%
ACC	Oscillator Accuracy	Factory default: TA=-40 ~+85 °C	1.5	-	2.2	
Tsu(LSI) oscillator startup time VSS ÿ VIN ÿ VDD			1	-	2	ÿs
IDD(LSI) Oscillator Power Consumption		-	-	5	8	ÿA

4.2.8 **GPIO** input clock

HK32F030M MCU supports clock input from EXTCLK1/EXTCLK2/EXTCLK3/EXTCLK4, the requirements are as follows:

Table 4-11 GPIO input clock characteristics

symbol	parameter	minimum value	typical value	maximum value	unit
Fext	input clock frequency	1	8.0	32	MHz
	Input clock duty cycle 40		-	60	%
Jitter	loop jitter	-	-	300	ps

4.2.9 **Flash** memory characteristics

Table 4-12 Flash memory characteristics

symbol	parameter	minimum value	typical value	maximum value	unit
TPROG	half word write time	-	60	-	µs
TERASE	page erase time	120	160	200	ms
	chip erase time	120	160	200	ms
IDDPROG	half word write current	-	-	5	mA
IDDERASE	Page/chip erase current	-	-	2	mA
IDD READ	Read current @24MHz	-	2	3	mA
	Read Current@1MHz	-	0.25	0.4	mA
NEND	Erase life	100	-	-	thousand times
TT	Data retention time	10	-	-	Year

4.2.10 **IO** input pin characteristics

Table 4-13 IO pin DC characteristics

Symbolic parameters		condition	minimum value	Typical Max.		unit
VIH input high level		VDD = 3.3 V 1.65	@without Schmitt trigger 1.75@with Schmitt trigger	-	-	V
VIL input low level		VDD = 3.3 V -0.3		-	1.60@with Schmitt trigger 1.45@without Schmitt trigger	V
Vhys Schmitt trigger voltage hysteresis VDD = 3.3 V 450				-	-	mV
Ilkg input leakage current		VIN = 3.3 V -		-	3	ÿA
RPU pull-up resistor		VIN = VSS	30	40	50	Kÿ

Symbolic parameters		condition	minimum value	Typical Max.		unit
RPD pull-down resistor		VIN = VDD	30	40	50	Kÿ
CIO	I/O pin capacitance		-	5	-	pF

4.2.11 **IO** output pin characteristics

Table 4-14 IO output voltage characteristics

Symbolic parameters	condition	minimum value	maximum value	unit
VOL output low level	VDD=3.3V IOL=-8mA	0	0.8	V
VOH output high level	VDD=3.3V IOH=8mA	2.4	3.3	
VOL output low level	VDD=3.3V IOL=-20mA	0	0.8	
VOH output high level	VDD=3.3V IOH=20mA	2.4	3.3	

Table 4-15 IO pin output AC characteristics

model (MODER bits)	Symbolic parameters	condition	minimum value	unit of maximum	
10	fmax(IO)out maximum frequency	CL = 50 pF, VDD = 2V ~ 3.6V	-	2	MHz
	tf(IO)out output high to low fall time		-	125	ns
	tr(IO)out output low to high rise time		-	125	
01	fmax(IO)out maximum frequency	CL = 50pF, VDD = 2V ~ 3.6V	-	10	MHz
	tf(IO)out output high to low fall time		-	25	ns
	tr(IO)out output low to high rise time		-	25	
11	fmax(IO)out maximum frequency	CL = 50 pF, VDD = 2.7 V ~ 3.6 V -		50	MHz
	tf(IO)out output high to low fall time CL = 50 pF, VDD = 2.7 V ~ 3.6 V -			5	ns
	tr(IO)out output low to high rise time CL = 50 pF, VDD = 2.7 V ~ 3.6 V -			5	ns

4.2.12 **NRST** reset pin characteristics

A pull-up resistor is integrated inside the NRST pin, and the peripheral application circuit may not be connected to any circuit, or an RC circuit may be connected externally.

Table 4-16 NRST pin input characteristics

symbol	parameter	minimum value	maximum value	unit
VIL	NRST reset low level voltage	-	0.8	V
VIH	NRST input high level voltage	2	-	V
Vhys	Schmitt trigger voltage	-	200	mV
Rpull	Internal weak pull-up resistor	-	50	K
T Noise	Low level is ignored	-	100	ns

4.2.13 TIM Counter Features

Table 4-17 TIM pin input characteristics

symbol	parameter	minimum value	maximum value	unit
tres(TIM)	timer resolution time	1	-	tTIMxCLK
wxya	Timer external clock frequency of CH1 to CH4	0	FTIMxCLK/2 (1)	MHz
RESTIM	Timer resolution	-	16	bit
tcounter	When the internal clock is selected, the clock period of the 16-bit counter is 1		65536	tTIMxCLK
tMAX_COUNT	maximum possible count	-	65536 x 65536 tTIMxCLK	

(1). fTIMxCLK = 32 MHz

Table 4-18 TIM2 pin input characteristics

symbol	parameter	condition	Min Typ		unit of maximum	
tres (TIM)	timer resolution time	fTIMxCLK=32MHz	-	31.2	-	ns
wxya	CH1 to CH4 of the timer, external input clock frequency	-	-	fTIMxCLK/2	-	MHz
		fTIMxCLK=32MHz	-	16	-	MHz
tMAX_COUNT	When the internal clock is selected, the clock period of the 16-bit counter	-	-	2 16	-	tTIMxCLK
		fTIMxCLK=32MHz	-	2.048	-	ms

4.2.14 ADC Characteristics

Table 4-19 ADC characteristics

project	describe	condition	minimum value	Typical Value	Maximum Unit	
VDD	ADC power supply	-	2	3.3	3.6	V
fADC	ADC clock frequency	-	0.6	-	14	MHz
f	Sampling frequency	-	0.05		1	MHz
fTRIG	External trigger frequency	fADC = 14MHz	-	-	823	kHz
		-	-		17	1/fADC
VAIN	Conversion voltage range	-	0	-	VDD	V
RAIN	External input impedance	-	-	-	50	kÿ
RADC	Sampling Switch Resistance	-	-	-	1	kÿ
CADC	Sample and hold capacitor	-	-	-	5	pF
tCAL	ADC calibration time	fADC = 14MHz	5.9			ÿs
		-	8.3			1/fADC
tlatr	Regular trigger conversion delay	fADC = 14MHz	-	-	0.143	ÿs
		-	-	-	2	1/fADC
tS	sampling time	fADC = 14 MHz	0.107	-	17.1	ÿs
		-	1.5	-	239.5	1/fADC
tSTAB	Power-on start time	-	0	0	1	ÿs
tCONV	Total conversion time (including sampling time)	fADC = 14 MHz	1	-	18	ÿs
		-	14 to 252 (ts + 12.5 for successive approximation)			1/fADC
ADC number of bits	12 bits (significant number of bits 8)	-	-			-

5 typical circuit

5.1 Power supply

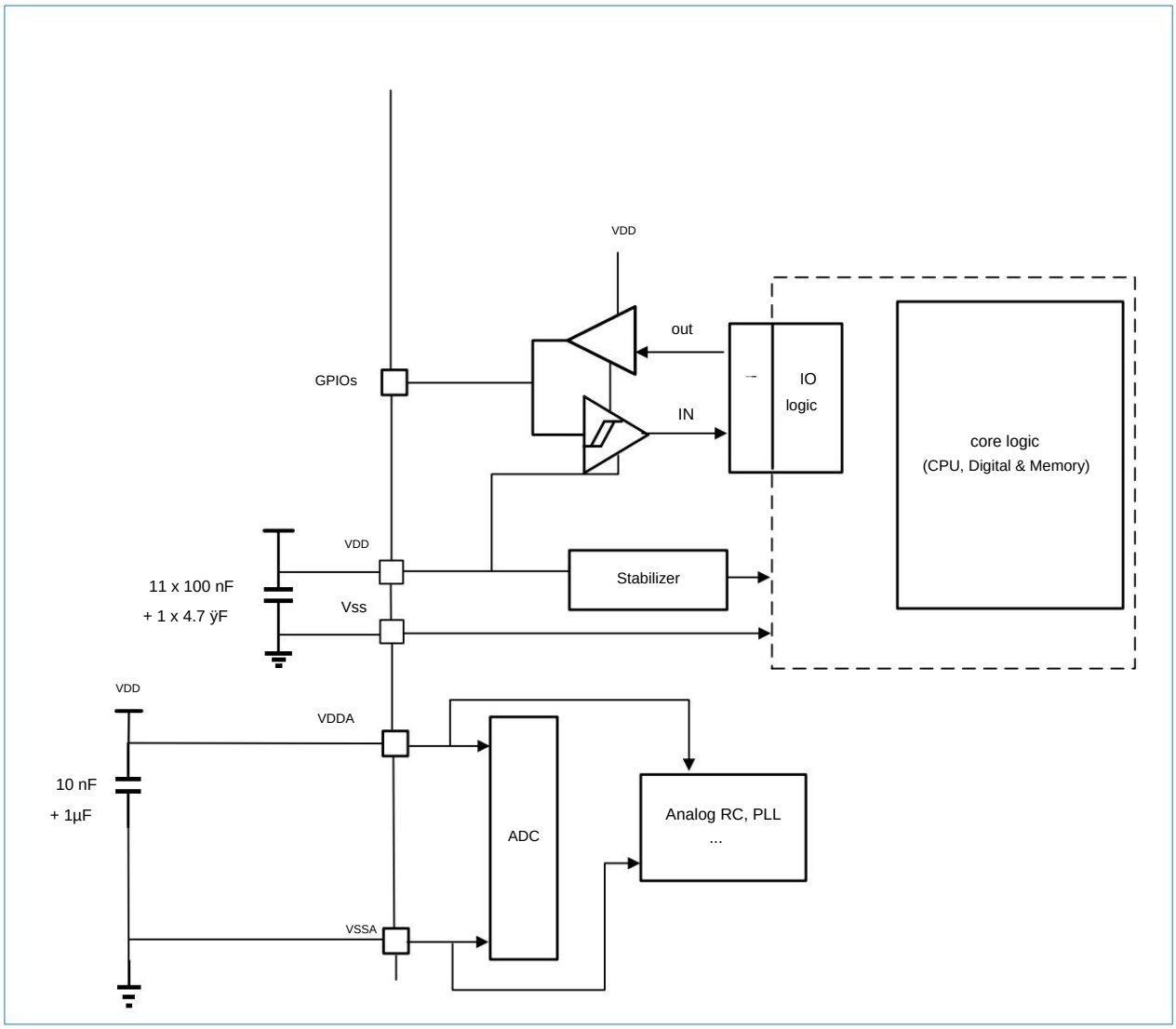

Figure 5-1 Power supply reference circuit

6 pin definition

HK32F030M MCU defines four packages: SOP8/TSSOP16/TSSOP20/QFN20, and the pins of each package are defined as follows.

6.1 SOP8 package

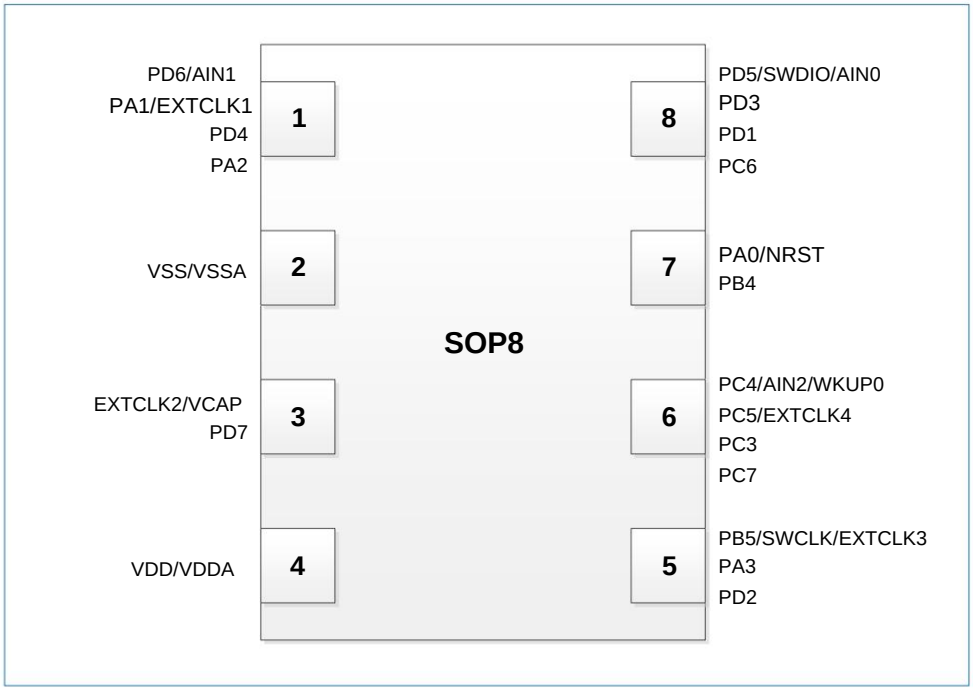

Figure 6-1 SOP8 package pin arrangement

Table 6-1 SOP8 package pin definition

pin number	pin name	Pin Type(1)	Default pin functions after power-on	Default Alternate Pin Function (AF0)
1	PD6/AIN1 (2)	I/O	PD6	-
	PA1/EXTCLK1	I/O	PA1	-
	PD4	I/O	PD4	I2C_SMBA
	PA2	I/O	PA2	I2C_SMBA
2	VSS/VSSA	S	On-chip digital ground and analog ground are connected	
3	VCAP/PD7/EXTCLK2	I/O	PD7	I2C_SMBA
4	VDD/VDDA	S	On-chip digital and analog power connections	
5	PB5/SWCLK/EXTCLK3	I/O	SWCLK	SWCLK_I2C_SDA (3)
	PA3	I/O	PA3	-
	PD2	I/O	PD2	-
6	PC4/AIN2 (2)	I/O	PC4	-
	PC5/EXTCLK4	I/O	PC5	I2C_SDA
	PC3	I/O	PC3	-
	PC7	I/O	PC7	-
7	NRST/PA0	I/O	NRST	-
	PB4	I/O	PB4	I2C_SCL
8	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
	PD3	I/O	PD3	-

pin number	pin name	Pin Type(1)	Default pin functions after power-on	Default Alternate Pin Function (AF0)
	PD1	I/O	PD1	I2C_SMBA
	PC6	I/O	PC6	I2C_SCL

(1). I means input, O means output, I/O means input/output, S means power supply.

(2). AIN0 ~ AIN2 have ADC analog input function.

(3). PB5 needs additional configuration register to select SWCLK or I2C_SDA.

6.2 TSSOP16 package

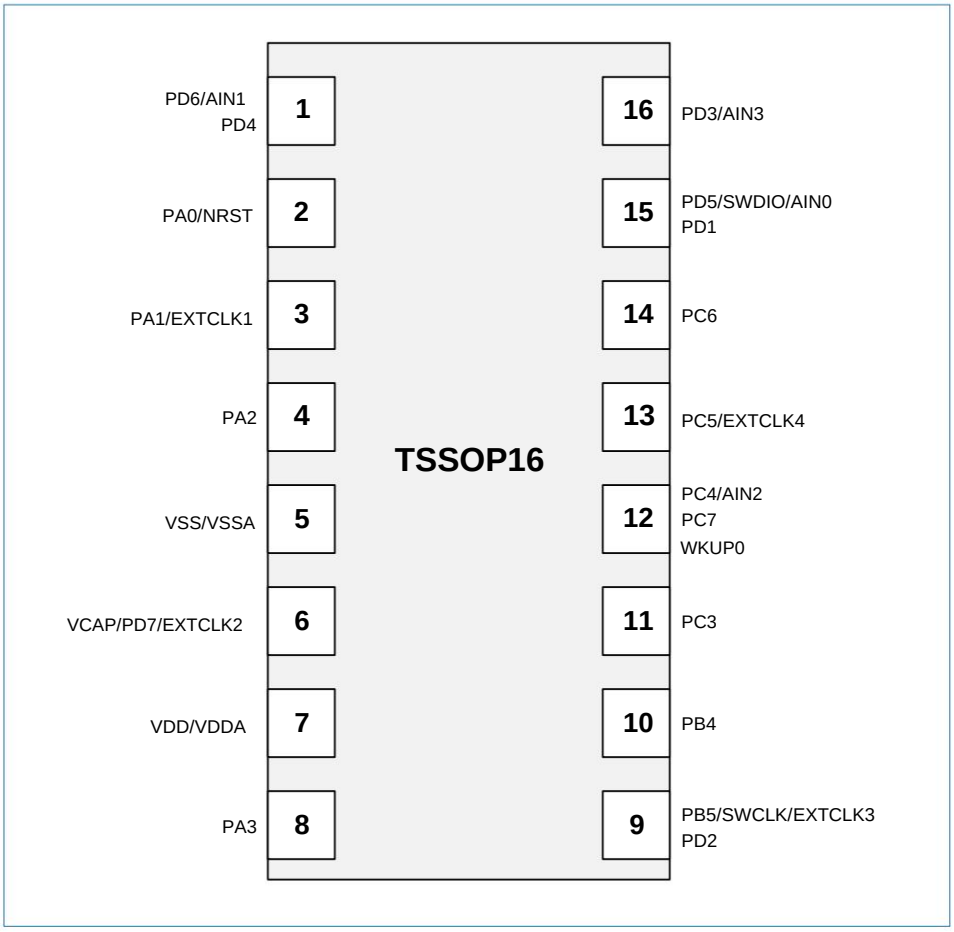

Figure 6-2 TSSOP16 package

Table 6-2 TSSOP16 package pin definition

Pin number	Pin name	Pin type (1)	Default pin function after power on	Default Alternate Pin Function (AF0)
1	PD6/AIN1 (2)	I/O	PD6	-
	PD4	I/O	PD4	I2C_SMBA
2	NRST/PA0	I/O	NRST	-
3	PA1/EXTCLK1	I/O	PA1	-
4	PA2	I/O	PA2	I2C_SMBA
5	VSS/VSSA	S	On-chip digital ground and analog ground are connected	
6	VCAP/PD7/EXTCLK2	I/O	PD7	I2C_SMBA
7	VDD/VDDA	S	On-chip digital and analog power connections	
8	PA3	I/O	PA3	-

Pin number Pin name		Pin type (1) Default pin function after power on		Default Alternate Pin Function (AF0)
9	PB5/SWCLK/EXTCLK3 I/O		SWCLK	SWCLK_I2C_SDA (3)
	PD2	I/O	PD2	-
10	PB4	I/O	PB4	I2C_SCL
11	PC3	I/O	PC3	-
12	PC4/AIN2 (2)	I/O	PC4	-
	PC7	I/O	PC7	-
13	PC5/EXTCLK4	I/O	PC5	I2C_SDA
14	PC6	I/O	PC6	I2C_SCL
15	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
	PD1	I/O	PD1	I2C_SMBA
16	PD3/AIN3 (2)	I/O	PD3	-

(1). I means input, O means output, I/O means input/output, S means power supply.

(2). AIN0 ~ AIN3 have ADC analog input function.

(3). PB5 needs additional configuration register to select SWCLK or I2C_SDA.

6.3 TSSOP20 package

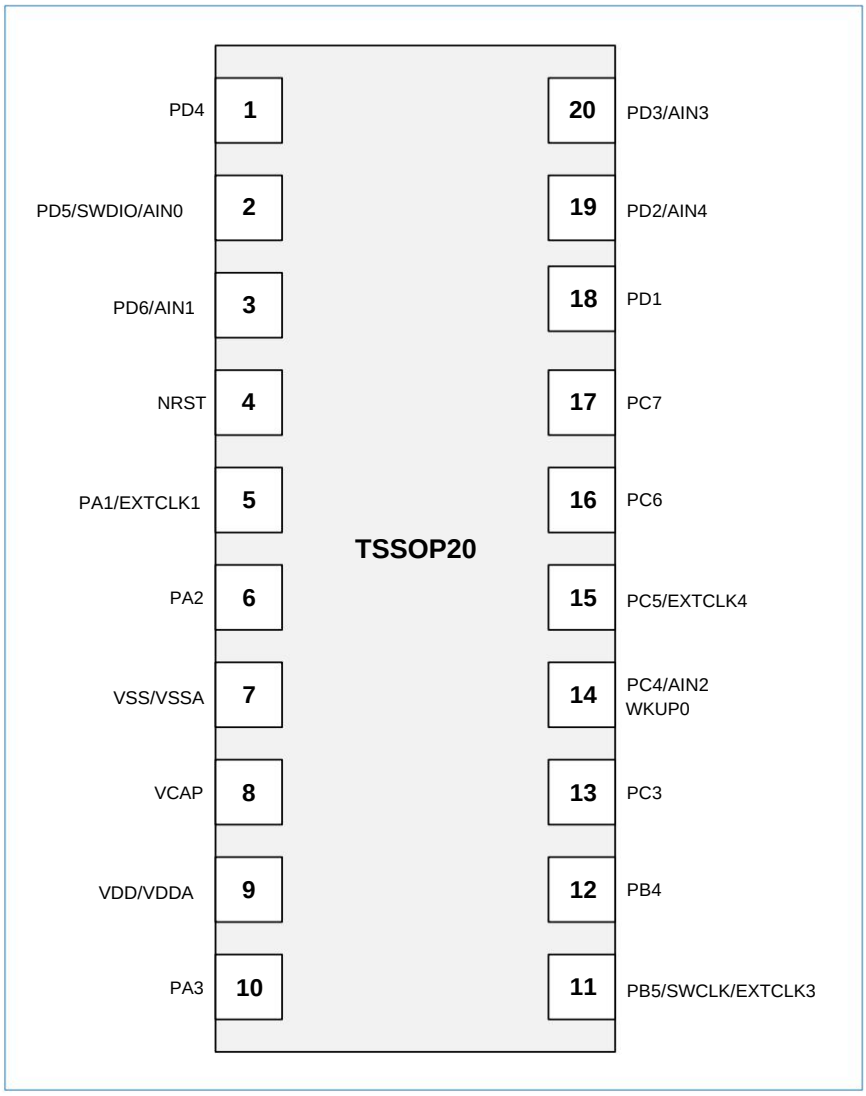

Figure 6-3 TSSOP20 package

Table 6-3 TSSOP20 package pin definition

pin number	pin name	Pin Type (1)	Default pin function after power-on	Default alternate pin function (AF0)
1	PD4	I/O	PD4	I2C_SMBA
2	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
3	PD6/AIN1	I/O	PD6	-
4	NRST	I	NRST	-
5	PA1/EXTCLK1	I/O	PA1	-
6	PA2	I/O	PA2	I2C_SMBA
7	VSS/VSSA	S	On-chip digital ground and analog ground are connected	
8	VCAP (4)	o	NC, floating	-
9	VDD/VDDA	S	On-chip digital and analog power connections	
10	PA3	I/O	PA3	-
11	PB5/SWCLK/EXTCLK3	I/O	SWCLK	SWCLK_I2C_SDA(3)
12	PB4	I/O	PB4	I2C_SCL
13	PC3	I/O	PC3	-
14	PC4/AIN2 (2)	I/O	PC4	-
15	PC5/EXTCLK4	I/O	PC5	I2C_SDA
16	PC6	I/O	PC6	I2C_SCL
17	PC7	I/O	PC7	-
18	PD1	I/O	PD1	I2C_SMBA
19	PD2/AIN4 (2)	I/O	PD2	-
20	PD3/AIN3 (2)	I/O	PD3	-

(1). I means input, O means output, I/O means input/output, S means power supply.

(2). AIN0 ~ AIN4 have ADC analog input function.

(3). PB5 needs additional configuration register to select SWCLK or I2C_SDA.

(4). TSSOP20 does not provide EXTCLK2 function.

6.4 QFN20 package

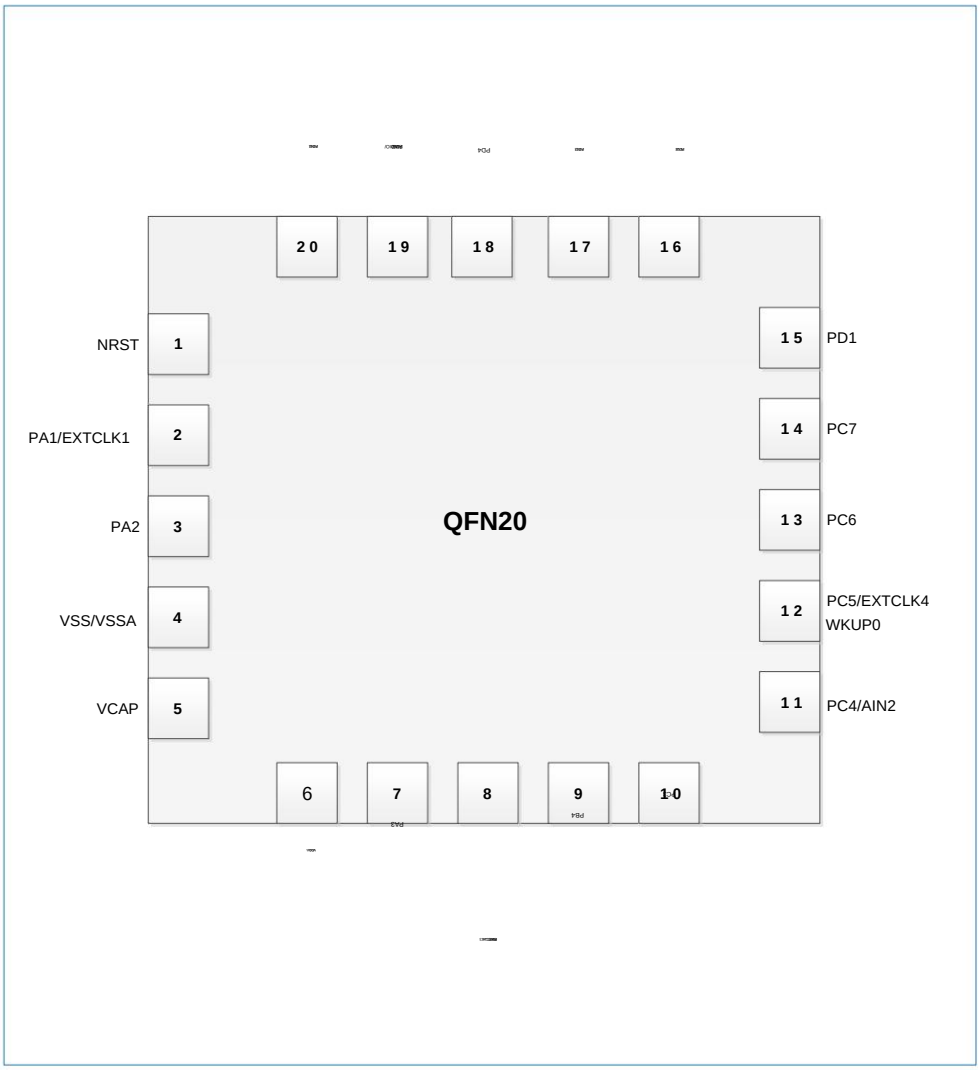

Figure 6-4 QFN20 package

Table 6-4 QFN20 package pin definition

pin number	pin name	Pin Type (1)	Default pin functions after power-on	
1	NRST	I	NRST	-
2	PA1/EXTCLK1	I/O	PA1	-
3	PA2	I/O	PA2	I2C_SMBA
4	VSS/VSSA	S	On-chip digital ground and analog ground are connected	
5	VCAP (4)	o	NC, floating	
6	VDD/VDDA	S	On-chip digital and analog power connections	
7	PA3	I/O	PA3	-
8	PB5/SWCLK/EXTCLK3	I/O	SWCLK	SWCLK_I2C_SDA (3)
9	PB4	I/O	PB4	I2C_SCL
10	PC3	I/O	PC3	-
11	PC4/AIN2 (2)	I/O	PC4	-
12	PC5/EXTCLK4	I/O	PC5	I2C_SDA
13	PC6	I/O	PC6	I2C_SCL
14	PC7	I/O	PC7	-

pin number	pin name	Pin Type (1)	Default pin functions after power-on	
15	PD1	I/O	PD1	I2C_SMBA
16	PD2/AIN4 (2)	I/O	PD2	-
17	PD3/AIN3 (2)	I/O	PD3	-
18	PD4	I/O	PD4 GPIOs	I2C_SMBA
19	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
20	PD6/AIN1 (2)	I/O	PD6 GPIOs	-

(1). I means input, O means output, I/O means input/output, S means power supply.

(2). AIN0 ~ AIN4 have ADC analog input function.

(3). PB5 needs additional configuration register to select SWCLK or I2C_SDA.

(4). QFN20 does not provide EXTCLK2 function.

6.5 Pin Alternate (AF) Function Table

Table 6-5 Pin Alternate Function Table

pin name	AF0 (I2C/SWD)	AF1 (USART)	AF2 (SPI/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6 (Beeper)	AF7 (ADC)
PA0	Reserved	Reserved	Reserved	TIM1_BKIN	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PA1	Reserved	Reserved	Reserved	TIM1_CH1N	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PA2	I2C_SMBA	Reserved	SPI_SCK/ I2S_CK	TIM1_CH2N	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PA3	Reserved	USART_TX	SPI_NSS/ I2S_WS	TIM1_CH3N	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PB4	I2C_SCL	USART_RX	SPI_MISO/ I2S_MCK	TIM1_CH2N	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PB5	SWCLK_I2C _SDA (1)	USART_RX	SPI_NSS/ I2S_WS	TIM1_BKIN	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PC3	Reserved	USART_CK	Reserved	TIM1_CH3_CH1N (2)	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC4	Reserved	Reserved	SPI_MISO/ I2S_MCK	TIM1_CH4_CH2N (2)	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PC5	I2C_SDA	Reserved	SPI_SCK/ I2S_CK	TIM1_ETR	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC6	I2C_SCL	Reserved	SPI_MOSI/ I2S_SD	TIM1_CH1	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PC7	Reserved	Reserved	SPI_MISO/ I2S_MCK	TIM1_CH2	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PD1	I2C_SMBA	USART_TX	Reserved	TIM1_CH1	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PD2	Reserved	Reserved	SPI_MOSI/ I2S_SD	TIM1_CH2	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PD3	Reserved	Reserved	SPI_SCK/ I2S_CK	TIM1_CH3	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PD4	I2C_SMBA	USART_CK	SPI_MOSI/ I2S_SD	TIM1_CH4	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PD5	SWDIO	USART_TX	Reserved	TIM1_ETR	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR

pin name	AF0 (I2C/SWD)	AF1 (USART)	AF2 (SPI/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6 (Beeper)	AF7 (ADC)
PD6 Reserved		USART_RX	SPI_MISO/ I2S_MCK	TIM1_CH2	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PD7 I2C_SMBA		USART_RX	SPI_NSS/ I2S_WS	TIM1_CH3	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR

(1). PB5 needs the following IOMUX peripheral register configuration to select SWCLK or I2C_SDA.

(2). PC3 and PC4 need the following IOMUX peripheral register configuration to select CH3/CH4 or CH1N/CH2N of TIM1.

bit	2	1	0
	PB5_I2C1_SEL	**PC4_TIM1_SEL**	**PC3_TIM1_SEL**
access	rw	rw	rw
reset value	0	0	0

Figure 6-5 Multiplexing function selection of PB5/PC4/PC3

• If PB5_AF is configured as AF0, when the value of PB5_I2C_SEL is:

ÿ 0: PB5 acts as SWCLK input pin (set for system reset).

ÿ 1: PB5 is used as the SDA pin of I2C.

• If PC4_AF is configured as AF3, when the value of PC4_TIM1_SEL is:

ÿ 0: PC3 is used as CH4 pin of TIM1.

ÿ 1: PC3 acts as the CH2N pin of TIM1.

• If PC3_AF is configured as AF3, when the value of PC3_TIM1_SEL is: ÿ 0:

PC3 acts as the CH3 pin of TIM1.

ÿ 1: PC3 acts as the CH1N pin of TIM1.

6.6 IOMUX pin function multiple mapping

TSSOP16/SOP8 package products can realize the mapping of a single pin to multiple GPIOs or peripheral IOs through the IOMUX pin function multiple mapping controller.

The following takes pin 8 in Figure 6-1 as an example to illustrate pin multiple mapping.

Table 6-6 Pin 8 function mapping of SOP8 package

operate	The function of the 8th pin of the SOP8 package chip
chip reset	Corresponding peripheral IO in PD5 and SYSCFG configuration
Configure IOMUX registers	• PD3 and corresponding peripheral IO in SYSCFG configuration • PD1 and corresponding peripheral IO in SYSCFG configuration • PC6 and corresponding peripheral IO in SYSCFG configuration

Through IOMUX configuration, SOP8 package products can flexibly use GPIO resources and all peripheral IO functions on-chip.

7 Package parameters

7.1 Package size

7.1.1 SOP8 package

The SOP8 is a 4.9 mm x 6 mm, 1.27 mm pitch package.

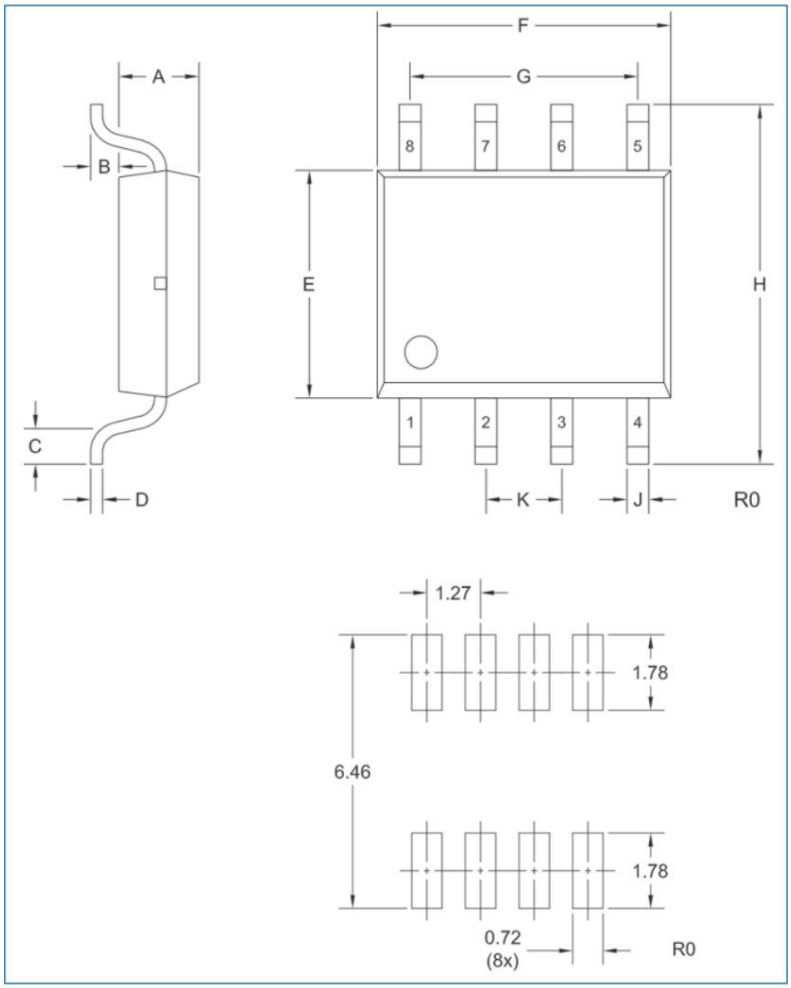

Figure 7-1 SOP8 Package Dimensions

Table 7-1 SOP8 Package Size Parameters

symbol	Unit: mm		Unit: inches(1)	
	minimum value	maximum value	minimum value	maximum value
A	1.24	1.44	0.049	0.057
B	0.00	0.27	0.000	0.011
C	0.46	-	0.018	-
D.	0.16	0.27	0.006	0.011
E.	3.70	3.90	0.145	0.154
f	4.81	5.01	0.189	0.198
G	3.81		0.150	
h	5.88	6.18	0.231	0.244
J	0.35	0.52	0.013	0.021
K	1.27		0.050	

7.1.2 **TSSOP16** package

The TSSOP16 is a 5.0 mm x 4.4 mm, 0.65 mm pitch package.

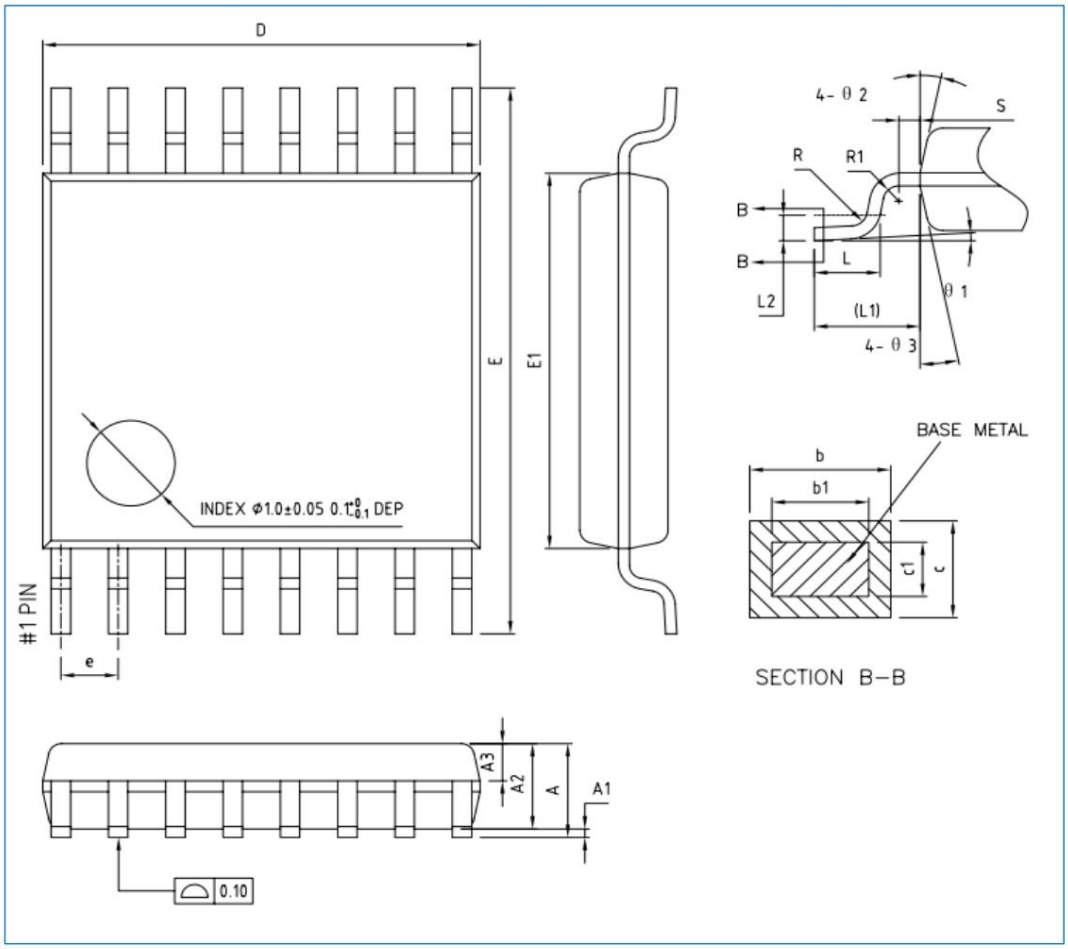

Figure 7-2 TSSOP16 package size

Table 7-2 TSSOP16 Package Size Parameters

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
b1	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	0.13	0.15
D.	4.86	4.96	5.06
E.	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
ÿ1	0°	-	8°
ÿ2	10°	12°	14°
ÿ3	10°	12°	14°

7.1.3 TSSOP20 package

The TSSOP20 is a 6.5 mm x 4.4 mm, 0.65 mm package.

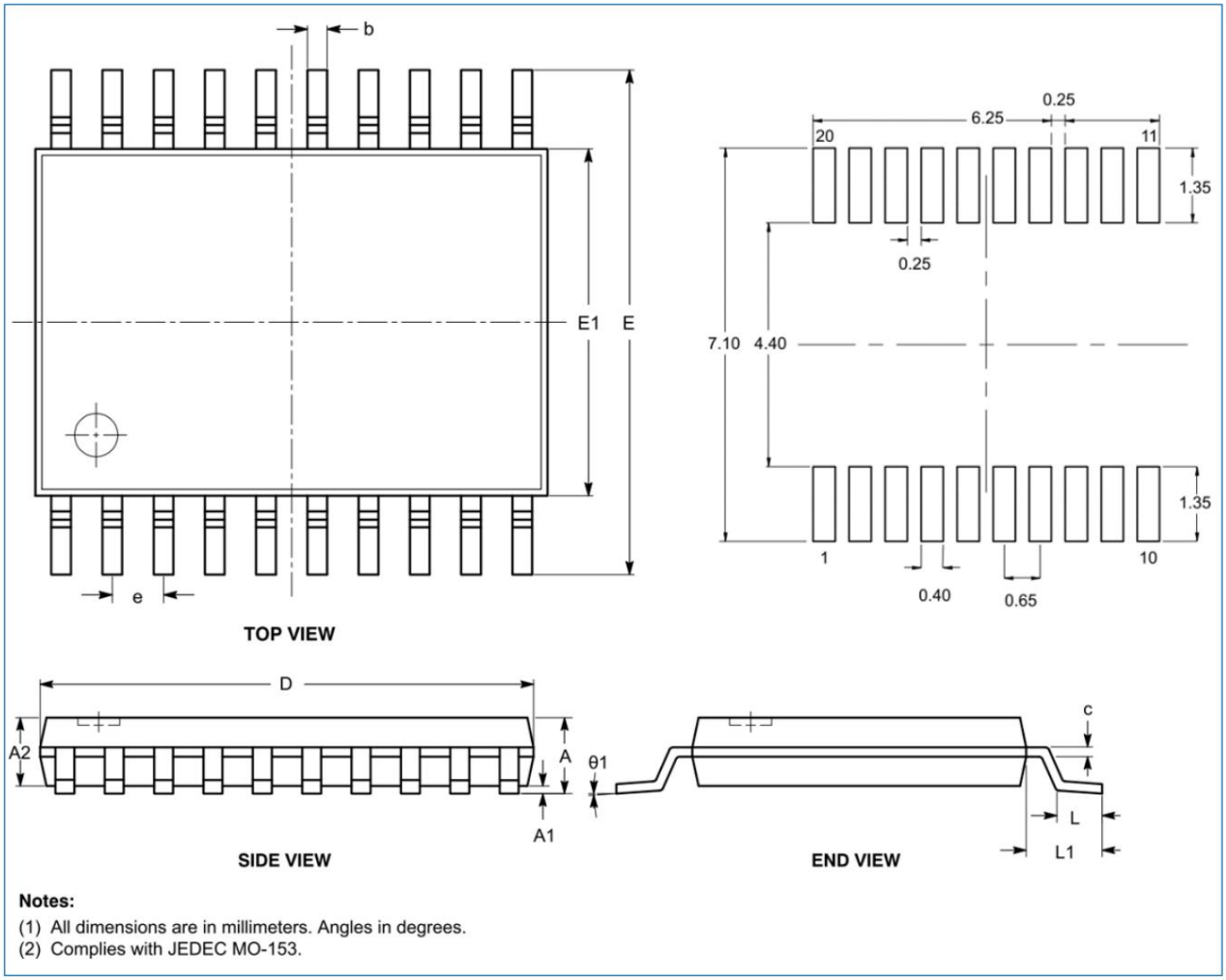

Figure 7-3 TSSOP20 package size

Table 7-3 TSSOP20 Package Size Parameters

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D.	6.40	6.50	6.60

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
E.	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
ÿ	0°	-	8°

7.1.4 QFN20 package

The QFN20 is available in two package sizes. A 3 mm x 3 mm, 0.4 mm pitch package (as shown in Figure 7-4), the corresponding model is HK32F030MF4N6; the other package is 4 mm x 4 mm, 0.5 mm pitch (as shown in Figure 7-5), and the corresponding model is HK32F030MF4U6.

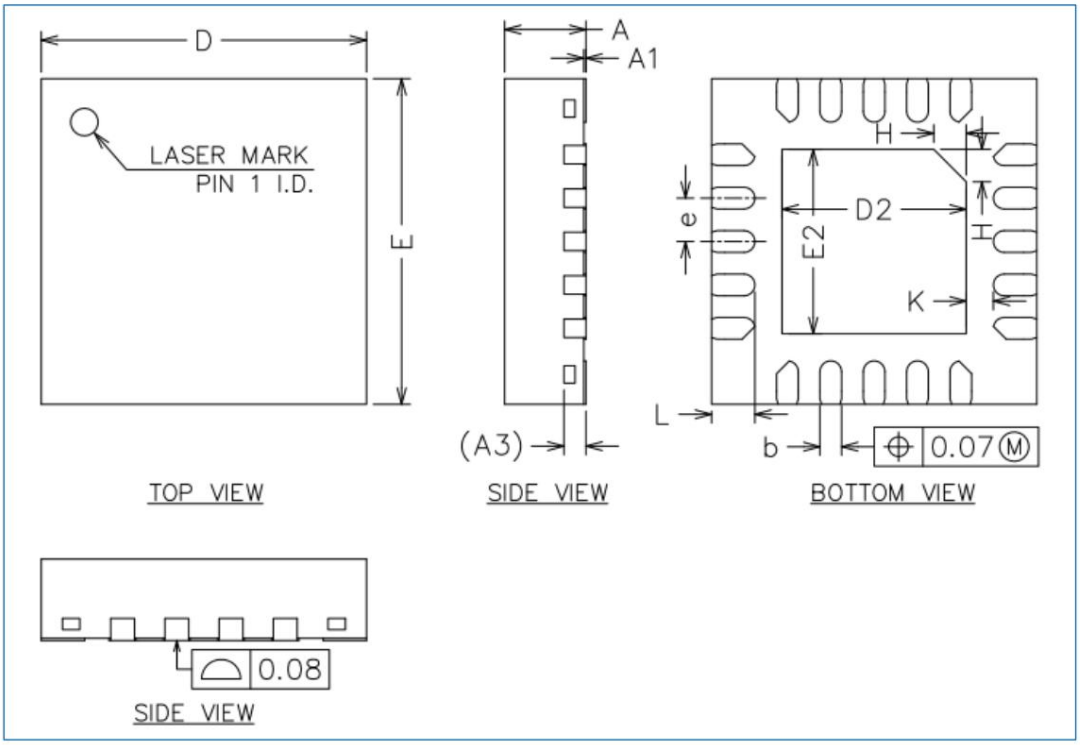

Figure 7-4 QFN20 package size 1

Table 7-4 Parameters of QFN20 package size 1

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D.	2.95	3.00	3.05
E.	2.95	3.00	3.05
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75
e	0.30	0.40	0.50
h	0.30 REF		
K	0.15	-	-

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
L	0.35	0.40	0.45

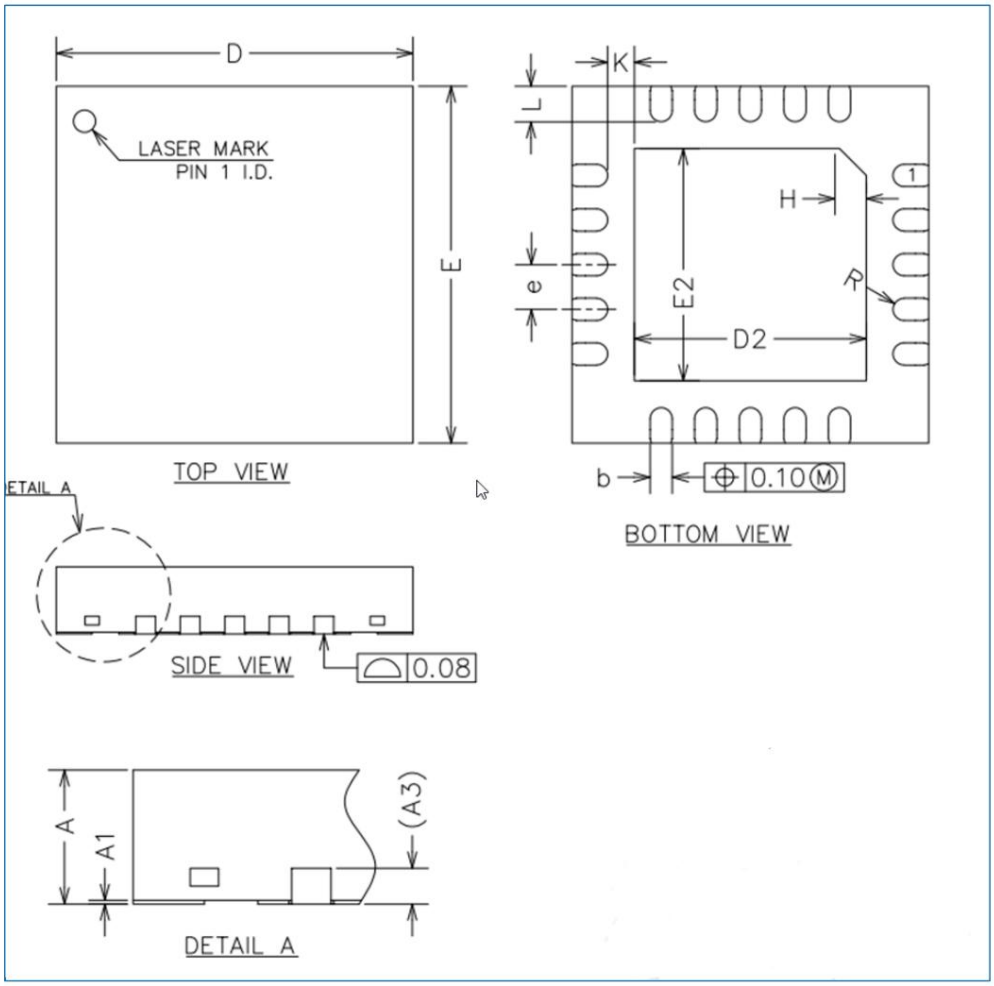

Figure 7-5 QFN20 package size 2

Table 7-5 Parameters of QFN20 package size 2

symbol	Minimum value (mm)	Typical value (mm)	Maximum value (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D.	3.90	4.00	4.10
E.	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
h	0.30 REF		
K	0.20	-	-
L	0.35	0.40	0.45
R	0.10	-	-

7.2 Silkscreen Information

The silk screen information includes Hangshun LOGO+ARM LOGO, product model and product batch number. Among them, the description of the product batch number is shown in the table below.

Table 7-6 Description of product batch number

Serial Number	illustrate
1st character	Represents the year, for example, 1 represents 21 years
2nd and 3rd characters	On behalf of packaging plant
4th and 5th characters	Represents a cycle, for example, 18 represents a cycle
The 6th, 7th and 8th characters represent the	last three digits of the wafer lot number

7.2.1 SOP8 Silkscreen

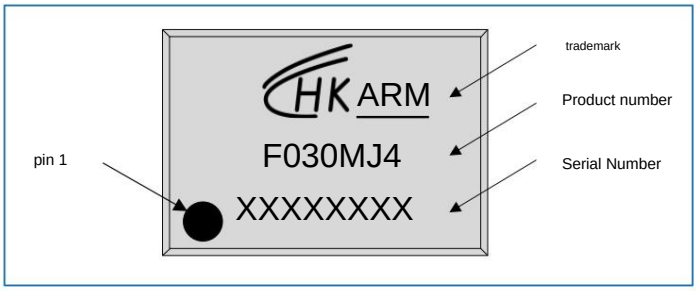

Figure 7-6 SOP8 HK32F030MJ4M6 silk screen example

7.2.2 TSSOP16 silkscreen

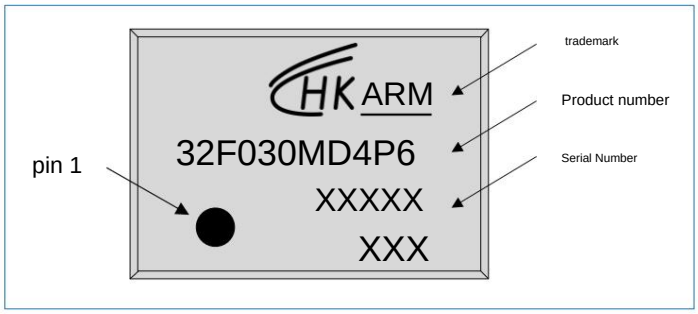

Figure 7-7 Silkscreen example of TSSOP16 HK32F030MD4P6

7.2.3 TSSOP20 silkscreen

Figure 7-8 TSSOP20 HK32F030MF4P6 silk screen example

7.2.4 QFN20 silkscreen

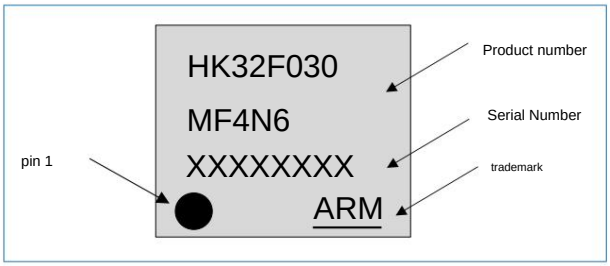

Figure 7-9 Silkscreen example of QFN20 HK32F030MF4N6

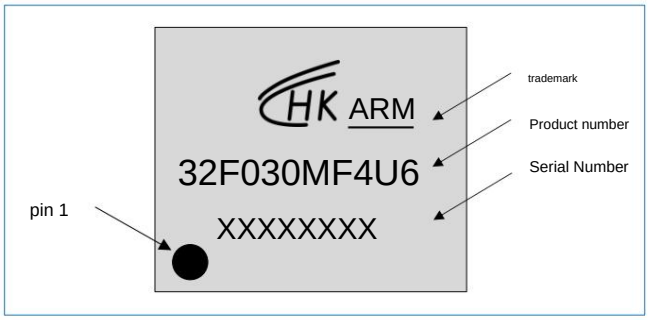

Figure 7-10 QFN20 HK32F030MF4U6 silk screen example

8 ordering information

8.1 Order code

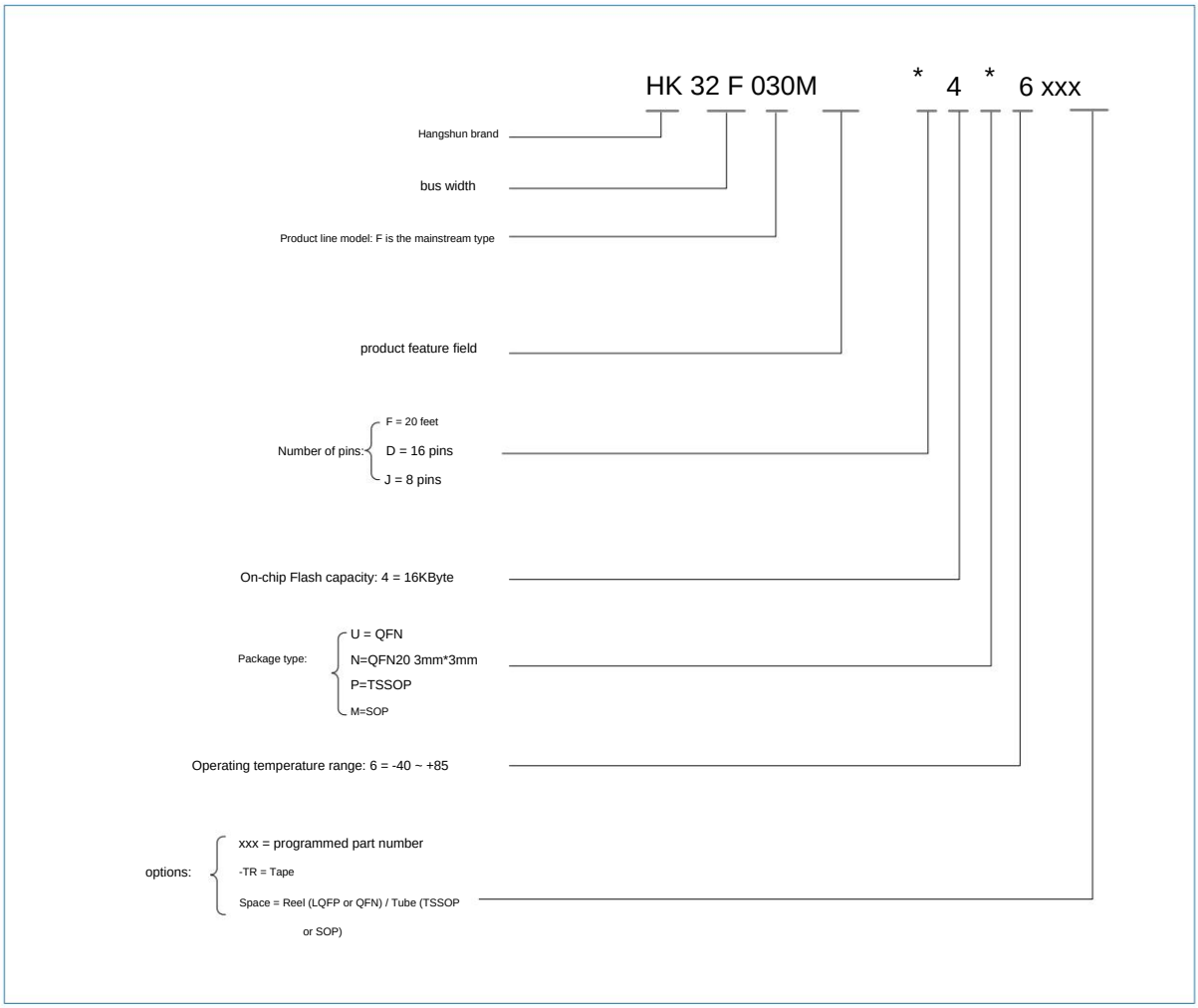

Figure 8-1 Order code

8.2 Order packaging

Table 8-1 Product order packaging

encapsulation	specific model	Package	Remark
SOP8	HK32F030MJ4M6	Tube	
SOP8	HK32F030MJ4M6-TR	taping	
TSSOP16	HK32F030MD4P6	Tube	
TSSOP16	HK32F030MD4P6-TR	taping	
TSSOP20	HK32F030MF4P6	Tube	
TSSOP20	HK32F030MF4P6-TR	taping	
QFN20	HK32F030MF4N6	Plate	Package size: 3 mm x 3 mm, 0.4 mm pitch
QFN20	HK32F030MF4N6-TR	taping	
QFN20	HK32F030MF4U6	Plate	Package size: 4 mm x 4 mm, 0.5 mm pitch
QFN20	HK32F030MF4U6-TR	taping	

9 Abbreviations

abbreviation	full name	Chinese description
ADC	Analog-to-Digital Converter	Analog to Digital Converter
AHB	Advanced High-Performance Bus	Advanced High Performance Bus
APB	Advanced Peripheral Bus	peripheral bus
AWU	Auto-Wakeup	auto wake up
CRC	Cyclic Redundancy Check	Cyclic Redundancy Check Code
CSS	Clock Security System	clock security system
DMA	Direct Memory Access	direct memory access
EEPROM	Electrically Erasable Programmable Read Only Memory	EEPROM
EXTI	Extended Interrupts and Events Controller	Interrupt and Event Controller
GPIOs	General Purpose Input Output	GPIO
I2C	Inter-Integrated Circuit	I2C bus
I2S	Inter-IC Sound	I2S bus
IWDG	Independent Watchdog	independent watchdog
LSI	Low-Speed InternalÿClock Signalÿ	Low-speed internal (clock signal)
MCU	Microcontroller Unit	micro control unit
MSPS	Million Samples Per Second	million samples per second
NVIC	Nested Vectored Interrupt Controller	Nested Vectored Interrupt Controller
PDR	Power-Down Reset	Brownout reset
PLLs	Phase Locked Loop	PLL
POR	Power-On Reset	power on reset
PWM	Pulse Width Modulation	pulse width modulation
RCC	Reset and Clock Control	Reset Clock Control
RISC	Reduced Instruction Set Computing	RISC
SPI	Serial Peripheral Interface	Serial Peripheral Interface
SRAM	Static Random Access Memory	SRAM
SWD	Serial Wire Debug	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter	Universal Synchronous/Asynchronous Transceiver
WWDG	Window Watchdog	window watchdog

10 important tips


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