PIC32MX3XX/4XX
Data Sheet

High-Performance, General Purpose and USB 32-bit Flash Microcontrollers

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PIC32MX3XX/4XX

High-Performance, General Purpose and USB 32-bit Flash Microcontrollers

High-Performance 32-bit RISC CPU:

- MIPS32® M4K® 32-bit core with 5-stage pipeline
- 80 MHz maximum frequency
- 1.56 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state Flash access
- Single-cycle multiply and high-performance divide unit
- MIPS16e® mode for up to 40% smaller code size
- Two sets of 32 core register files (32-bit) to reduce interrupt latency
- Prefetch Cache module to speed execution from Flash

Microcontroller Features:

- Operating voltage range of 2.3V to 3.6V
- 32K to 512K Flash memory (plus an additional 12 KB of boot Flash)
- 8K to 32K SRAM memory
- Pin-compatible with most PIC24/dsPIC® DSC devices
- Multiple power management modes
- Multiple interrupt vectors with individually programmable priority
- Fail-Safe Clock Monitor Mode
- Configurable Watchdog Timer with on-chip Low-Power RC Oscillator for reliable operation

Peripheral Features:

- Atomic SET, CLEAR and INVERT operation on select peripheral registers
- Up to 4-channel hardware DMA with automatic data size detection
- USB 2.0-compliant full-speed device and On-The-Go (OTG) controller
- USB has a dedicated DMA channel
- 3 MHz to 25 MHz crystal oscillator
- Internal 8 MHz and 32 kHz oscillators
- Separate PLLs for CPU and USB clocks
- Two I^2C™ modules
- Two UART modules with:
  - RS-232, RS-485 and LIN 1.2 support
  - IrDA® with on-chip hardware encoder and decoder
- Parallel Master and Slave Port (PMP/PSP) with 8-bit and 16-bit data and up to 16 address lines
- Hardware Real-Time Clock and Calendar (RTCC)
- Five 16-bit Timers/Counters (two 16-bit pairs combine to create two 32-bit timers)
- Five capture inputs
- Five compare/PWM outputs
- Five external interrupt pins
- High-Speed I/O pins capable of toggling at up to 80 MHz
- High-current sink/source (18 mA/18 mA) on all I/O pins
- Configurable open-drain output on digital I/O pins

Debug Features:

- Two programming and debugging Interfaces:
  - 2-wire interface with unintrusive access and real-time data exchange with application
  - 4-wire MIPS® standard enhanced JTAG interface
- Unintrusive hardware-based instruction trace
- IEEE Standard 1149.2-compatible (JTAG) boundary scan

Analog Features:

- Up to 16-channel 10-bit Analog-to-Digital Converter:
  - 1000 ksps conversion rate
  - Conversion available during Sleep, Idle
- Two Analog Comparators
- 5V tolerant input pins (digital pins only)

TABLE 1: PIC32MX GENERAL PURPOSE – FEATURES

General Purpose														
Device	Pins	Packages(2)	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	VREG	Trace	EUART/SPI/I²C™	10-bit A/D (ch)	Comparators	PMP/PSP	JTAG
PIC32MX320F032H	64	PT, MR	40	32 + 12(1)	8	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F064H	64	PT, MR	80	64 + 12(1)	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128H	64	PT, MR	80	128 + 12(1)	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F128H	64	PT, MR	80	128 + 12(1)	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F256H	64	PT, MR	80	256 + 12(1)	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F512H	64	PT, MR	80	512 + 12(1)	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128L	100	PT	80	128 + 12(1)	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX340F128L	100	PT	80	128 + 12(1)	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F256L	100	PT	80	256 + 12(1)	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F512L	100	PT	80	512 + 12(1)	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												

Legend: PT = TQFP MR = QFN BG = XBGA

Note 1: This device features 12 KB Boot Flash memory.

2: See Legend for an explanation of the acronyms. See **Section 30.0 "Packaging Information"** for details.

TABLE 2: PIC32MX USB – FEATURES

USB															
Device	Pins	Packages(2)	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	Dedicated USB DMA Channels	VREG	Trace	EUART/SPI/I²C™	10-bit A/D (ch)	Comparators	PMP/PSP	JTAG
PIC32MX420F032H	64	PT, MR	40	32 + 12(1)	8	5/5/5	0	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F128H	64	PT, MR	80	128 + 12(1)	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F256H	64	PT, MR	80	256 + 12(1)	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F512H	64	PT, MR	80	512 + 12(1)	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F128L	100	PT	80	128 + 12(1)	32	5/5/5	4	2	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG													
PIC32MX460F256L	100	PT	80	256 + 12(1)	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG													
PIC32MX460F512L	100	PT	80	512 + 12(1)	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG													

Legend: PT = TQFP MR = QFN BG = XBGA

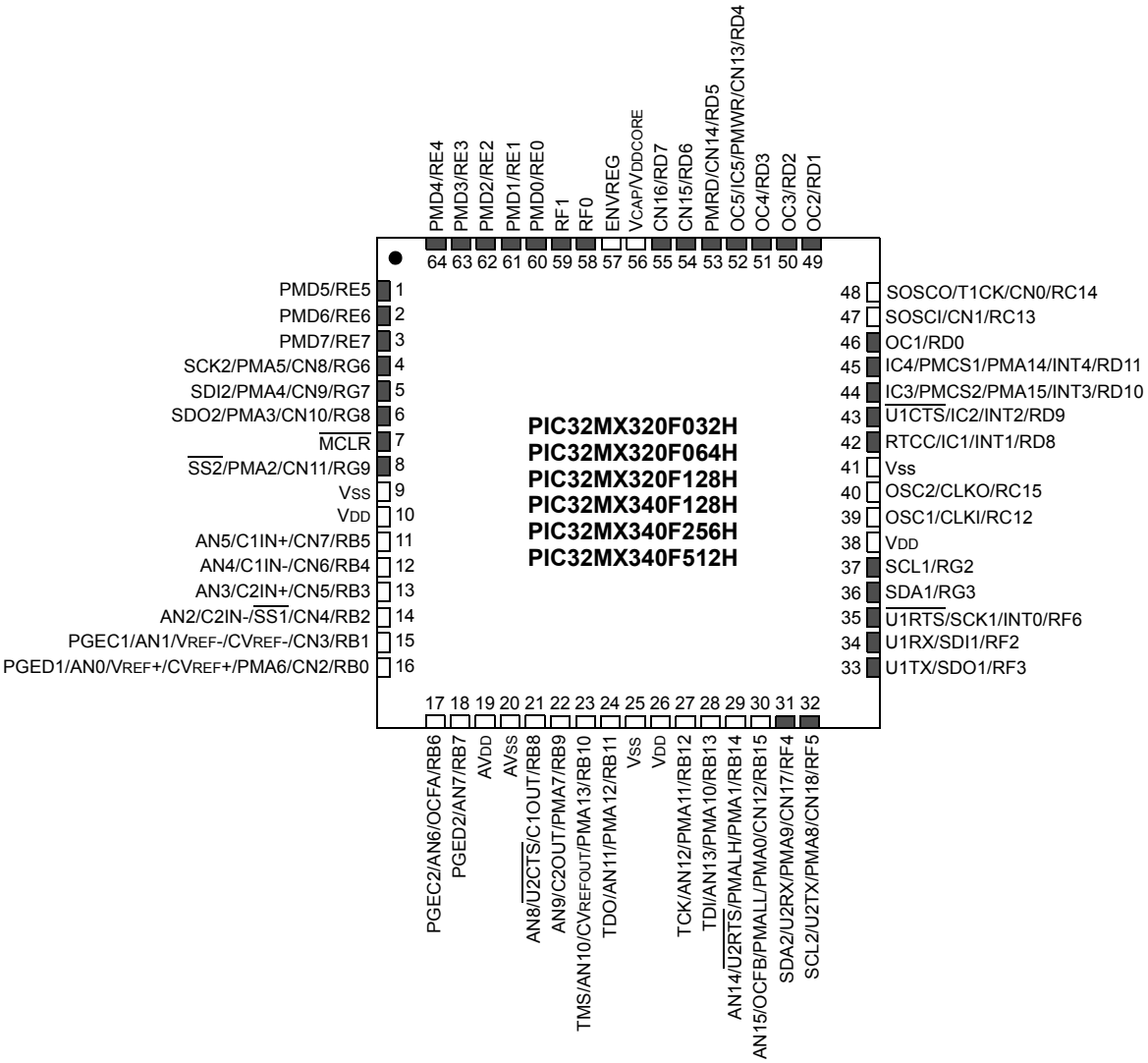
Note 1: This device features 12 KB Boot Flash memory.

2: See Legend for an explanation of the acronyms. See **Section 30.0 "Packaging Information"** for details.

Pin Diagrams

64-Pin QFN (General Purpose)

■ = Pins are up to 5V tolerant

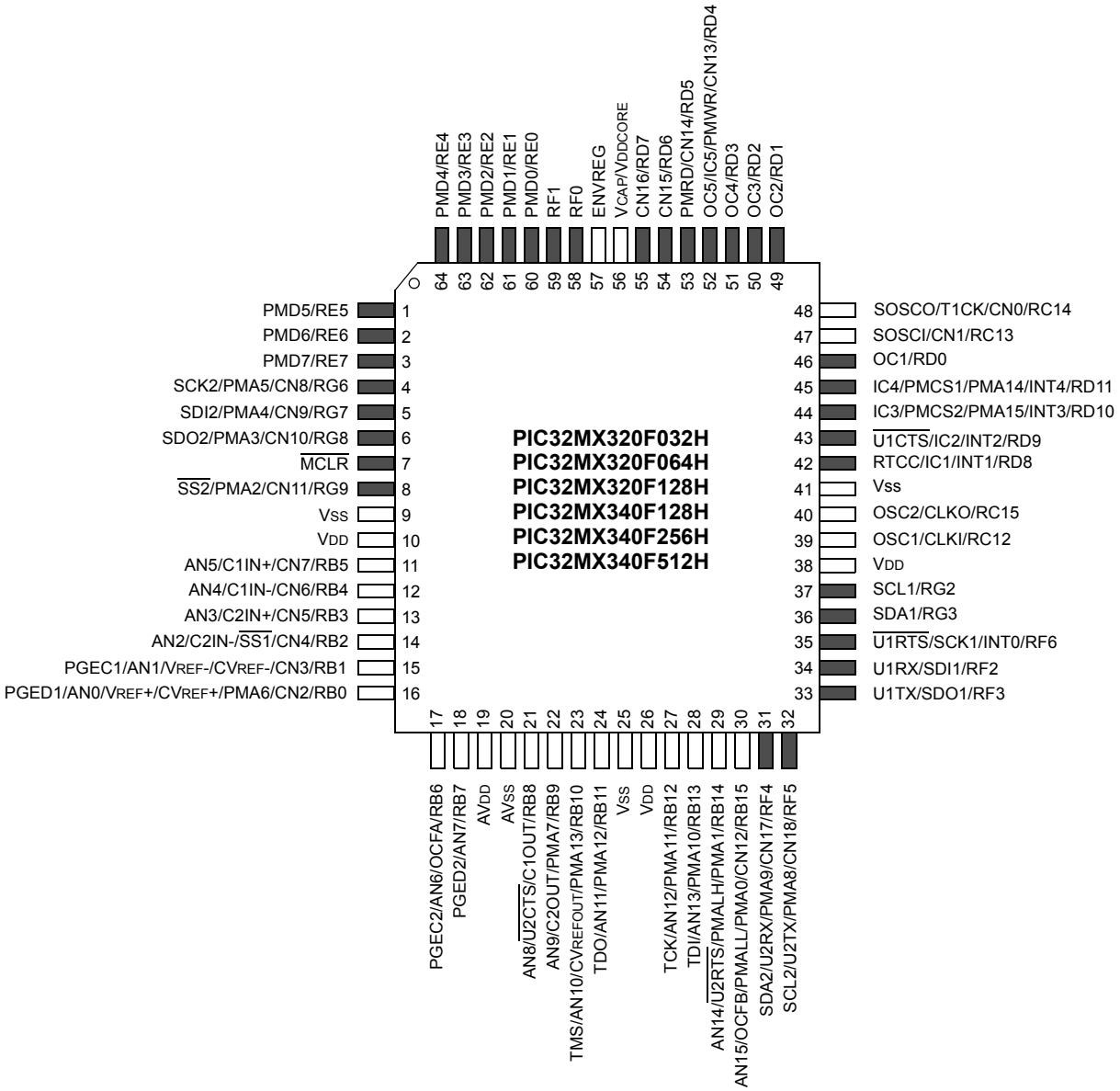


Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

64-Pin TQFP (General Purpose)

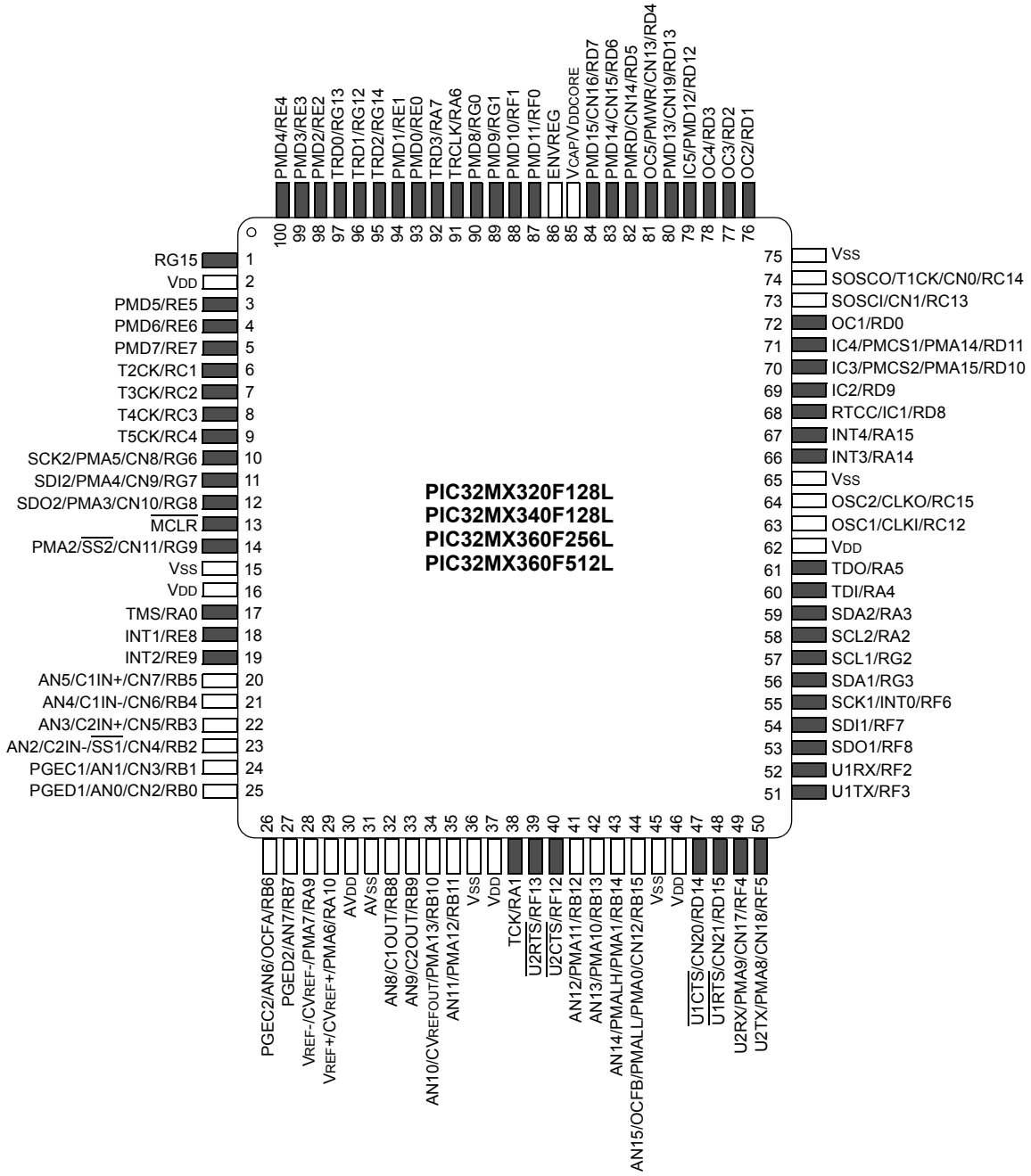
= Pins are up to 5V tolerant



Pin Diagrams (Continued)

100-Pin TQFP (General Purpose)

= Pins are up to 5V tolerant



Pin Diagrams (Continued)

121-Pin XBGA(1)

● = Pins are up to 5V tolerant

PIC32MX320F128L
PIC32MX340F128L
PIC32MX360F256L
PIC32MX360F512L

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	ENVREG	VSS	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP/ VDDCORE	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	VDD	RC13	RD11
D	RC1	RE7	RE5	VSS	VSS	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	VDD	RG1	VSS	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	VSS	VDD	NC	VDD	NC	RF7	RF6	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 3 for full pin names.

TABLE 3: PIN NAMES: PIC32MX320F128L, PIC32MX340F128L, AND PIC32MX360F128L, AND PIC32MX360F512L DEVICES

Pin Number	Full Pin Name
A1	PMD4/RE4
A2	PMD3/RE3
A3	TRD0/RG13
A4	PMD0/RE0
A5	PMD8/RG0
A6	PMD10/RF1
A7	ENVREG
A8	VSS
A9	IC5/PMD12/RD12
A10	OC3/RD2
A11	OC2/RD1
B1	No Connect (NC)
B2	RG15
B3	PMD2/RE2
B4	PMD1/RE1
B5	TRD3/RA7
B6	PMD11/RF0
B7	VCAP/VDDCORE
B8	PMRD/CN14/RD5
B9	OC4/RD3
B10	VSS
B11	SOSCO/T1CK/CN0/RC14
C1	PMD6/RE6
C2	VDD
C3	TRD1/RG12
C4	TRD2/RG14
C5	TRCLK/RA6
C6	No Connect (NC)
C7	PMD15/CN16/RD7
C8	OC5/PMWR/CN13/RD4
C9	VDD
C10	SOSCI/CN1/RC13
C11	IC4/PMCS1/PMA14/RD11
D1	T2CK/RC1
D2	PMD7/RE7
D3	PMD5/RE5
D4	VSS
D5	VSS
D6	No Connect (NC)
D7	PMD14/CN15/RD6
D8	PMD13/CN19/RD13
D9	OC1/RD0
D10	No Connect (NC)
D11	IC3/PMCS2/PMA15/RD10
E1	T5CK/RC4
E2	T4CK/RC3
E3	SCK2/PMA5/CN8/RG6
E4	T3CK/RC2
E5	VDD
E6	PMD9/RG1

Pin Number	Full Pin Name
E8	INT4/RA15
E9	RTCC/IC1/RD8
E10	IC2/RD9
E11	INT3/RA14
F1	$\overline{\text{MCLR}}$
F2	SDO2/PMA3/CN10/RG8
F3	$\overline{\text{SS2}}$/PMA2/CN11/RG9
F4	SDI2/PMA4/CN9/RG7
F5	VSS
F6	No Connect (NC)
F7	No Connect (NC)
F8	VDD
F9	OSC1/CLKI/RC12
F10	VSS
F11	OSC2/CLKO/RC15
G1	INT1/RE8
G2	INT2/RE9
G3	TMS/RA0
G4	No Connect (NC)
G5	VDD
G6	VSS
G7	VSS
G8	No Connect (NC)
G9	TDO/RA5
G10	SDA2/RA3
G11	TDI/RA4
H1	AN5/C1IN+/CN7/RB5
H2	AN4/C1IN-/CN6/RB4
H3	VSS
H4	VDD
H5	No Connect (NC)
H6	VDD
H7	No Connect (NC)
H8	SDI1/RF7
H9	SCK1/INT0/RF6
H10	SCL1/RG2
H11	SCL2/RA2
J1	AN3/C2IN+/CN5/RB3
J2	AN2/C2IN-/$\overline{\text{SS1}}$/CN4/RB2
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/PMA12/RB11
J6	TCK/RA1
J7	AN12/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	SDO1/RF8
J11	SDA1/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0

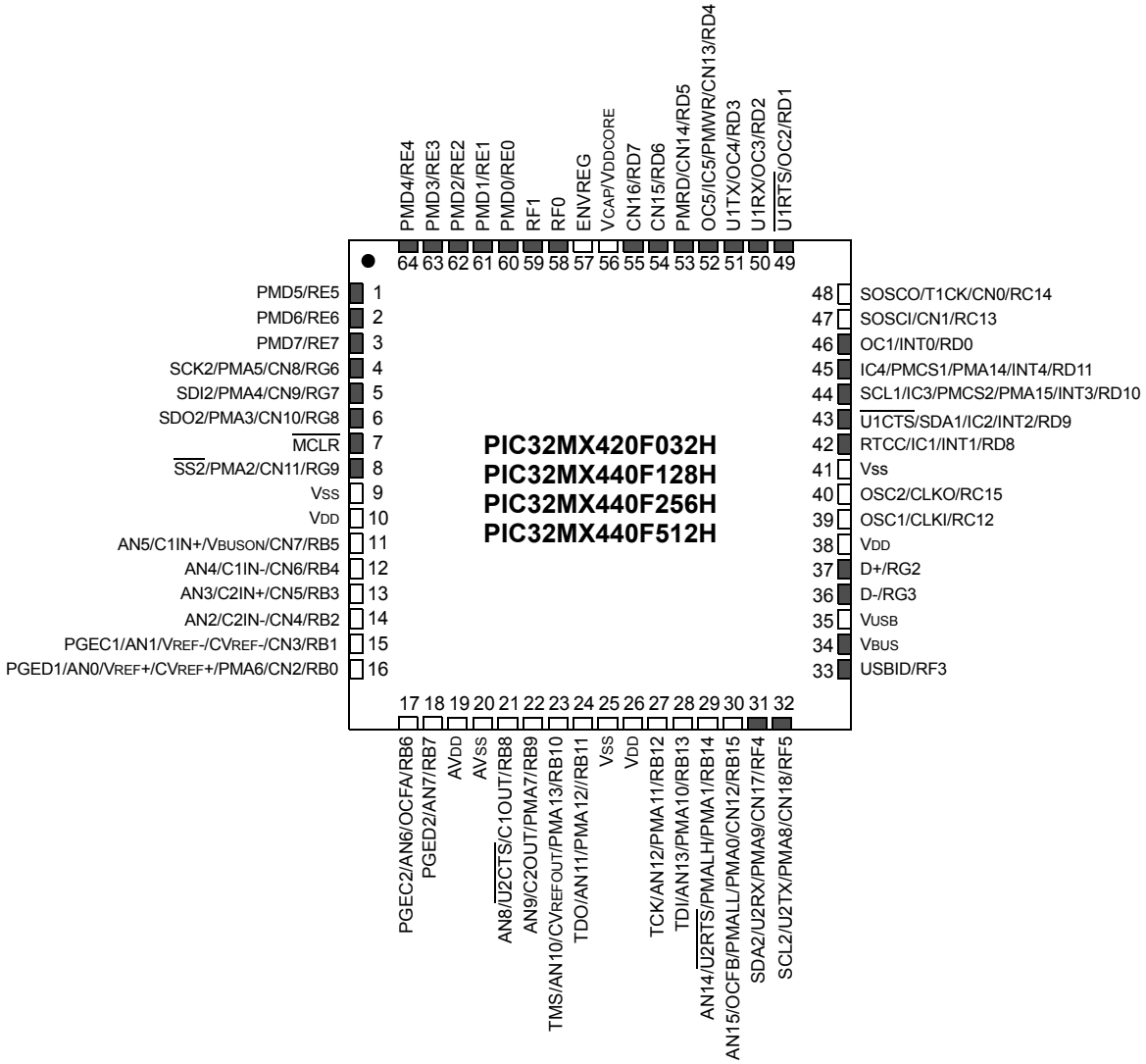
TABLE 3: PIN NAMES: PIC32MX320F128L, PIC32MX340F128L, AND PIC32MX360F128L, AND PIC32MX360F512L DEVICES (CONTINUED)

Pin Number	Full Pin Name
E7	VSS
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	U2CTS/RF12
K7	AN14/PMALH/PMA1/RB14
K8	VDD
K9	U1RTS/CN21/RD15
K10	U1TX/RF3
K11	U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/PMA7/RA9
K3	VREF+/CVREF+/PMA6/RA10
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	U2RTS/RF13
L7	AN13/PMA10/RB13
L8	AN15/OCFB/PMALL/PMA0/CN12/RB15
L9	CN20/U1CTS/RD14
L10	U2RX/PMA9/CN17/RF4
L11	U2TX/PMA8/CN18/RF5

Pin Diagrams (Continued)

64-Pin QFN (USB)

■ = Pins are up to 5V tolerant

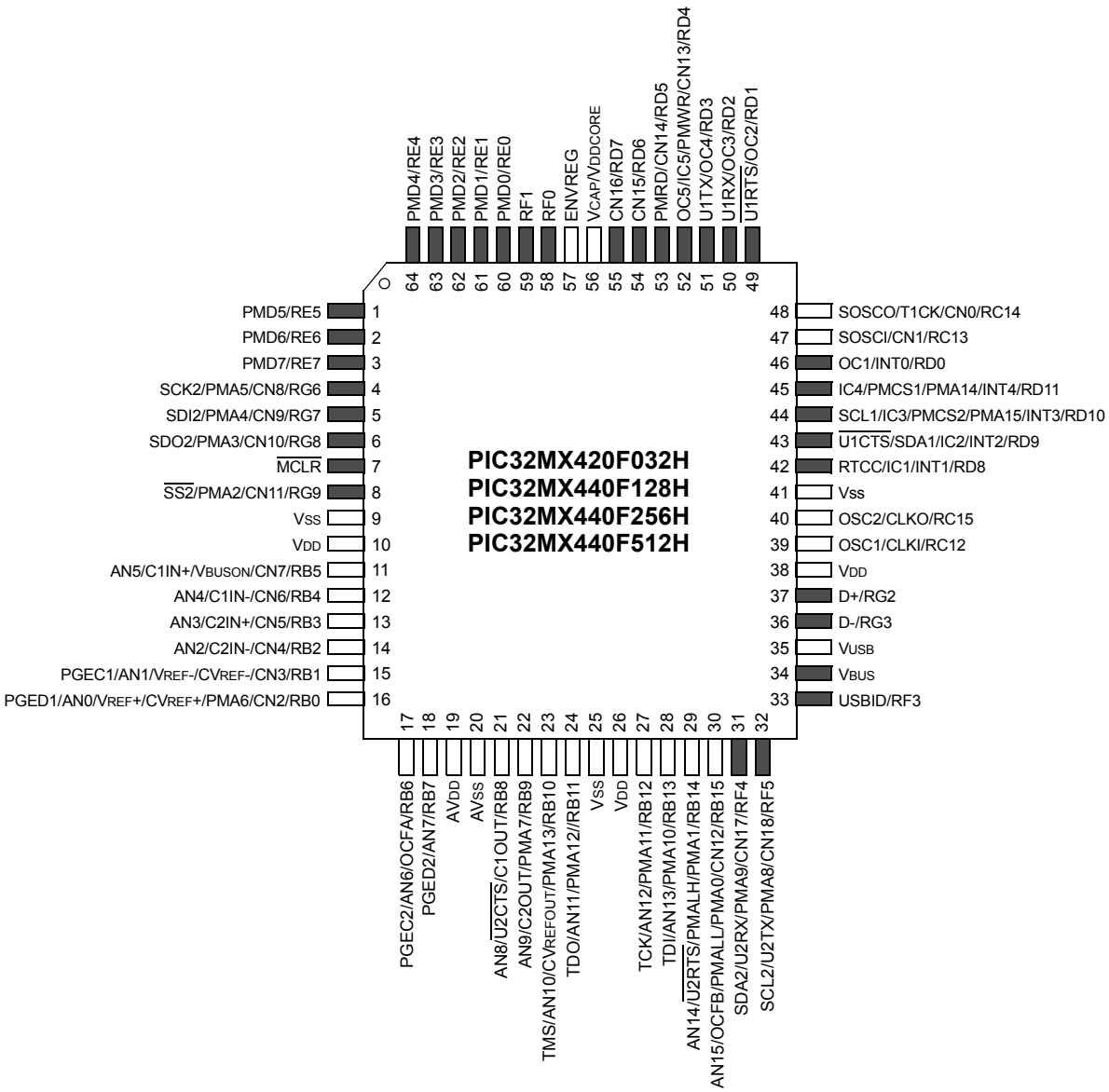


Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

64-Pin TQFP (USB)

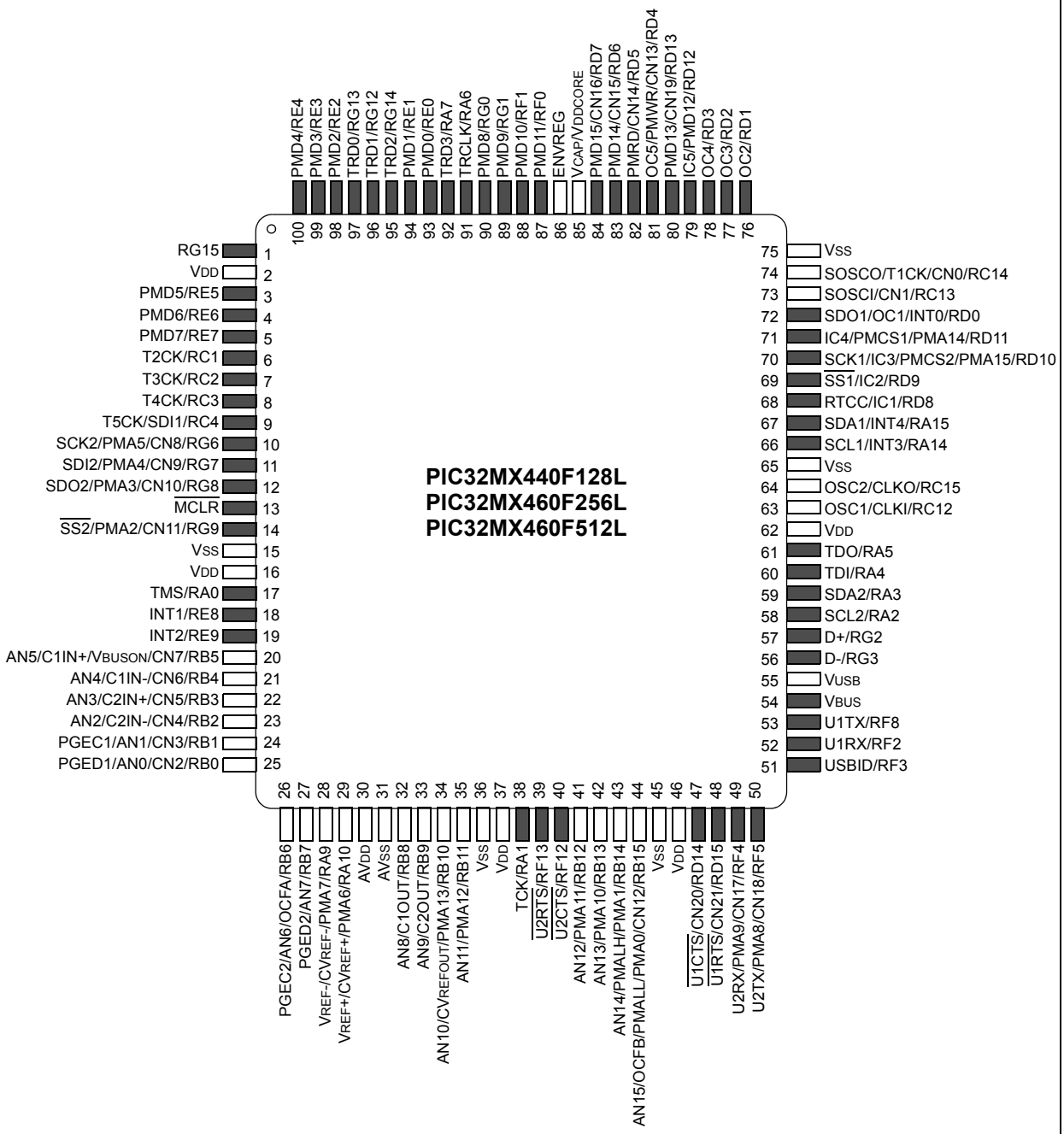
= Pins are up to 5V tolerant



Pin Diagrams (Continued)

100-Pin TQFP (USB)

= Pins are up to 5V tolerant



Pin Diagrams (Continued)

121-Pin XBGA(1)

● = Pins are up to 5V tolerant

PIC32MX440F128L
PIC32MX460F256L
PIC32MX460F512L

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	ENVREG	VSS	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP/ VDDCORE	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	VDD	RC13	RD11
D	RC1	RE7	RE5	VSS	VSS	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	VDD	RG1	VSS	RA15	RD8	RD9	RA14
F	MCLR	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	VSS	VDD	NC	VDD	NC	VBUS	VUSB	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 4 for full pin names.

TABLE 4: PIN NAMES: PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES

Pin Number	Full Pin Name
A1	PMD4/RE4
A2	PMD3/RE3
A3	TRD0/RG13
A4	PMD0/RE0
A5	PMD8/RG0
A6	PMD10/RF1
A7	ENVREG
A8	VSS
A9	IC5/PMD12/RD12
A10	OC3/RD2
A11	OC2/RD1
B1	No Connect (NC)
B2	RG15
B3	PMD2/RE2
B4	PMD1/RE1
B5	TRD3/RA7
B6	PMD11/RF0
B7	VCAP/VDDCORE
B8	PMRD/CN14/RD5
B9	OC4/RD3
B10	VSS
B11	SOSCO/T1CK/CN0/RC14
C1	PMD6/RE6
C2	VDD
C3	TRD1/RG12
C4	TRD2/RG14
C5	TRCLK/RA6
C6	No Connect (NC)
C7	PMD15/CN16/RD7
C8	OC5/PMWR/CN13/RD4
C9	VDD
C10	SOSCI/CN1/RC13
C11	IC4/PMCS1/PMA14/RD11
D1	T2CK/RC1
D2	PMD7/RE7
D3	PMD5/RE5
D4	VSS
D5	VSS
D6	No Connect (NC)
D7	PMD14/CN15/RD6
D8	CN19/PMD13/RD13
D9	SDO1/OC1/INT0/RD0
D10	No Connect (NC)
D11	SCK1/IC3/PMCS2/PMA15/RD10
E1	T5CK/SDI1/RC4
E2	T4CK/RC3
E3	SCK2/PMA5/CN8/RG6
E4	T3CK/RC2
E5	VDD
E6	PMD9/RG1

Pin Number	Full Pin Name
E8	SDA1/INT4/RA15
E9	RTCC/IC1/RD8
E10	$\overline{SS1}$/IC2/RD9
E11	SCL1/INT3/RA14
F1	$\overline{MCLR}$
F2	SDO2/PMA3/CN10/RG8
F3	$\overline{SS2}$/PMA2/CN11/RG9
F4	SDI2/PMA4/CN9/RG7
F5	VSS
F6	No Connect (NC)
F7	No Connect (NC)
F8	Vdd
F9	OSC1/CLKI/RC12
F10	VSS
F11	OSC2/CLKO/RC15
G1	INT1/RE8
G2	INT2/RE9
G3	TMS/RA0
G4	No Connect (NC)
G5	VDD
G6	VSS
G7	VSS
G8	No Connect (NC)
G9	TDO/RA5
G10	SDA2/RA3
G11	TDI/RA4
H1	AN5/C1IN+/VBUSON/CN7/RB5
H2	AN4/C1IN-/CN6/RB4
H3	VSS
H4	VDD
H5	No Connect (NC)
H6	VDD
H7	No Connect (NC)
H8	VBUS
H9	VUSB
H10	D+/RG2
H11	SCL2/RA2
J1	AN3/C2IN+/CN5/RB3
J2	AN2/C2IN-/CN4/RB2
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/PMA12/RB11
J6	TCK/RA1
J7	AN12/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	U1TX/RF8
J11	D-/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0

TABLE 4: PIN NAMES: PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES (CONTINUED)

Pin Number	Full Pin Name
E7	VSS
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	U2CTS/RF12
K7	AN14/PMALH/PMA1/RB14
K8	VDD
K9	U1RTS/CN21/RD15
K10	USBID/RF3
K11	U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/PMA7/RA9

Pin Number	Full Pin Name
K3	VREF+/CVREF+/PMA6/RA10
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	U2RTS/RF13
L7	AN13/PMA10/RB13
L8	AN15/OCFB/PMALL/PMA0/CN12/RB15
L9	U1CTS/CN20/RD14
L10	U2RX/PMA9/CN17/RF4
L11	U2TX/PMA8/CN18/RF5

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NOTES:

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

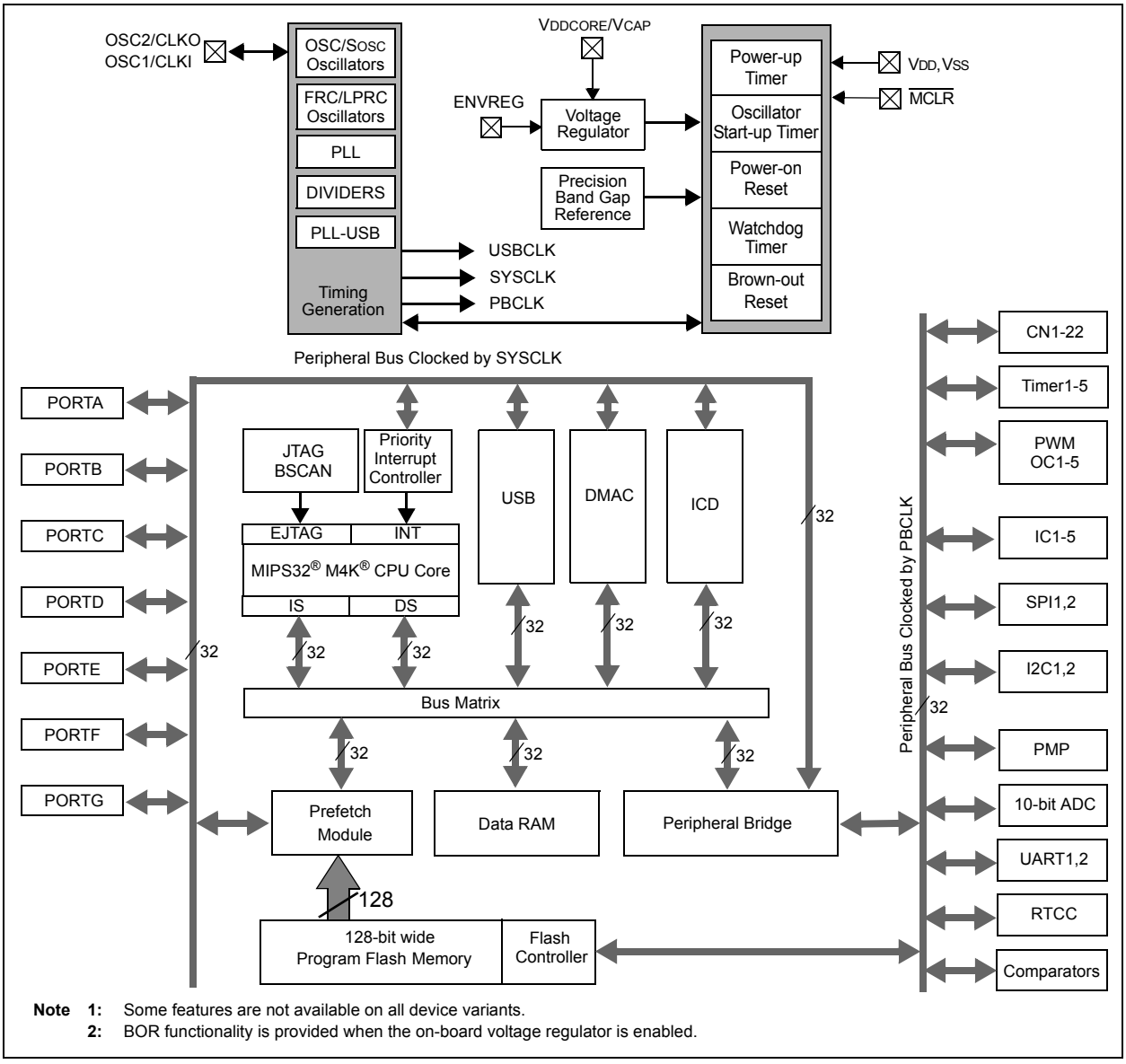
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the PIC32MX3XX/4XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX3XX/4XX families of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM(1,2)



Note 1: Some features are not available on all device variants.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
AN0	16	25	K2	I	Analog	Analog input channels.
AN1	15	24	K1	I	Analog	
AN2	14	23	J2	I	Analog	
AN3	13	22	J1	I	Analog	
AN4	12	21	H2	I	Analog	
AN5	11	20	H1	I	Analog	
AN6	17	26	L1	I	Analog	
AN7	18	27	J3	I	Analog	
AN8	21	32	K4	I	Analog	
AN9	22	33	L4	I	Analog	
AN10	23	34	L5	I	Analog	
AN11	24	35	J5	I	Analog	
AN12	27	41	J7	I	Analog	
AN13	28	42	L7	I	Analog	
AN14	29	43	K7	I	Analog	
AN15	30	44	L8	I	Analog	
CLKI	39	63	F9	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	F11	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	39	63	F9	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	F11	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	C10	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	74	B11	O	—	32.768 kHz low-power oscillator crystal output.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
CN0	48	74	B11	I	ST	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
CN1	47	73	C10	I	ST	
CN2	16	25	K2	I	ST	
CN3	15	24	K1	I	ST	
CN4	14	23	J2	I	ST	
CN5	13	22	J1	I	ST	
CN6	12	21	H2	I	ST	
CN7	11	20	H1	I	ST	
CN8	4	10	E3	I	ST	
CN9	5	11	F4	I	ST	
CN10	6	12	F2	I	ST	
CN11	8	14	F3	I	ST	
CN12	30	44	L8	I	ST	
CN13	52	81	C8	I	ST	
CN14	53	82	B8	I	ST	
CN15	54	83	D7	I	ST	
CN16	55	84	C7	I	ST	
CN17	31	49	L10	I	ST	
CN18	32	50	L11	I	ST	
CN19	—	80	D8	I	ST	
CN20	—	47	L9	I	ST	
CN21	—	48	K9	I	ST	
IC1	42	68	E9	I	ST	Capture inputs 1-5.
IC2	43	69	E10	I	ST	
IC3	44	70	D11	I	ST	
IC4	45	71	C11	I	ST	
IC5	52	79	A9	I	ST	
OCFA	17	26	L1	I	ST	Output Compare Fault A Input.
OC1	46	72	D9	O	—	Output Compare output 1.
OC2	49	76	A11	O	—	Output Compare output 2
OC3	50	77	A10	O	—	Output Compare output 3.
OC4	51	78	B9	O	—	Output Compare output 4.
OC5	52	81	C8	O	—	Output Compare output 5.
OCFB	30	44	L8	I	ST	Output Compare Fault B Input.
INT0	35,46	55,72	H9,D9	I	ST	External interrupt 0.
INT1	42	18	61	I	ST	External interrupt 1.
INT2	43	19	62	I	ST	External interrupt 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
INT3	44	66	E11	I	ST	External interrupt 3.
INT4	45	67	E8	I	ST	External interrupt 4.
RA0	—	17	G3	I/O	ST	PORTA is a bidirectional I/O port.
RA1	—	38	J6	I/O	ST	
RA2	—	58	H11	I/O	ST	
RA3	—	59	G10	I/O	ST	
RA4	—	60	G11	I/O	ST	
RA5	—	61	G9	I/O	ST	
RA6	—	91	C5	I/O	ST	
RA7	—	92	B5	I/O	ST	
RA9	—	28	L2	I/O	ST	
RA10	—	29	K3	I/O	ST	
RA14	—	66	E11	I/O	ST	
RA15	—	67	E8	I/O	ST	
RB0	16	25	K2	I/O	ST	PORTB is a bidirectional I/O port.
RB1	15	24	K1	I/O	ST	
RB2	14	23	J2	I/O	ST	
RB3	13	22	J1	I/O	ST	
RB4	12	21	H2	I/O	ST	
RB5	11	20	H1	I/O	ST	
RB6	17	26	L1	I/O	ST	
RB7	18	27	J3	I/O	ST	
RB8	21	32	K4	I/O	ST	
RB9	22	33	L4	I/O	ST	
RB10	23	34	L5	I/O	ST	
RB11	24	35	J5	I/O	ST	
RB12	27	41	J7	I/O	ST	
RB13	28	42	L7	I/O	ST	
RB14	29	43	K7	I/O	ST	
RB15	30	44	L8	I/O	ST	
RC1	—	6	D1	I/O	ST	PORTC is a bidirectional I/O port.
RC2	—	7	E4	I/O	ST	
RC3	—	8	E2	I/O	ST	
RC4	—	9	E1	I/O	ST	
RC12	39	63	F9	I/O	ST	
RC13	47	73	C10	I/O	ST	
RC14	48	74	B11	I/O	ST	
RC15	40	64	F11	I/O	ST	

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
P = Power
I = Input

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RD0	46	72	D9	I/O	ST	PORTD is a bidirectional I/O port.
RD1	49	76	A11	I/O	ST	
RD2	50	77	A10	I/O	ST	
RD3	51	78	B9	I/O	ST	
RD4	52	81	C8	I/O	ST	
RD5	53	82	B8	I/O	ST	
RD6	54	83	D7	I/O	ST	
RD7	55	84	C7	I/O	ST	
RD8	42	68	E9	I/O	ST	
RD9	43	69	E10	I/O	ST	
RD10	44	70	D11	I/O	ST	
RD11	45	71	C11	I/O	ST	
RD12	—	79	A9	I/O	ST	
RD13	—	80	D8	I/O	ST	
RD14	—	47	L9	I/O	ST	
RD15	—	48	K9	I/O	ST	
RE0	60	93	A4	I/O	ST	PORTE is a bidirectional I/O port.
RE1	61	94	B4	I/O	ST	
RE2	62	98	B3	I/O	ST	
RE3	63	99	A2	I/O	ST	
RE4	64	100	A1	I/O	ST	
RE5	1	3	D3	I/O	ST	
RE6	2	4	C1	I/O	ST	
RE7	3	5	D2	I/O	ST	
RE8	—	18	G1	I/O	ST	
RE9	—	19	G2	I/O	ST	
RF0	58	87	B6	I/O	ST	PORTF is a bidirectional I/O port.
RF1	59	88	A6	I/O	ST	
RF2	34	52	K11	I/O	ST	
RF3	33	51	K10	I/O	ST	
RF4	31	49	L10	I/O	ST	
RF5	32	50	L11	I/O	ST	
RF6	35	55	H9	I/O	ST	
RF7	—	54	H8	I/O	ST	
RF8	—	53	J10	I/O	ST	
RF12	—	40	K6	I/O	ST	
RF13	—	39	L6	I/O	ST	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RG0	—	90	A5	I/O	ST	PORTG is a bidirectional I/O port.
RG1	—	89	E6	I/O	ST	
RG6	4	10	E3	I/O	ST	
RG7	5	11	F4	I/O	ST	
RG8	6	12	F2	I/O	ST	
RG9	8	14	F3	I/O	ST	
RG12	—	96	C3	I/O	ST	
RG13	—	97	A3	I/O	ST	
RG14	—	95	C4	I/O	ST	
RG15	—	1	B2	I/O	ST	
RG2	37	57	H10	I	ST	PORTG input pins.
RG3	36	56	J11	I	ST	
T1CK	48	74	B11	I	ST	Timer1 external clock input.
T2CK	—	6	D1	I	ST	Timer2 external clock input.
T3CK	—	7	E4	I	ST	Timer3 external clock input.
T4CK	—	8	E2	I	ST	Timer4 external clock input.
T5CK	—	9	E1	I	ST	Timer5 external clock input.
$\overline{U1CTS}$	43	47	L9	I	ST	UART1 clear to send.
$\overline{U1RTS}$	35, 49	48	K9	O	—	UART1 ready to send.
U1RX	34, 50	52	K11	I	ST	UART1 receive.
U1TX	33, 51	51, 53	J10, K10	O	—	UART1 transmit.
$\overline{U2CTS}$	21	40	K6	I	ST	UART2 clear to send.
$\overline{U2RTS}$	29	39	L6	O	—	UART2 ready to send.
U2RX	31	49	L10	I	ST	UART2 receive.
U2TX	32	50	L11	O	—	UART2 transmit.
SCK1	35	55, 70	D11, H9	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	34	9, 54	E1, H8	I	ST	SPI1 data in.
SDO1	33	53, 72	D9, J10	O	—	SPI1 data out.
$\overline{SS1}$	14	23, 69	E10, J2	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SCK2	4	10	E3	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	5	11	F4	I	ST	SPI2 data in.
SDO2	6	12	F2	O	—	SPI2 data out.
$\overline{SS2}$	8	14	F3	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SCL1	37, 44	57, 66	E11, H10	I/O	ST	Synchronous serial clock input/output for I2C1.
SDA1	36, 43	56, 67	E8, J11	I/O	ST	Synchronous serial data input/output for I2C1.
SCL2	32	58	H11	I/O	ST	Synchronous serial clock input/output for I2C2.
SDA2	31	59	G10	I/O	ST	Synchronous serial data input/output for I2C2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
TMS	23	17	G3	I	ST	JTAG Test mode select pin.
TCK	27	38	J6	I	ST	JTAG test clock input pin.
TDI	28	60	G11	I	ST	JTAG test data input pin.
TDO	24	61	G9	O	—	JTAG test data output pin.
RTCC	42	68	E9	O	—	Real-Time Clock Alarm Output.
CVREF-	15	28	L2	I	Analog	Comparator Voltage Reference (low).
CVREF+	16	29	K3	I	Analog	Comparator Voltage Reference (high).
CVREFOUT	23	34	L5	O	Analog	Comparator Voltage Reference Output.
C1IN-	12	21	H2	I	Analog	Comparator 1 Negative Input.
C1IN+	11	20	H1	I	Analog	Comparator 1 Positive Input.
C1OUT	21	32	K4	O	—	Comparator 1 Output.
C2IN-	14	23	J2	I	Analog	Comparator 2 Negative Input.
C2IN+	13	22	J1	I	Analog	Comparator 2 Positive Input.
C2OUT	22	33	L4	O	—	Comparator 2 Output.
PMA0	30	44	L8	I/O	TTL/ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	43	K7	I/O	TTL/ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	14	F3	O	—	Parallel Master Port Address (De-multiplexed Master Modes).
PMA3	6	12	F2	O	—	
PMA4	5	11	F4	O	—	
PMA5	4	10	E3	O	—	
PMA6	16	29	K3	O	—	
PMA7	22	28	L2	O	—	
PMA8	32	50	L11	O	—	
PMA9	31	49	L10	O	—	
PMA10	28	42	L7	O	—	
PMA11	27	41	J7	O	—	
PMA12	24	35	J5	O	—	
PMA13	23	34	L5	O	—	
PMA14	45	71	C11	O	—	
PMA15	44	70	D11	O	—	
PMCS1	45	71	C11	O	—	Parallel Master Port Chip Select 1 Strobe.
PMCS2	44	70	D11	O	—	Parallel Master Port Chip Select 2 Strobe.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PMD0	60	93	A4	I/O	TTL/ST	Parallel Master Port Data (De-multiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	94	B4	I/O	TTL/ST	
PMD2	62	98	B3	I/O	TTL/ST	
PMD3	63	99	A2	I/O	TTL/ST	
PMD4	64	100	A1	I/O	TTL/ST	
PMD5	1	3	D3	I/O	TTL/ST	
PMD6	2	4	C1	I/O	TTL/ST	
PMD7	3	5	D2	I/O	TTL/ST	
PMD8	—	90	A5	I/O	TTL/ST	
PMD9	—	89	E6	I/O	TTL/ST	
PMD10	—	88	A6	I/O	TTL/ST	
PMD11	—	87	B6	I/O	TTL/ST	
PMD12	—	79	A9	I/O	TTL/ST	
PMD13	—	80	D8	I/O	TTL/ST	
PMD14	—	83	D7	I/O	TTL/ST	
PMD15	—	84	C7	I/O	TTL/ST	
PMRD	53	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	81	C8	O	—	Parallel Master Port Write Strobe.
PMALL	30	44	L8	O	—	Parallel Master Port Address Latch Enable low-byte (Multiplexed Master modes).
PMALH	29	43	K7	O	—	Parallel Master Port Address Latch Enable high-byte (Multiplexed Master modes).
VBUS	34	54	H8	I	Analog	USB Bus Power Monitor.
VUSB	35	55	H9	P	—	USB Internal Transceiver Supply.
VBUSON	11	20	H1	O	—	USB Host and OTG Bus Power Control Output.
D+	37	57	H10	I/O	Analog	USB D+.
D-	36	56	J11	I/O	Analog	USB D-.
USBID	33	51	K10	I	ST	USB OTG ID Detect.
ENVREG	57	86	A7	I	ST	Enable for On-Chip Voltage Regulator.
TRCLK	—	91	C5	O	—	Trace Clock.
TRD0	—	97	A3	O	—	Trace Data Bits 0-3.
TRD1	—	96	C3	O	—	
TRD2	—	95	C4	O	—	
TRD3	—	92	B5	O	—	
PGED1	16	25	K2	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGEC1	15	24	K1	I	ST	Clock input pin for programming/debugging communication channel 1.

Legend: CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = TTL input buffer; Analog = Analog input; O = Output; P = Power; I = Input

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PGED2	18	27	J3	I/O	ST	Data I/O pin for programming/debugging communication channel 2.
PGEC2	17	26	L1	I	ST	Clock input pin for programming/debugging communication channel 2.
$\overline{MCLR}$	7	13	F1	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	J4	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	L3	P	P	Ground reference for analog modules.
VDD	10, 26, 38	2, 16, 37, 46, 62	C2, C9, E5, F8, G5, H4, H6, K8	P	—	Positive supply for peripheral logic and I/O pins.
VCAP/ VDDCORE	56	85	B7	P	—	CPU logic filter capacitor connection.
Vss	9, 25, 41	15, 36, 45, 65, 75	A8, B10, D4, D5, E7, F10, F5, G6, G7, H3	P	—	Ground reference for logic and I/O pins.
VREF+	16	29	K3	I	Analog	Analog voltage reference (high) input.
VREF-	15	28	L2	I	Analog	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the PIC32MX3XX/4XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP/VDDCORE
  (see **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP/VDDCORE)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.8 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of ADC use and ADC voltage reference source.

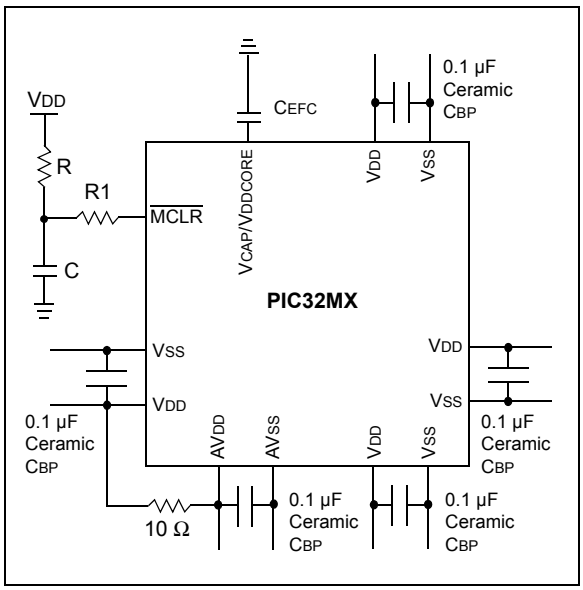
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP/VDDCORE)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR (< 1 Ohm) capacitor is required on the VCAP/VDDCORE pin, which is used to stabilize the internal voltage regulator output. The VCAP/VDDCORE pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 29.0 "Electrical Characteristics"** for additional information on CEFC specifications. This mode is enabled by connecting the ENVREG pin to VDD.

2.3.2 EXTERNAL REGULATOR MODE

In this mode the core voltage is supplied externally through the VDDCORE pin. A low-ESR capacitor of 10 µF is recommended on the VDDCORE pin. This mode is enabled by grounding the ENVREG pin.

The placement of this capacitor should be close to the VCAP/VDDCORE. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 26.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

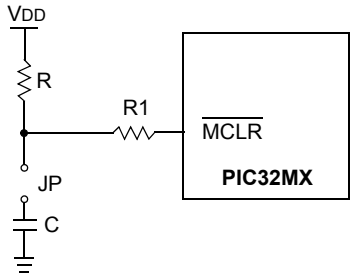
- Device Reset
- Device Programming and Debugging

Pulling The MCLR pin low generates a device reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

3: The capacitor can be sized to prevent unintentional resets from brief glitches or to extend the device reset period during POR.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip website.

- *"MPLAB® ICD 2 In-Circuit Debugger User's Guide"* DS51331
- *"Using MPLAB® ICD 2"* (poster) DS51265
- *"MPLAB® ICD 2 Design Advisory"* DS51566
- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™"* (poster) DS51749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.7 Trace

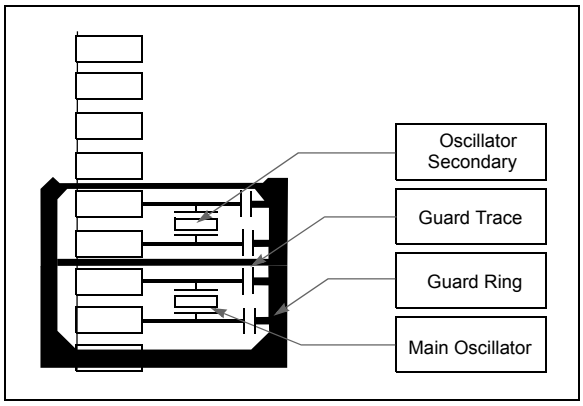
The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.9 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 2, ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins by setting all bits in the ADPCFG register.

The bits in this register that correspond to the A/D pins that are initialized by MPLAB ICD 2, ICD 3 or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must clear the corresponding bits in the ADPCFG register during initialization of the ADC module.

When MPLAB ICD 2, ICD 3 or REAL ICE is used as a programmer, the user application firmware must correctly configure the ADPCFG register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

2.10 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternately, inputs can be reserved by connecting the pin to VSS through a 1k to 10k resistor and configuring the pin as an input.

3.0 PIC32MX MCU

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "MCU"** (DS61113) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at: www.mips.com/products/cores/32-bit-cores/mips32-m4k/#.

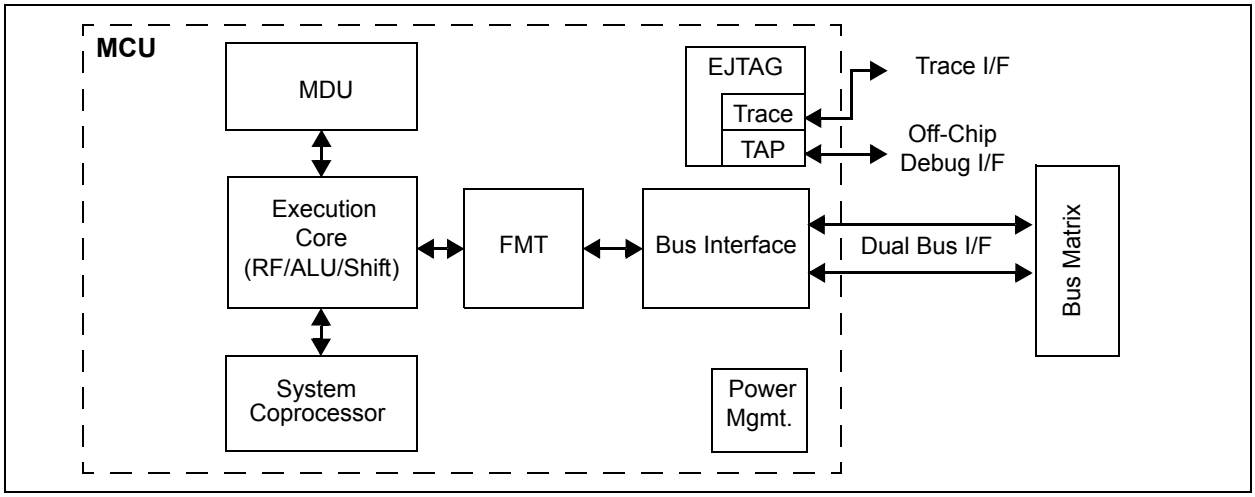
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The MCU module is the heart of the PIC32MX3XX/4XX Family processor. The MCU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- 32-bit Address and Data Paths
- MIPS32 Enhanced Architecture (Release 2)
  - Multiply-Accumulate and Multiply-Subtract Instructions
  - Targeted Multiply Instruction
  - Zero/One Detect Instructions
  - `WAIT` Instruction
  - Conditional Move Instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
- MIPS16e® Code Compression
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple Dual Bus Interface
  - Independent 32-bit address and data busses
  - Transactions can be aborted to improve interrupt latency
- Autonomous Multiply/Divide Unit
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 34 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace
  - Support for single stepping
  - Virtual instruction and data address/value
  - breakpoints
  - PC tracing with trace compression

FIGURE 3-1: MCU BLOCK DIAGRAM



3.2 Architecture Overview

The PIC32MX3XX/4XX Family core contains several logic blocks working together in parallel, providing an efficient high performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The PIC32MX3XX/4XX Family core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit general purpose registers used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and Store Aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The PIC32MX3XX/4XX Family core includes a multiply/divide unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the integer unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32MX core only checks the value of the latter (*rt)* operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit-wide rs, 15 iterations are skipped, and for a 24-bit-wide rs, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32MX core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: PIC32MX3XX/4XX FAMILY CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU	16 bits	1	1
	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general purpose register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, multiply-add (MADD) and multiply-subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (kernel, user and debug), and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX3XX/4XX Family core
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers
8	BadVAddr(1)	Reports the address for the most recent address-related exception
9	Count(1)	Processor cycle count
10	Reserved	Reserved in the PIC32MX3XX/4XX Family core
11	Compare(1)	Timer interrupt control
12	Status(1)	Processor status and control
12	IntCtl(1)	Interrupt system status and control
12	SRSCtl(1)	Shadow register set status and control
12	SRSMap(1)	Provides mapping from vectored interrupt to a shadow set
13	Cause(1)	Cause of last general exception
14	EPC(1)	Program counter at last exception
15	PRId	Processor identification and revision
15	EBASE	Exception vector base register
16	Config	Configuration register
16	Config1	Configuration register 1
16	Config2	Configuration register 2
16	Config3	Configuration register 3

TABLE 3-2: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
17-22	Reserved	Reserved in the PIC32MX3XX/4XX Family core
23	Debug(2)	Debug control and exception status
24	DEPC(2)	Program counter at last debug exception
25-29	Reserved	Reserved in the PIC32MX3XX/4XX Family core
30	ErrorEPC(1)	Program counter at last error
31	DESAVE(2)	Debug handler scratchpad register

Note 1: Registers used in exception processing.

2: Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 shows the exception types in order of priority.

TABLE 3-3: PIC32MX3XX/4XX FAMILY CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR)
DSS	EJTAG Debug Single Step
DINT	EJTAG Debug Interrupt. Caused by the assertion of the external *EJ_DINT* input, or by setting the EjtagBrk bit in the ECR register
NMI	Assertion of NMI signal
Interrupt	Assertion of unmasked hardware or software interrupt signal
DIB	EJTAG debug hardware instruction break matched
AdEL	Fetch address alignment error Fetch reference to protected address
IBE	Instruction fetch bus error
DBp	EJTAG Breakpoint (execution of `SDBBP` instruction)
Sys	Execution of `SYSCALL` instruction
Bp	Execution of `BREAK` instruction
RI	Execution of a Reserved Instruction
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled
CEU	Execution of a `CorExtend` instruction when `CorExtend` is not enabled
Ov	Execution of an arithmetic instruction that overflowed
Tr	Execution of a trap (when trap condition is true)
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG Data Value Break on Store (address + value)
AdEL	Load address alignment error Load reference to protected address
AdES	Store address alignment error Store to protected address
DBE	Load or store bus error
DDBL	EJTAG data hardware breakpoint matched in load data compare

3.3 Power Management

The PIC32MX3XX/4XX Family core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking power-down mode is through execution of the `WAIT` instruction. For more information on power management, see **Section 25.0 "Power-Saving Features"**.

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX3XX/4XX Family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The PIC32MX3XX/4XX Family core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard user mode and kernel modes of operation, the PIC32MX3XX/4XX Family core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (`DERET`) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the PIC32MX3XX/4XX Family core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used.

NOTES:

4.0 MEMORY ORGANIZATION

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 3. "Memory Organization"** (DS61115) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions including program, data memory, SFRs and Configuration registers reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX3XX/4XX to execute from data memory.

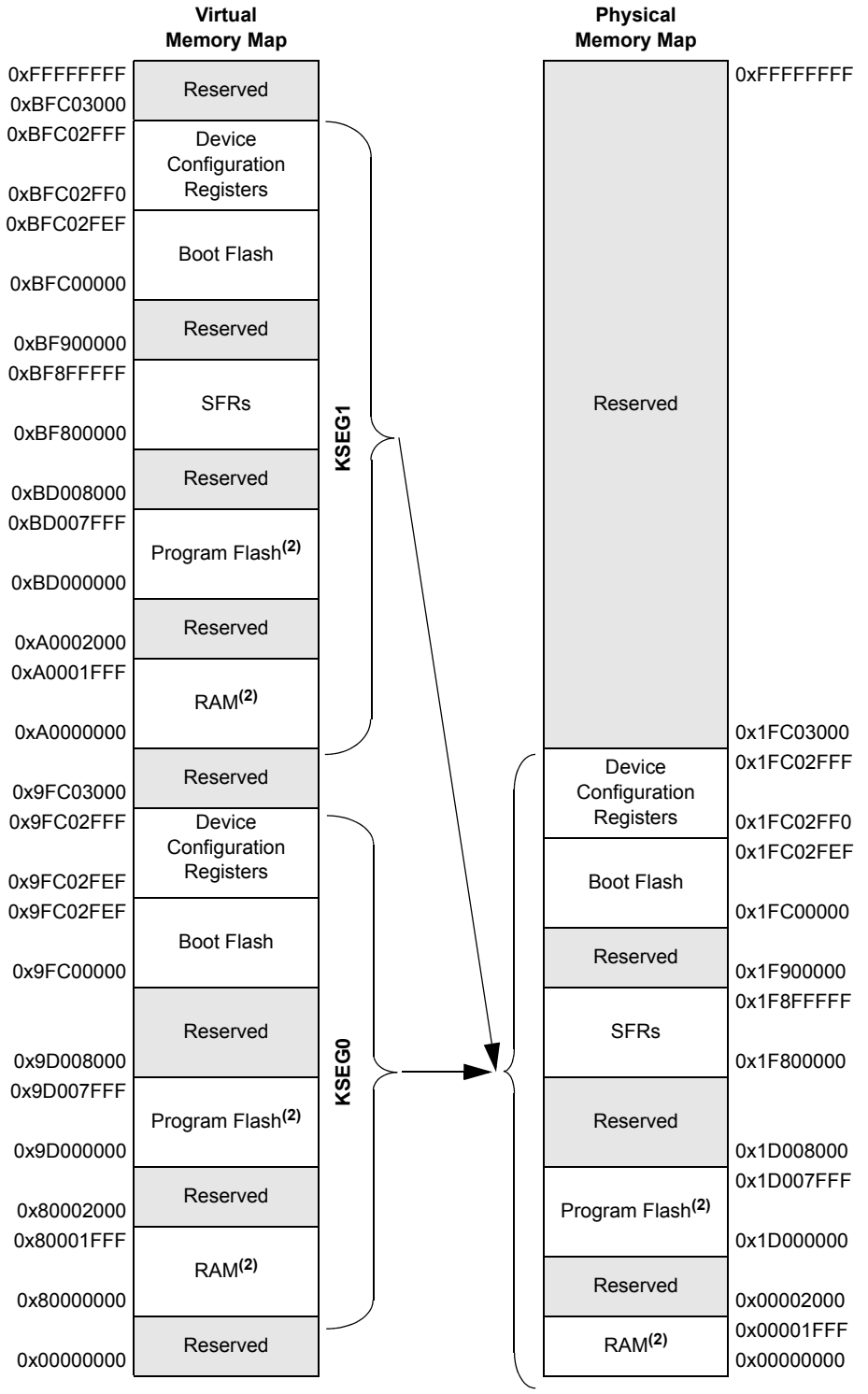
4.1 Key Features

- 32-bit native data width
- Separate User and Kernel mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable and non-cacheable address regions

4.2 PIC32MX3XX/4XX Memory Layout

PIC32MX3XX/4XX microcontrollers implement two address spaces: Virtual and Physical. All hardware resources such as program memory, data memory and peripherals are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by peripherals such as DMA and Flash controller that access memory independently of CPU.

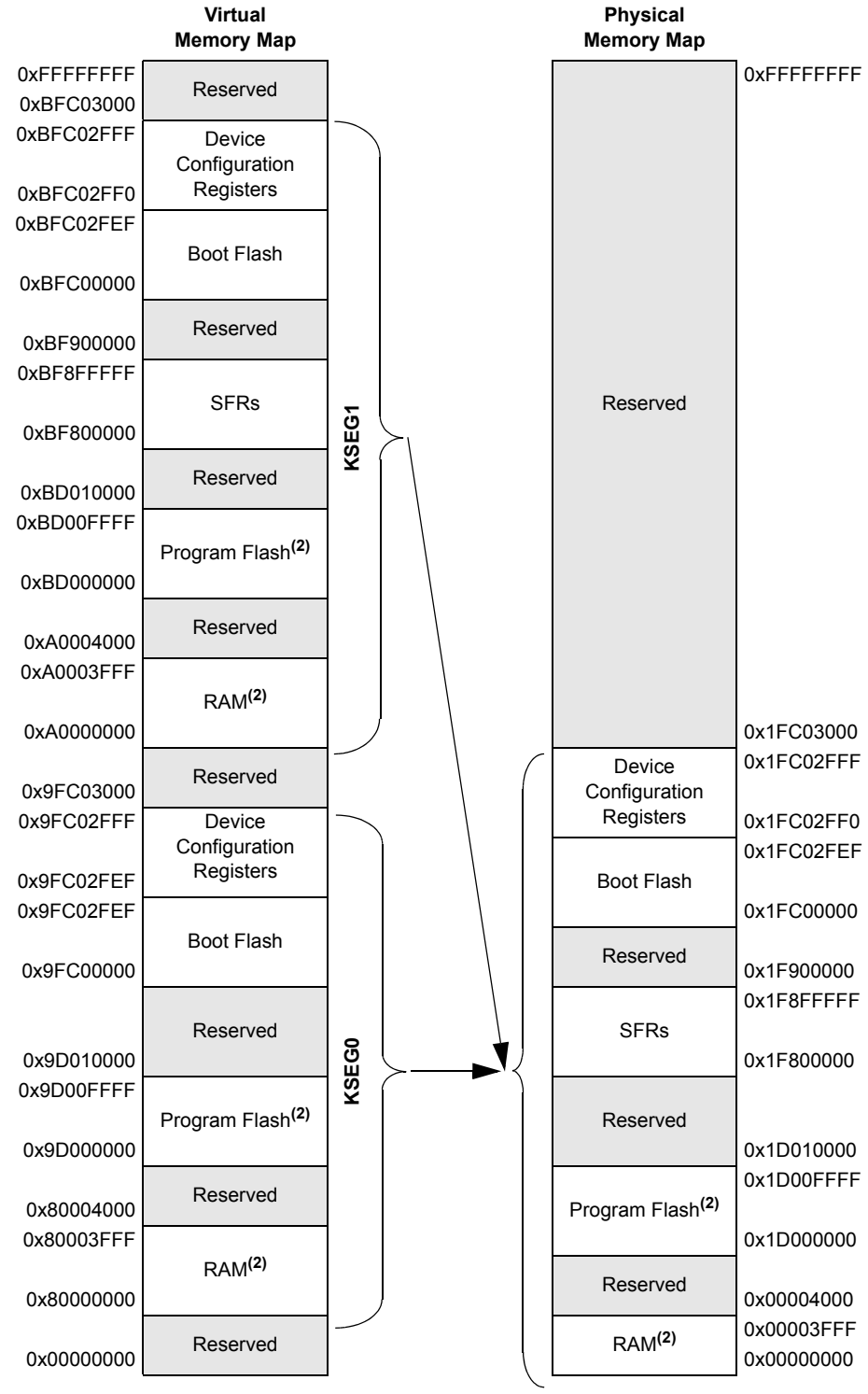
FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX320F032H AND PIC32MX420F032H DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

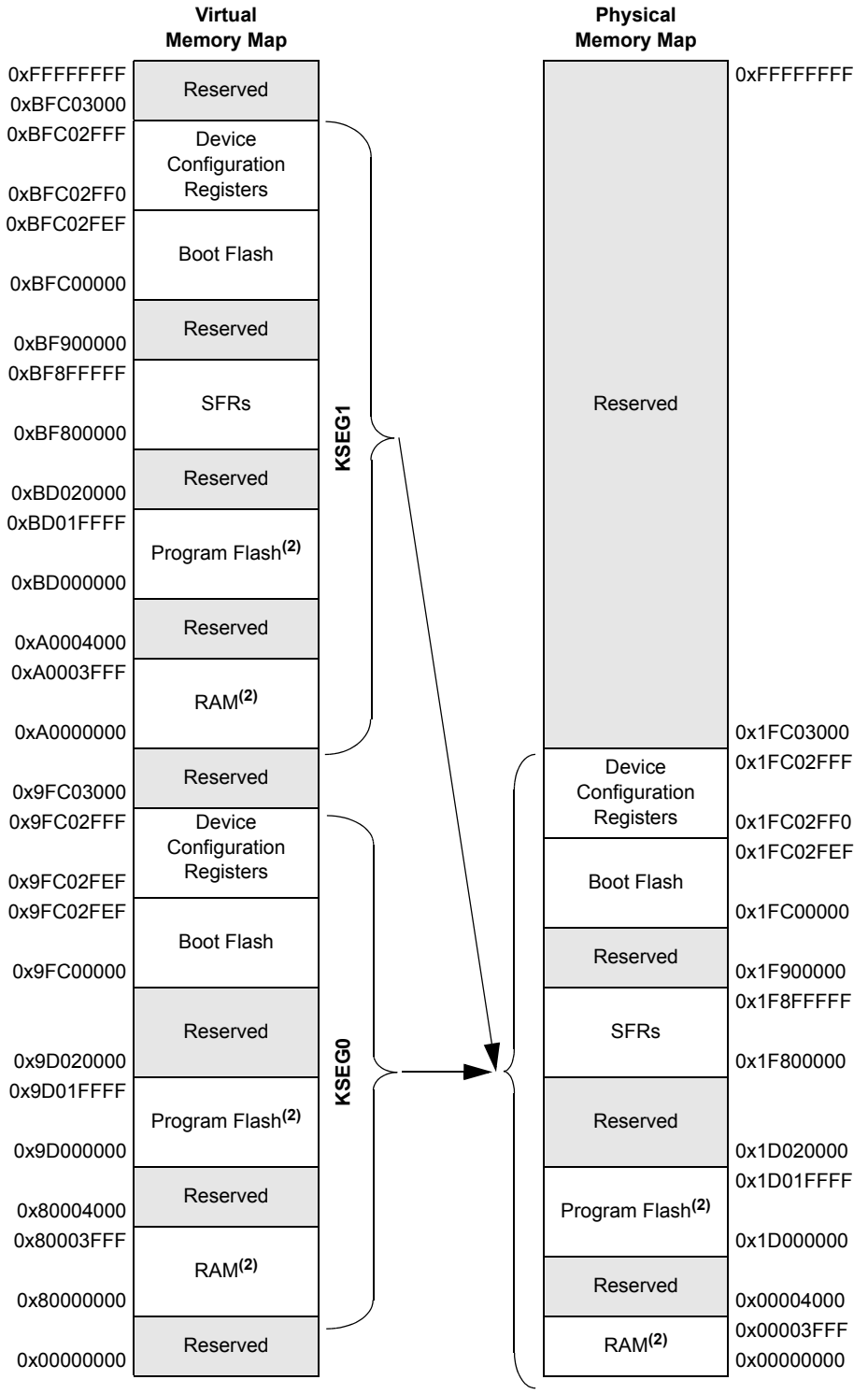
FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX320F064H DEVICE(1)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

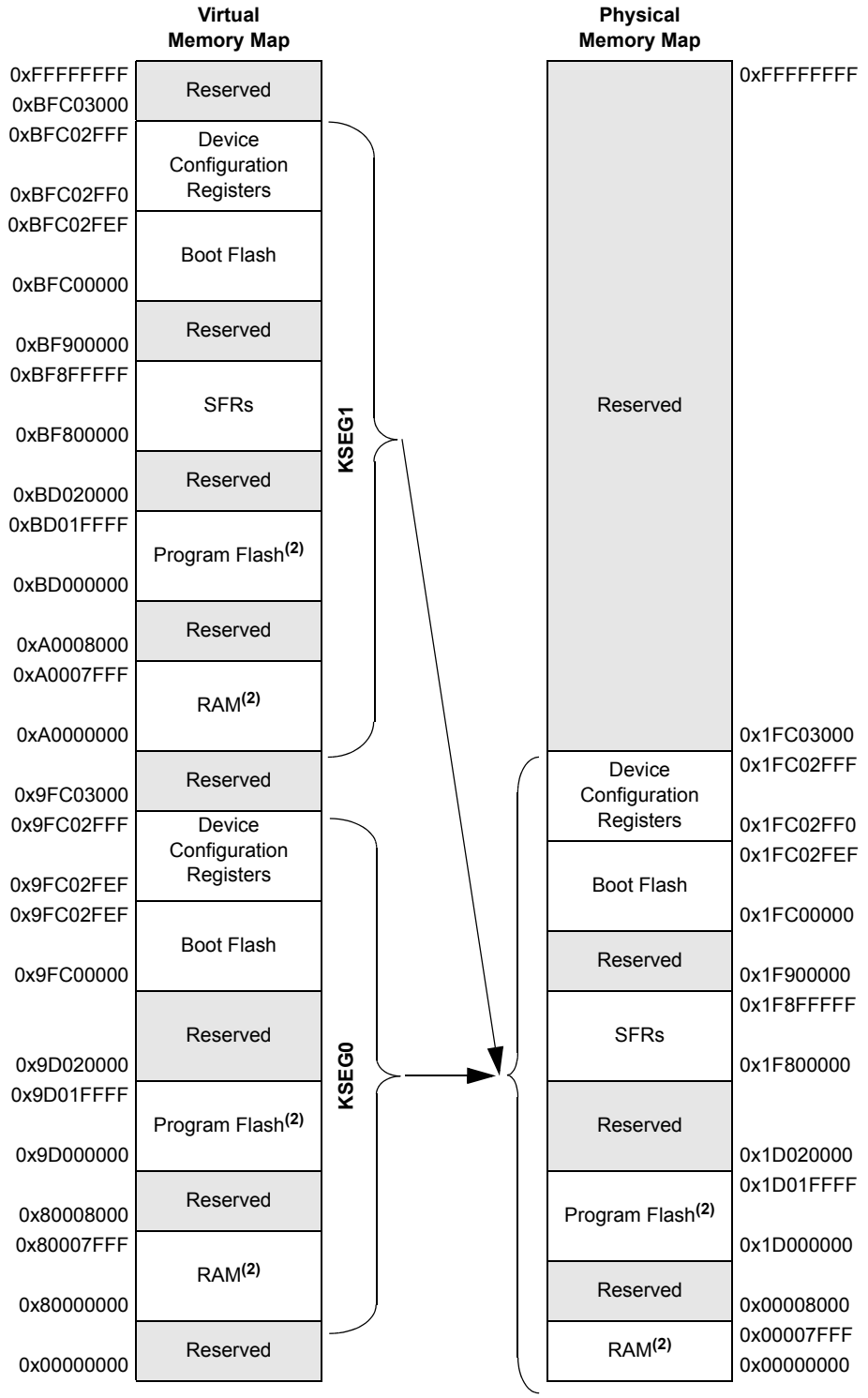
FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX320F128H AND PIC32MX320F128L DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

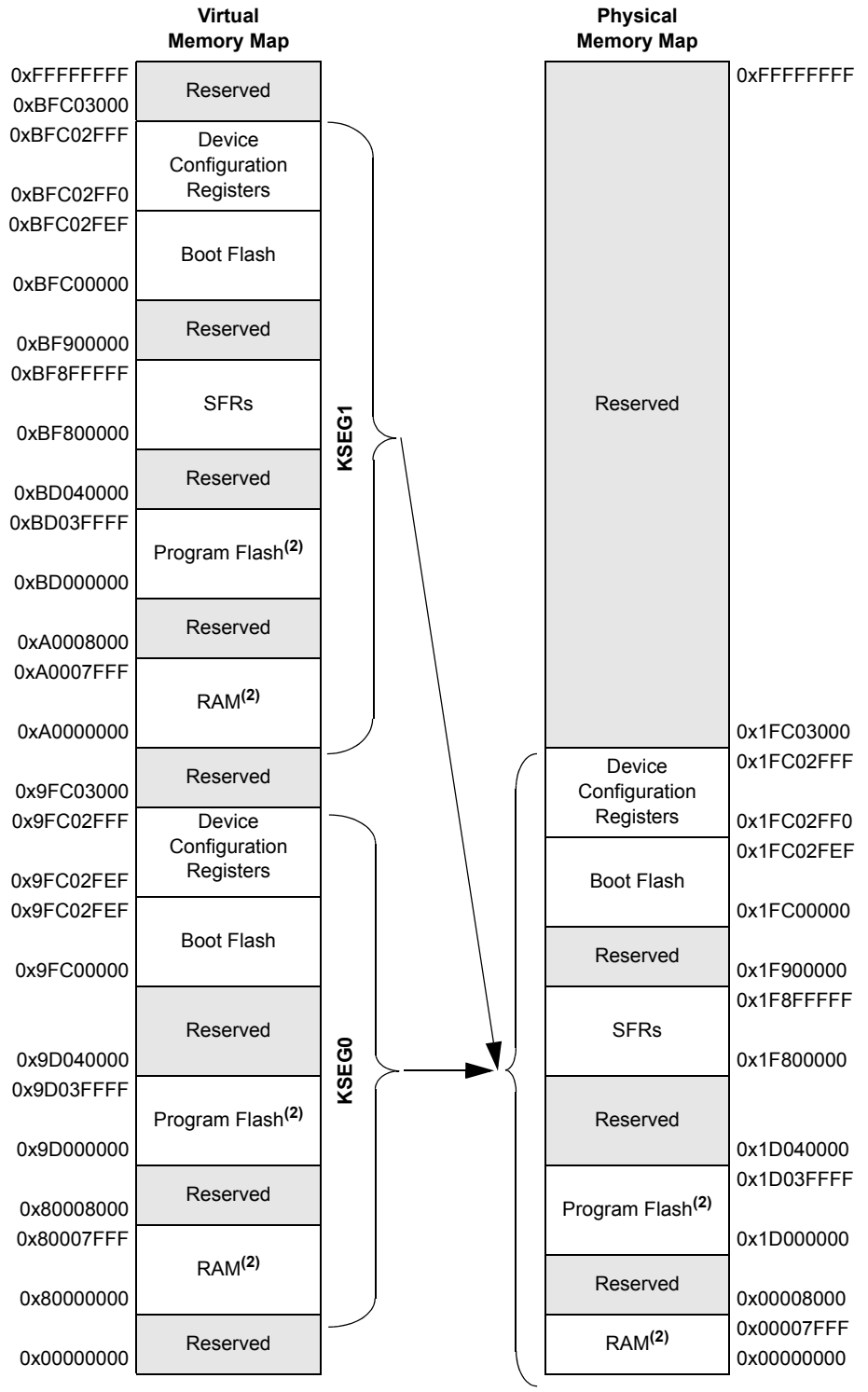
FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX340F128H, PIC32MX340F128L, PIC32MX440F128H AND PIC32MX440F128L DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

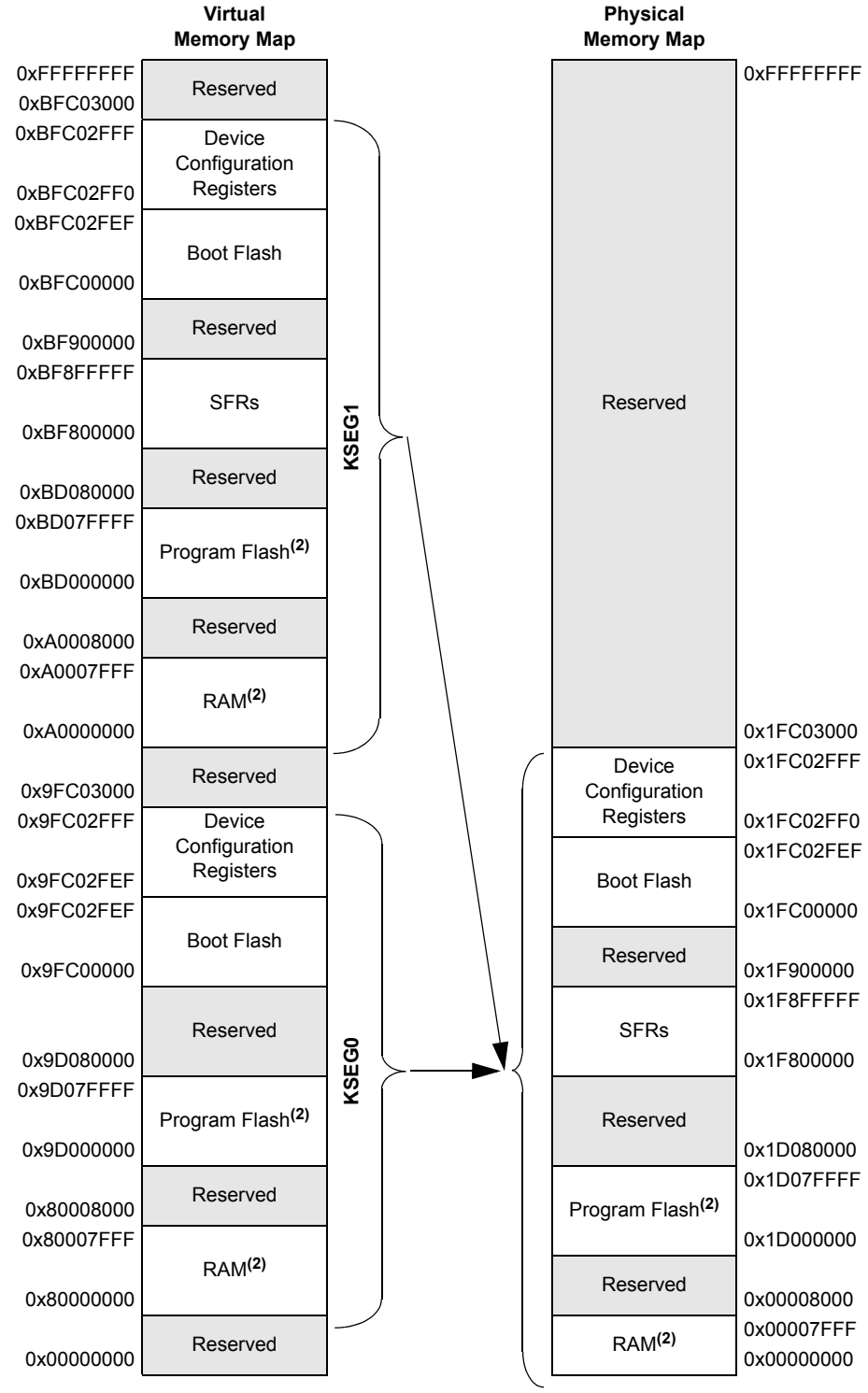
FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX340F256H, PIC32MX360F256L, PIC32MX440F256H AND PIC32MX460F256L DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX340F512H, PIC32MX360F512L, PIC32MX440F512H AND PIC32MX460F512L DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

TABLE 4-1: BUS MATRIX REGISTERS MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	BMX CON(1)	31:16	—	—	—	—	—	BMXCHEDMA	—	—	—	—	—	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	001F
		15:0	—	—	—	—	—	—	—	—	—	BMXWSDRM	—	—	—	BMXARB<2:0>			0042
2010	BMX DKPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDKPBA<15:0>																0000
2020	BMX DUDBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUDBA<15:0>																0000
2030	BMX DUPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUPBA<15:0>																0000
2040	BMX DRMSZ	31:16	BMXDRMSZ<31:0>																xxxx
		15:0																	xxxx
2050	BMX PUPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>				0000
		15:0	BMXPUPBA<15:0>																0000
2060	BMX PFMSZ	31:16	BMXPFMSZ<31:0>																xxxx
		15:0																	xxxx
2070	BMX BOOTSZ	31:16	BMXBOOTSZ<31:0>																0000
		15:0																	3000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET,and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-2: INTERRUPT REGISTERS MAP FOR PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	FRZ	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	USBIF	FCEIF	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	USBIE	FCEIE	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>		—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-3: INTERRUPT REGISTERS MAP FOR PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX340F128L, PIC32MX340F256L AND PIC32MX340F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	FRZ	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	—	FCEIF	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	—	FCEIE	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	—	—	—	—	—	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>		—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-4: INTERRUPT REGISTERS MAP FOR PIC32MX320F032H, PIC32MXF064H, PIC32MX320F128H AND PIC32MX320F128L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	FRZ	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	—	FCEIF	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	—	FCEIE	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	—	—	—	—	—	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>		—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-5: INTERRUPT REGISTERS MAP FOR PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	FRZ	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	USBIF	FCEIF	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	USBIE	FCEIE	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-6: INTERRUPT REGISTERS MAP FOR THE PIC32MX420F032H DEVICE ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	FRZ	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	USBIF	FCEIF	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	USBIE	FCEIE	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		—	—	—	U1IP<2:0>			U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>		—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-7: TIMER1-5 REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-8: INPUT CAPTURE1-5 REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-9: OUTPUT COMPARE1-5 REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
3020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
3220	OC2RS	31:16 15:0	OC2RS<31:0>																xxxx
																			xxxx
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
3420	OC3RS	31:16 15:0	OC3RS<31:0>																xxxx
																			xxxx
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
3620	OC4RS	31:16 15:0	OC4RS<31:0>																xxxx
																			xxxx
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
3820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-10: I2C1-2 REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
5010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0																	0000
			—	—	—	—	—	—	ADD<9:0>										0000
5030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	I2C1BRG<11:0>												0000
5050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2CT1DATA<7:0>								0000
5260	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2CR1DATA<7:0>								0000
5200	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
5210	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
5220	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
5230	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
5240	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	I2C2BRG<11:0>												0000
5250	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2CT2DATA<7:0>								0000
5260	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2CR2DATA<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-11: UART1-2 REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	U1MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6010	U1STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6040	U1BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BRG<15:0>																0000
6200	U2MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6210	U2STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6240	U2BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BRG<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-12: SPI1-2 REGISTERS MAP(1,2)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0000
		15:0	ON	FRZ	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5810	SPI1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0000
5820	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5830	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0000
		15:0	ON	FRZ	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5A10	SPI2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0000
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: SPI2 Module is not present on PIC32MX420FXXXX/440FXXXX devices.

TABLE 4-13: ADC REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9060	AD1PCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-13: ADC REGISTERS MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000
9120	ADC1BUFB	31:16	ADC Result Word B (ADC1BUFB<31:0>)																0000
		15:0																	0000
9130	ADC1BUFC	31:16	ADC Result Word C (ADC1BUFC<31:0>)																0000
		15:0																	0000
9140	ADC1BUFD	31:16	ADC Result Word D (ADC1BUFD<31:0>)																0000
		15:0																	0000
9150	ADC1BUFE	31:16	ADC Result Word E (ADC1BUFE<31:0>)																0000
		15:0																	0000
9160	ADC1BUFF	31:16	ADC Result Word F (ADC1BUFF<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-14: DMA GLOBAL REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	SUSPEND	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	—	DMACH<1:0>		0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-15: DMA CRC REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PLEN<3:0>				CRCEN	CRCAPP	—	—	—	—	CRCCH<1:0>		0000
3040	DCRCDATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCDATA<15:0>																0000
3050	DCRCXOR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCXOR<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-16: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>								0000
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>								0000
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSTR<7:0>								0000
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>								0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>								0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>								0000
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR and DCHxCPTR have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-16: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY(1) (CONTINUED)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>								0000
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>								0000
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSPTR<7:0>								0000
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>								0000
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>								0000
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>								0000
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>								0000
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>								0000
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSPTR<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR and DCHxCPTR have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-16: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY(1) (CONTINUED)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>								0000
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>								0000
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>								0000
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
32E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>								0000
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>								0000
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHSTR<7:0>								0000
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>								0000
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>								0000
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>								0000
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR and DCHxCPTR have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-17: COMPARATOR REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	FRZ	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-18: COMPARATOR VOLTAGE REFERENCE REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-19: FLASH CONTROLLER REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F400	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
F420	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
F430	NVMDATA	31:16	NVMDATA<31:0>																0000
		15:0																	0000
F440	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-20: SYSTEM CONTROL REGISTERS MAP(1,2)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			RCDIV<2:0>			—	SOSCRDY	—	PBDIV<1:0>		PLLMULT<2:0>			0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK	LOCK	SLPEN	CF	UFRCEN	SOSCEN	OSWEN	0000
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					—	WDTCLR	0000
F600	RCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	0000
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

TABLE 4-21: PORT A REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
6010	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6020	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6030	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-22: PORT B REGISTERS MAP(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6040	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6050	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
6060	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
6070	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-23: PORT C REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-24: PORT C REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-25: PORT D REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-26: PORT D REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-27: PORT E REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-28: PORT E REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-29: PORT F REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L AND PIC32MX360F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	31FF
6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-30: PORT F REGISTERS MAP FOR PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-31: PORT F REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H AND PIC32MX340F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	07FF
6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-32: PORT F REGISTERS MAP FOR PIC32MX420F032H, PIC32MX440F128H AND PIC2MX440F256H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	03FF
6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-33: PORT G REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	TRISG1	TRISG0	F3CF
6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	RG1	RG0	xxxx
61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	LATG1	LATG0	xxxx
61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	ODCG1	ODCG0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-34: PORT G REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	—	—	03cc
6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	—	—	xxxx
61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	—	—	xxxx
61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-35: CHANGE NOTICE AND PULL-UP REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
61C0	CNCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
61D0	CNEN	31:16	—	—	—	—	—	—	—	—	—	—	CNEN21	CNEN20	CNEN19	CNEN18	CNEN17	CNEN16	0000
		15:0	CNEN15	CNEN14	CNEN13	CNEN12	CNEN11	CNEN10	CNEN9	CNEN8	CNEN7	CNEN6	CNEN5	CNEN4	CNEN3	CNEN2	CNEN1	CNEN0	0000
61E0	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	CNPUE21	CNPUE20	CNPUE19	CNPUE18	CNPUE17	CNPUE16	0000
		15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	CNPUE11	CNPUE10	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE1	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-36: CHANGE NOTICE AND PULL-UP REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
61C0	CNCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
61D0	CNEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CNEN18	CNEN17	CNEN16	0000
		15:0	CNEN15	CNEN14	CNEN13	CNEN12	CNEN11	CNEN10	CNEN9	CNEN8	CNEN7	CNEN6	CNEN5	CNEN4	CNEN3	CNEN2	CNEN1	CNEN0	0000
61E0	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUE18	CNPUE17	CNPUE16	0000
		15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	CNPUE11	CNPUE10	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE1	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-37: PARALLEL MASTER PORT REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	FRZ	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2EN/A15	CS1EN/A14	ADDR<13:0>														0000
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	0080

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-38: PROGRAMMING AND DIAGNOSTICS REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	TROEN	—	—	0008

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PREFETCH REGISTERS MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	CHECON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHECOH	0000
		15:0	—	—	—	—	—	—	DCSZ<1:0>		—	—	PREFEN<1:0>		—	PFMWS<2:0>			0000
4010	CHEACC(1)	31:16	CHEWEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CHEIDX<3:0>				00xx
4020	CHETAG(1)	31:16	LTAGBOOT	—	—	—	—	—	—	—	LTAG<23:16>								xxx0
		15:0	LTAG<15:4>												LVALID	LLOCK	LTYPE	—	0000
4030	CHEMSK(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LMASK<15:5>											—	—	—	—	—	xxxx
4040	CHEW0	31:16	CHEW0<31:0>																xxxx
		15:0																	xxxx
4050	CHEW1	31:16	CHEW1<31:0>																xxxx
		15:0																	xxxx
4060	CHEW2	31:16	CHEW2<31:0>																xxxx
		15:0																	xxxx
4070	CHEW3	31:16	CHEW3<31:0>																xxxx
		15:0																	xxxx
4080	CHELRU	31:16	—	—	—	—	—	—	—	CHELRU<24:16>									0000
		15:0	CHELRU<15:0>																0000
4090	CHEHIT	31:16	CHEHIT<31:0>																xxxx
		15:0																	xxxx
40A0	CHEMIS	31:16	CHEMIS<31:0>																xxxx
		15:0																	xxxx
40C0	CHEPFABT	31:16	CHEPFABT<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV Registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-40: RTCC REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<11:0>										0000
		15:0	ON	FRZ	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x
0240	ALRMTIME	31:16	MIN10<3:0>				MIN01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV Registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-41: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2FF0	DEVCFG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID15	USERID14	USERID13	USERID12	USERID11	USERID10	USERID9	USERID8	USERID7	USERID6	USERID5	USERID4	USERID3	USERID2	USERID1	USERID0	xxxx
2FF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	FUPLLEN(1)	—	—	—	—	FUPLLIDIV<2:0>(1)			—	FPLLMULT<2:0>			—	FPLLIDIV<2:0>			xxxx
2FF8	DEVCFG1	31:16	—	—	—	—	—	—	—	—	FWDTEN	—	—	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>			xxxx
2FFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	PWP19	PWP18	PWP17	PWP16	xxxx
		15:0	PWP15	PWP14	PWP13	PWP12	—	—	—	—	—	—	—	—	ICESEL	—	DEBUG<1:0>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are only available on PIC32MX4XX devices.

TABLE 4-42: DEVICE AND REVISION ID SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F220	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: USB REGISTERS MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTGIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTG STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000
5200	U1IR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
5240	U1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000
5280	U1FRML	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	FRML<7:0>								0000
5290	U1FRMH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	FRMH<10:8>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: USB REGISTERS MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
52A0	U1TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PID<3:0>				EP<3:0>				0000
52B0	U1SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>								0000
52C0	U1BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<7:0>								0000
52D0	U1BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<7:0>								0000
52E0	U1CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	USBFRZ	USBSIDL	—	—	—	—	0000
5300	U1EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5310	U1EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5320	U1EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5330	U1EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340	U1EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5350	U1EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5360	U1EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5370	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5380	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: USB REGISTERS MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS61121) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

PIC32MX3XX/4XX devices contain an internal program Flash memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self Programming (RTSP)
- In-Circuit Serial Programming™ (ICSP™)
- EJTAG Programming

RTSP is performed by software executing from either Flash or RAM memory. EJTAG is performed using the EJTAG port of the device and a EJTAG capable programmer. ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP. RTSP techniques are described in this chapter. The ICSP and EJTAG methods are described in the "*PIC32MX3XX/4XX Programming Specification*" (DS61145), which may be downloaded from the Microchip web site.

NOTES:

6.0 RESETS

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS61118) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

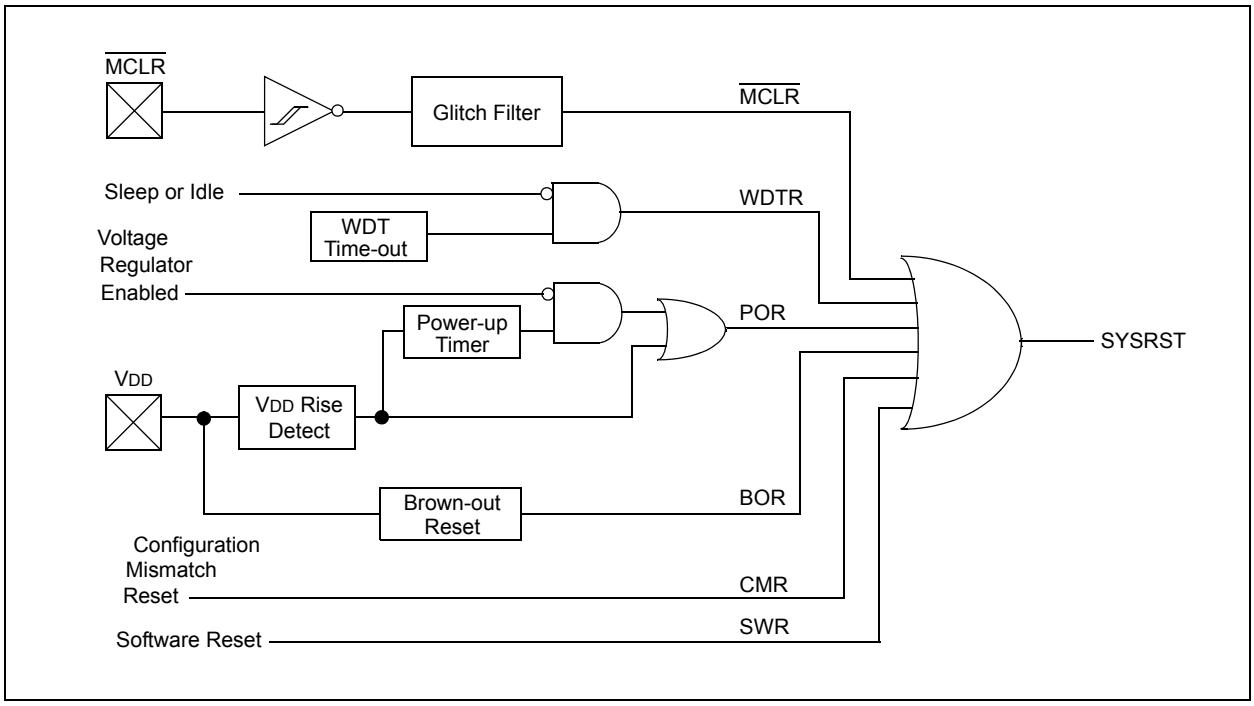
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Reset Pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



NOTES:

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS61108) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

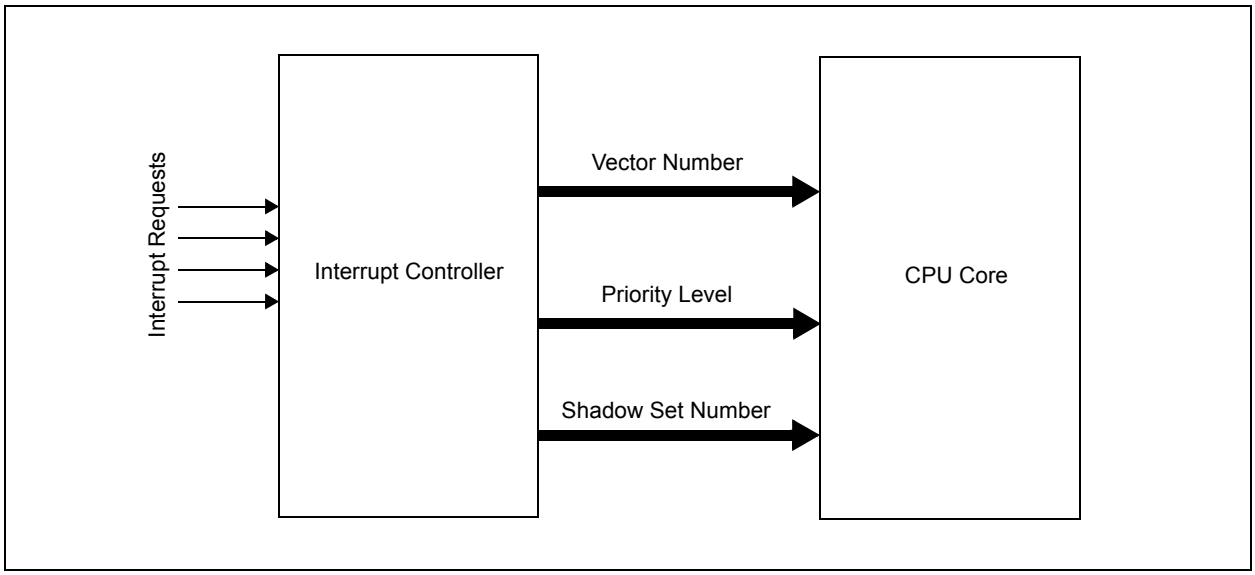
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

PIC32MX3XX/4XX devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX3XX/4XX interrupts module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and Multi-Vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Module Freeze in Debug mode
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Dedicated shadow set for highest priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

FIGURE 7-1: INTERRUPT CONTROLLER MODULE



Note: Several of the registers cited in this section are not in the interrupt controller module. These registers (and bits) are associated with the CPU. Details about them are available in **Section 3.0 "PIC32MX MCU"**.

To avoid confusion, a typographic distinction is made for registers in the CPU. The register names in this section, and all other sections of this manual, are signified by uppercase letters only. The CPU register names are signified by upper and lowercase letters. For example, INTSTAT is an Interrupts register; whereas, IntCtl is a CPU register.

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source(1)	IRQ	Vector Number	Interrupt Bit Location			
Highest Natural Order Priority			Flag	Enable	Priority	Subpriority
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: **"PIC32MX General Purpose – Features"** and TABLE 2: **"PIC32MX USB – Features"** for available peripherals.

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION (CONTINUED)

Interrupt Source(1)	IRQ	Vector Number	Interrupt Bit Location			
Highest Natural Order Priority			Flag	Enable	Priority	Subpriority
SPI2E – SPI2 Fault	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>
SPI2TX – SPI2 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>
SPI2RX – SPI2 Receive Done	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>
U2E – UART2 Error	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>
U2RX – UART2 Receiver	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>
U2TX – UART2 Transmitter	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>
RTCC – Real-Time Clock and Calendar	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>
USB	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>
Lowest Natural Order Priority						

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: **"PIC32MX General Purpose – Features"** and TABLE 2: **"PIC32MX USB – Features"** for available peripherals.

NOTES:

8.0 OSCILLATOR CONFIGURATION

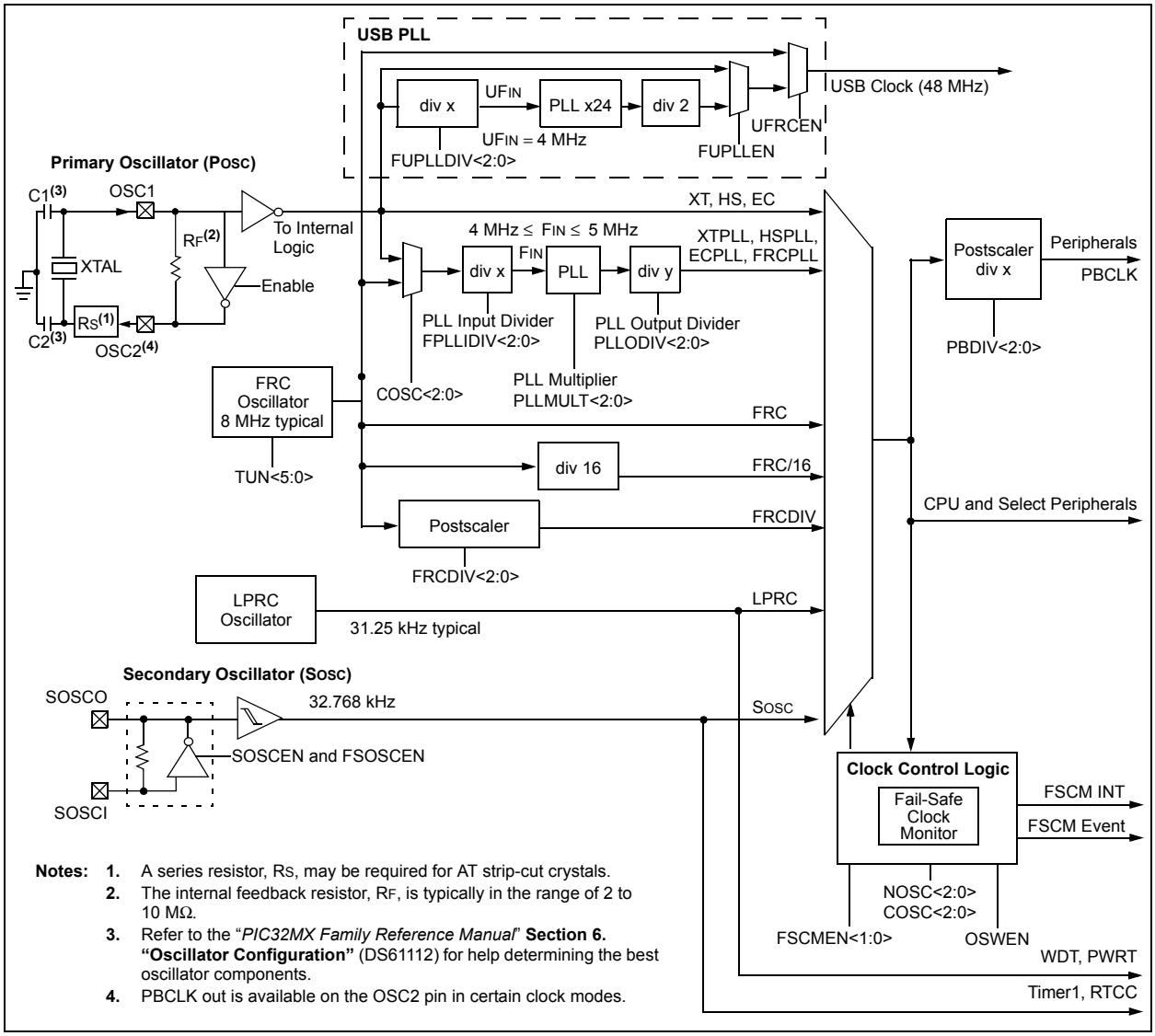
Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32MX Family Reference Manual"* **Section 6. "Oscillator Configuration"** (DS61112), which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC32MX oscillator system has the following modules and features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL (phase-locked loop) with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shut down
- Dedicated on-chip PLL for USB peripheral

FIGURE 8-1: PIC32MX3XX/4XX FAMILY CLOCK DIAGRAM



Notes:
1. A series resistor, RS, may be required for AT strip-cut crystals.
2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3. Refer to the "*PIC32MX Family Reference Manual*" **Section 6. "Oscillator Configuration"** (DS61112) for help determining the best oscillator components.
4. PBCLK out is available on the OSC2 pin in certain clock modes.

NOTES:

9.0 PREFETCH CACHE

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache"** (DS61119) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

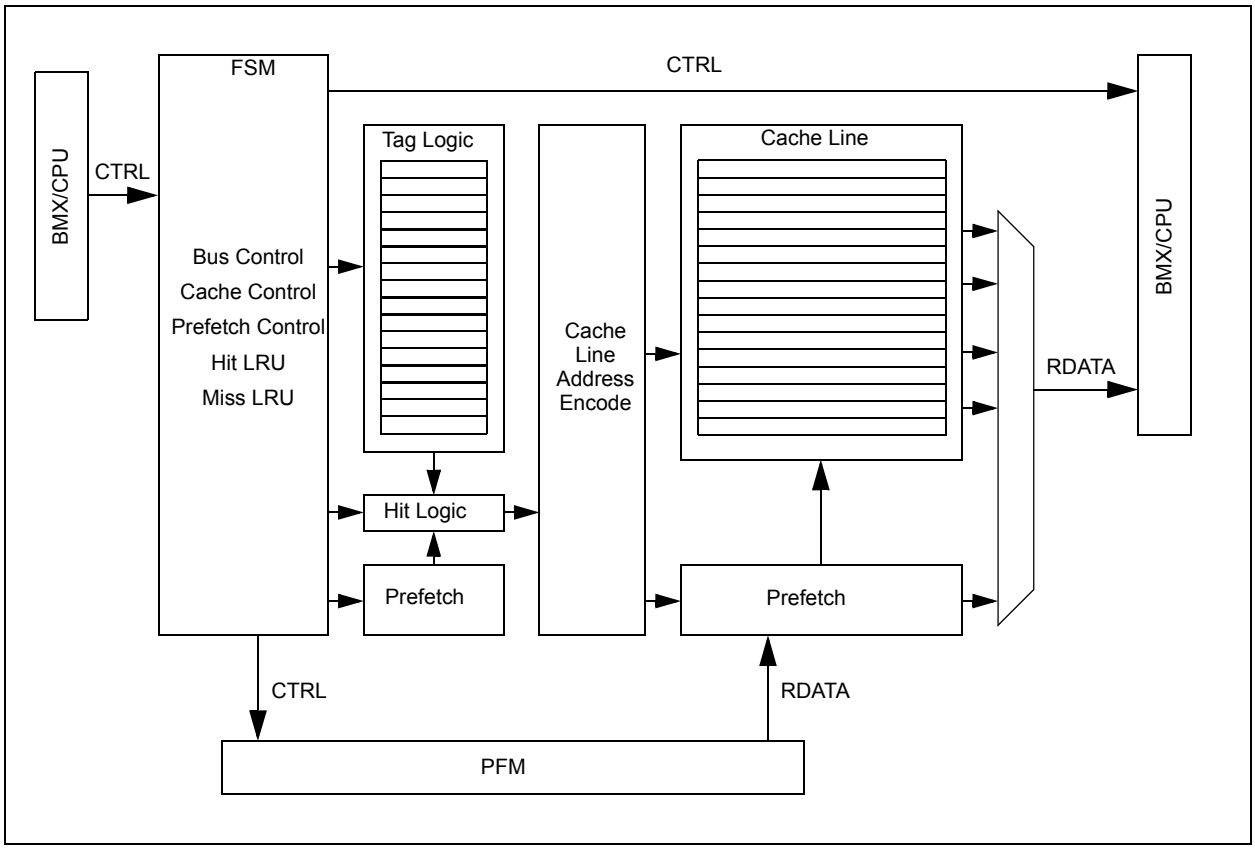
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

9.1 Features

- 16 Fully Associative Lockable Cache Lines
- 16-byte Cache Lines
- Up to four Cache Lines Allocated to Data
- Two Cache Lines with Address Mask to hold repeated instructions
- Pseudo LRU replacement policy
- All Cache Lines are software writable
- 16-byte parallel memory fetch
- Predictive Instruction Prefetch

FIGURE 9-1: PREFETCH MODULE BLOCK DIAGRAM



NOTES:

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS61117) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

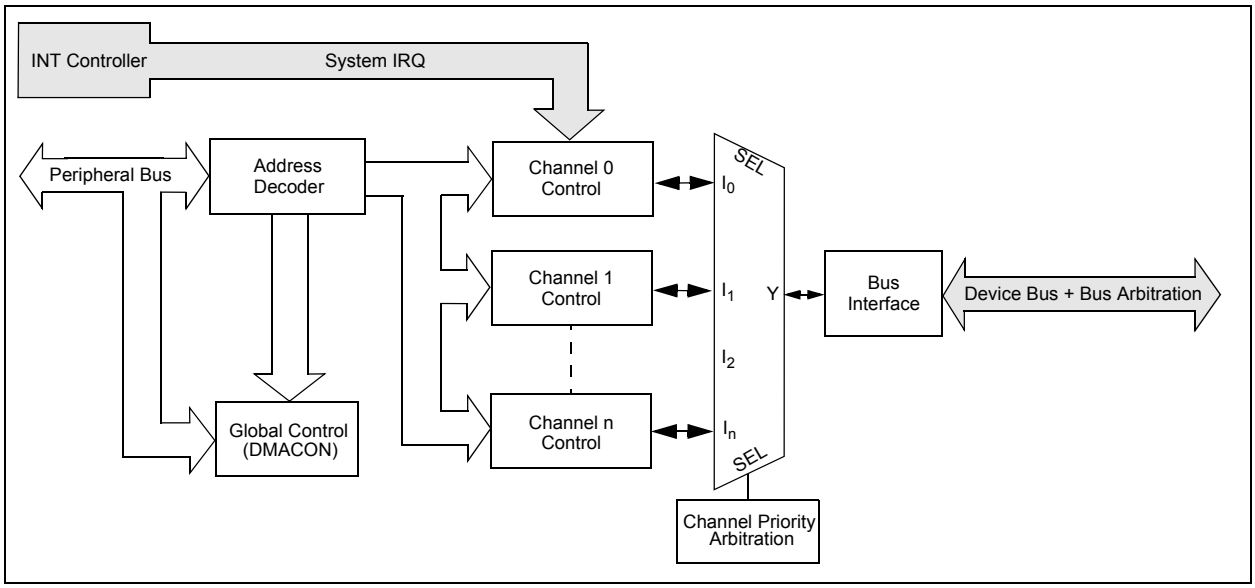
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC32MX Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32MX (such as Peripheral Bus (PBUS) devices: SPI, UART, I^2C™, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four Identical Channels, each featuring:
  - Auto-Increment Source and Destination Address Registers
  - Source and Destination Pointers
  - Memory to Memory and Memory to Peripheral Transfers
- Automatic Word-Size Detection:
  - Transfer Granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating Modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA Requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half-full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA Debug Support Features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation Module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



NOTES:

11.0 USB ON-THE-GO (OTG)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS61126) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device, or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32MX USB OTG module is presented in Figure 11-1.

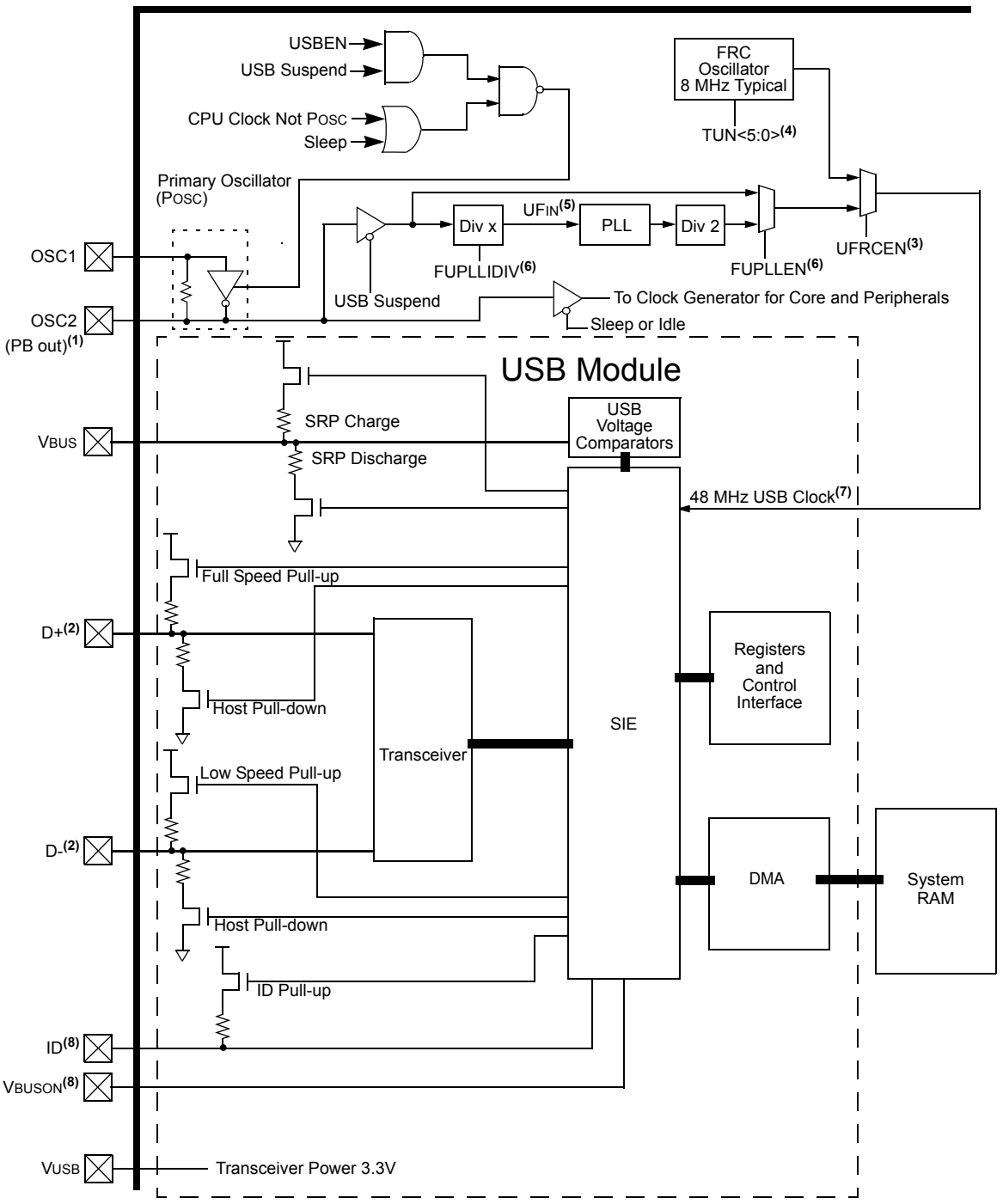
The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32MX USB module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Host Support
- USB OTG Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Transaction Handshaking Performed by Hardware
- Endpoint Buffering Anywhere in System RAM
- Integrated DMA to Access System RAM and Flash

Note: The implementation and use of the USB specifications, as well as other third-party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

FIGURE 11-1: PIC32MX3XX/4XX FAMILY USB INTERFACE DIAGRAM



Note 1: PB clock is only available on this pin for select EC modes.
2: Pins can be used as digital inputs when USB is not enabled.
3: This bit field is contained in the OSCCON register.
4: This bit field is contained in the OSCTRM register.
5: USB PLL UFIN requirements: 4 MHz.
6: This bit field is contained in the DEVCFG2 register.
7: A 48 MHz clock is required for proper USB operation.
8: Pins can be used as GPIO when the USB module is disabled.

12.0 I/O PORTS

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS61120) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

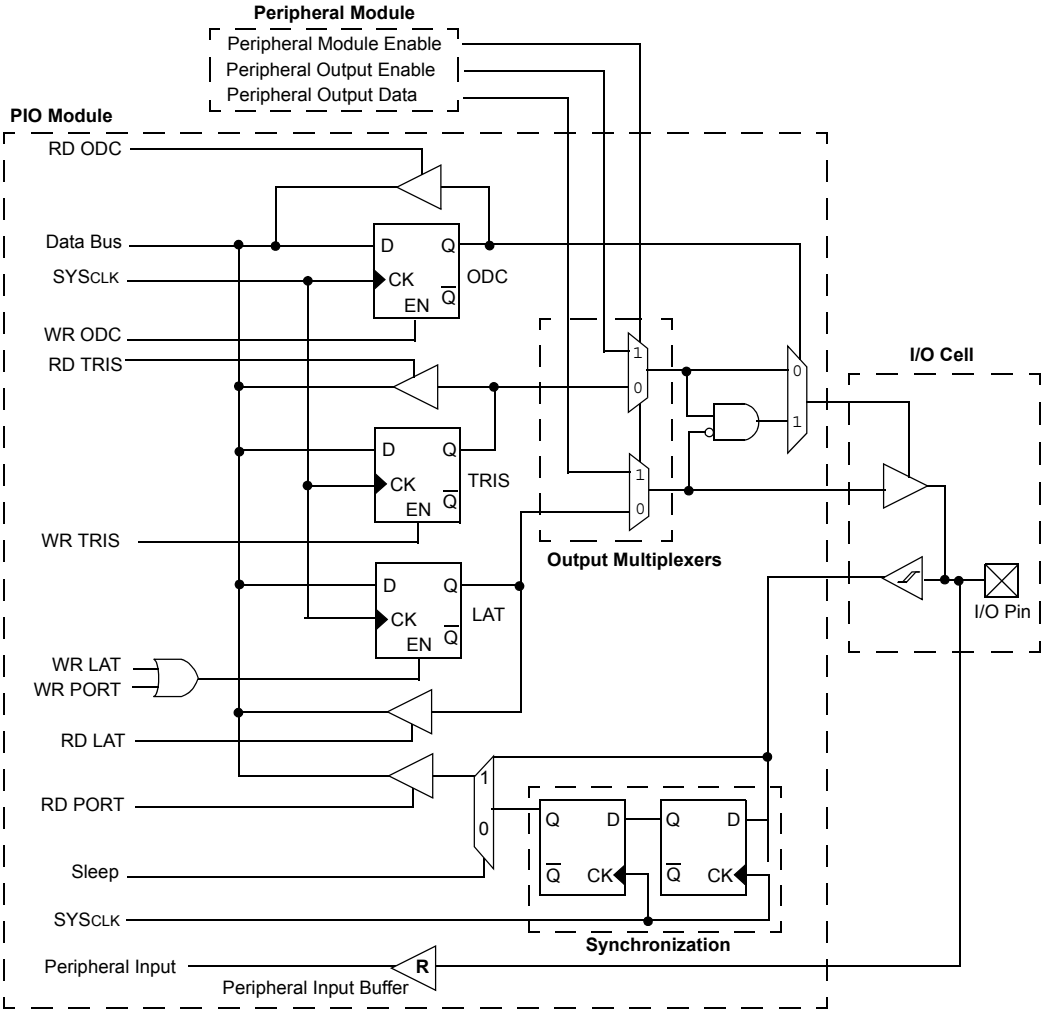
General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Following are some of the key features of this module:

- Individual Output Pin Open-drain Enable/Disable
- Individual Input Pin Weak Pull-up Enable/Disable
- Monitor Selective Inputs and Generate Interrupt when Change in Pin State is Detected
- Operation during CPU Sleep and Idle modes
- Fast Bit Manipulation using CLR, SET and INV Registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to **Table 1-1 "Pinout I/O Descriptions"** for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than it is shown here.

12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT and PORT) that are directly associated with their operation.

TRIS is a data direction or tri-state control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1 configures the corresponding I/O pin as an input; setting a TRISx register bit = 0 configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx latch register holds the data written to either the LATx or PORTx registers. Reading the LATx latch register reads the last value written to the corresponding port or latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

Note:	Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions as compared to the traditional read-modify-write method shown below: PORTC ^= 0x0001;

12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

The maximum input voltage allowed on the input pins is the same as the maximum V_{IH} specification. Refer to **Section 29.0 "Electrical Characteristics"** for V_{IH} specification details.

Note:	Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and Comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level (V_{OH} or V_{OL}) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG Register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open drain outputs by setting the corresponding bits in the ODCx Open-Drain Configuration register.

The open-drain feature allows the generation of outputs higher than V_{DD} (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

See the **"Pin Diagrams"** section for the available pins and their functionality.

12.1.5 ANALOG OUTPUTS

Certain pins can be configured as analog outputs, such as the CV_{REF} output voltage used by the comparator module. Configuring the Comparator Reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

12.1.6 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports (CNx) allows devices to generate interrupt requests in response to change of state on selected pin.

Each CNx pin also has a weak pull-up, which acts as a current source connected to the pin. The pull-ups are enabled by setting corresponding bit in CNPUE register.

13.0 TIMER1

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS61105) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

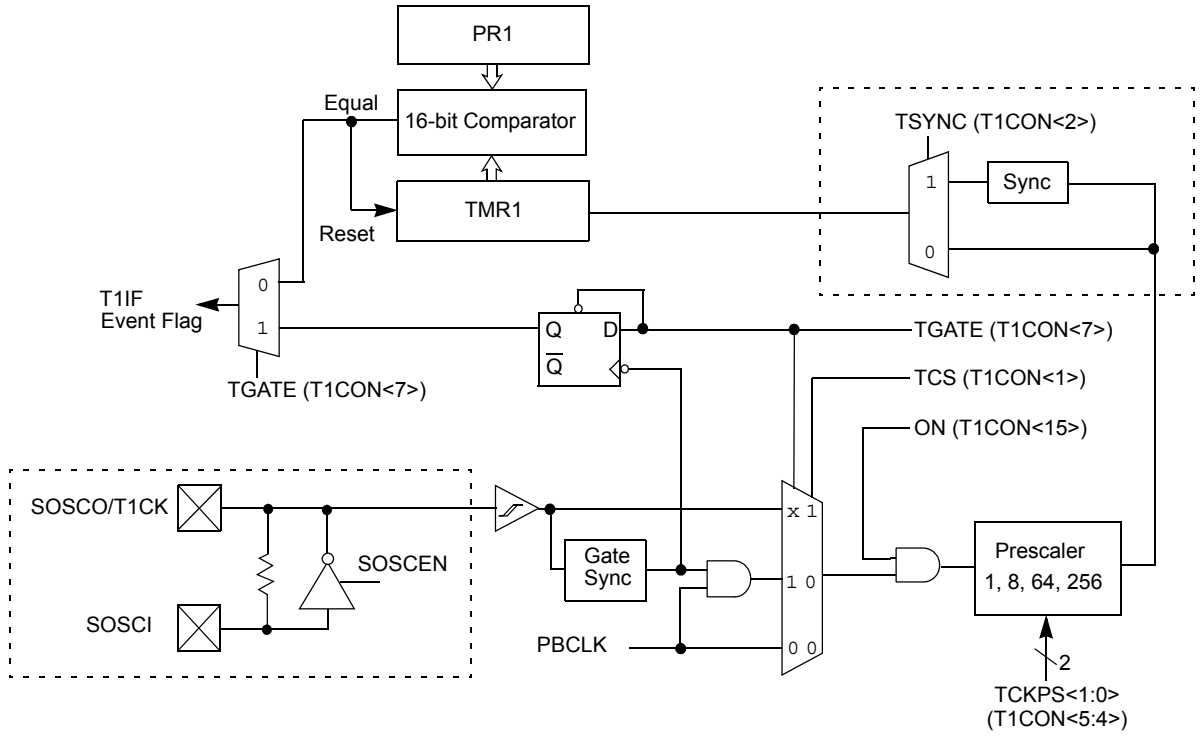
This family of PIC32MX devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Secondary Oscillator (SOSC) for real-time clock applications. The following modes are supported:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a Real-Time Clock (RTC)

FIGURE 13-1: TIMER1 BLOCK DIAGRAM(1)



Note 1: The default state of the SOSCEN (OSCCON<1>) during a device Reset is controlled by the FSOSCEN bit in Configuration Word DEVCFG1.

NOTES:

14.0 TIMERS 2, 3, 4, 5

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS61105) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This family of PIC32MX devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-bit Timer
- Synchronous Internal 16-bit Gated Timer
- Synchronous External 16-bit Timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

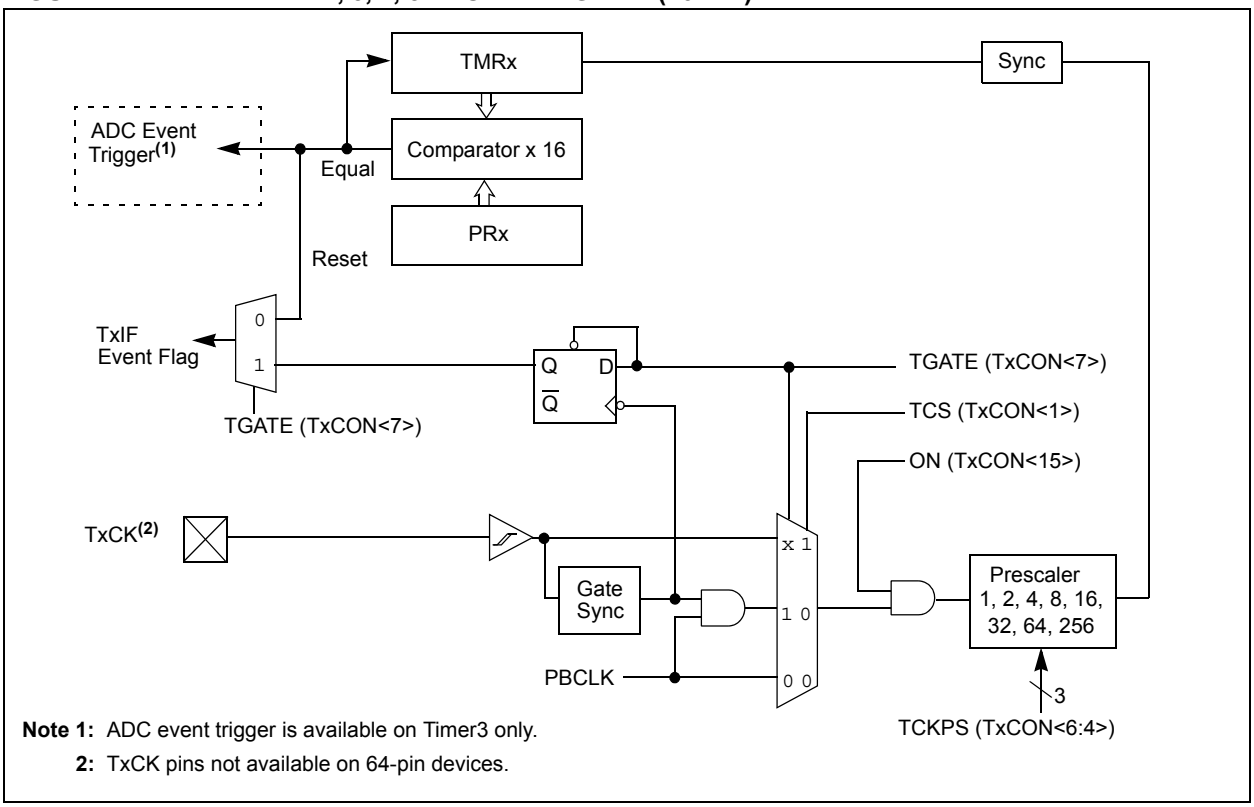
- Synchronous Internal 32-bit Timer
- Synchronous Internal 32-bit Gated Timer
- Synchronous External 32-bit Timer

Note: Throughout this chapter, references to registers TxCON, TMRx and PRx use 'x' to represent Timer2 through 5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or 4; 'y' represents Timer3 or 5.

14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU Idle
- Time base for input capture and output compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 only)
- Fast bit manipulation using CLR, SET and INV registers

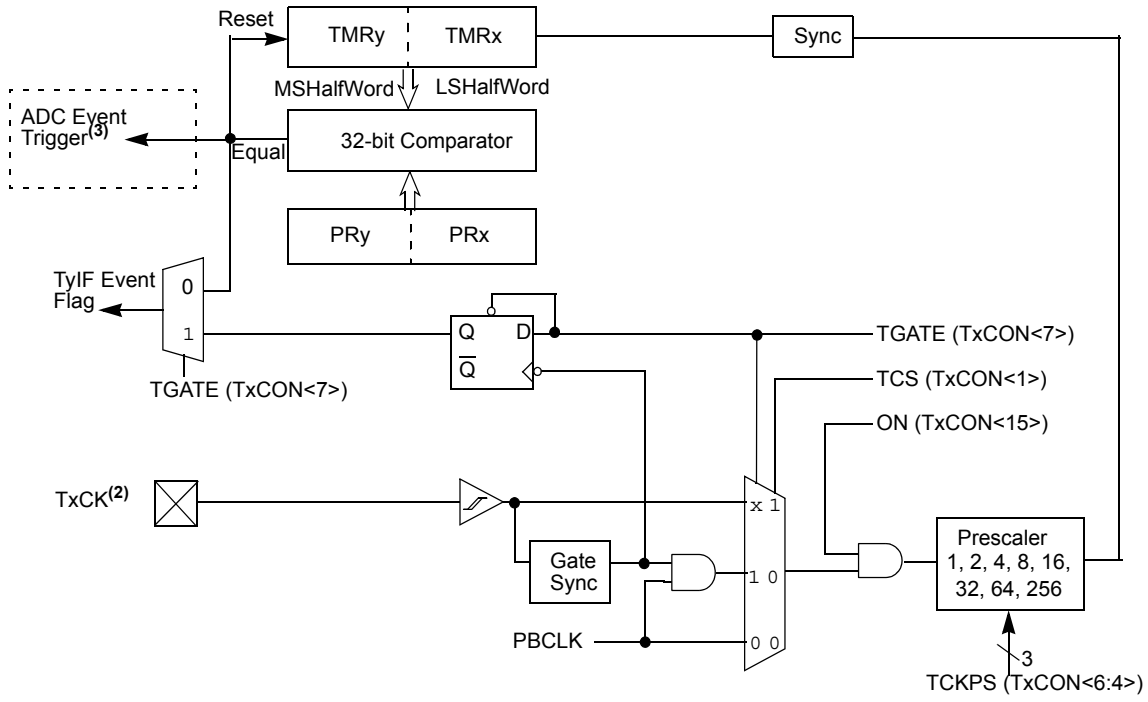
FIGURE 14-1: TIMER2, 3, 4, 5 BLOCK DIAGRAM (16-BIT)



Note 1: ADC event trigger is available on Timer3 only.

2: TxCK pins not available on 64-pin devices.

FIGURE 14-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)



Note 1: In this diagram, the use of 'x' in registers TxCON, TMRx, PRx and TxCK refers to either Timer2 or Timer4; the use of 'y' in registers TyCON, TMRy, PRy and TyIF refers to either Timer3 or Timer5.

2: TxCK pins are not available on 64-pin devices.

3: ADC event trigger is available only on Timer2/3 pair.

15.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS61122) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The PIC32MX3XX/4XX devices support up to five input capture channels.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

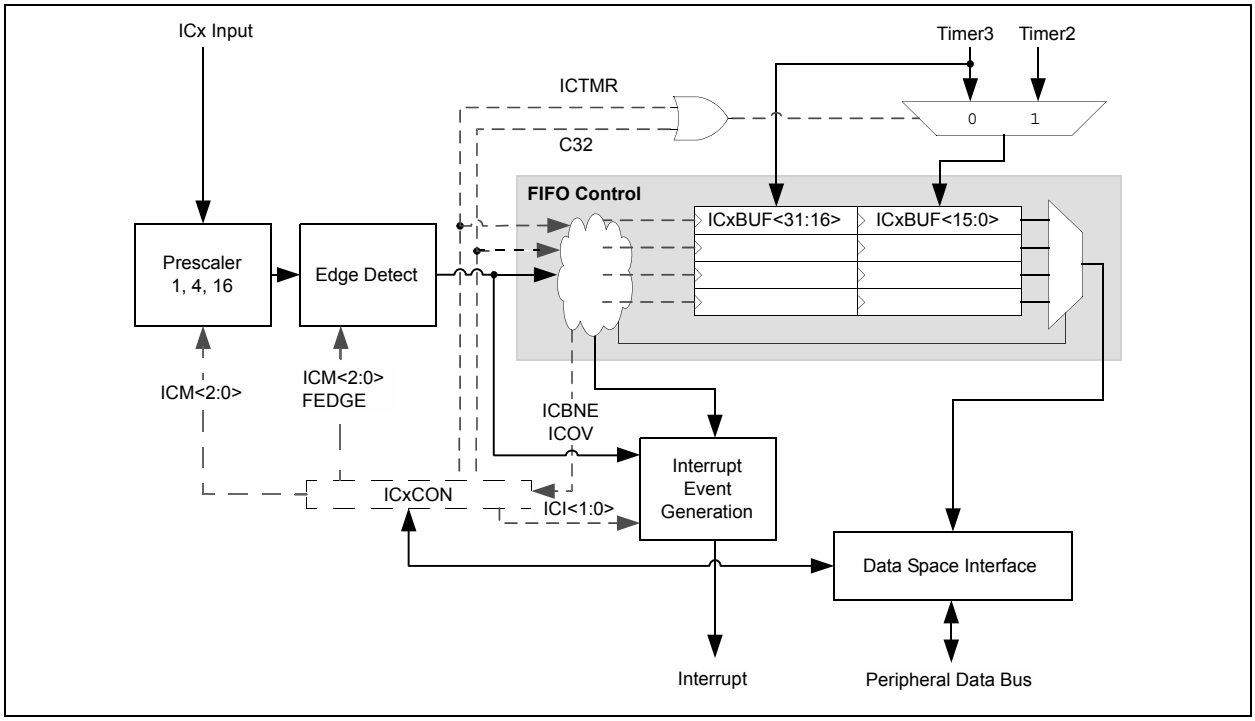
1. Simple Capture Event modes
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling)
3. Capture timer value on every edge (rising and falling), specified edge first.
4. Prescaler Capture Event modes
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



NOTES:

16.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Capture"** (DS61111) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

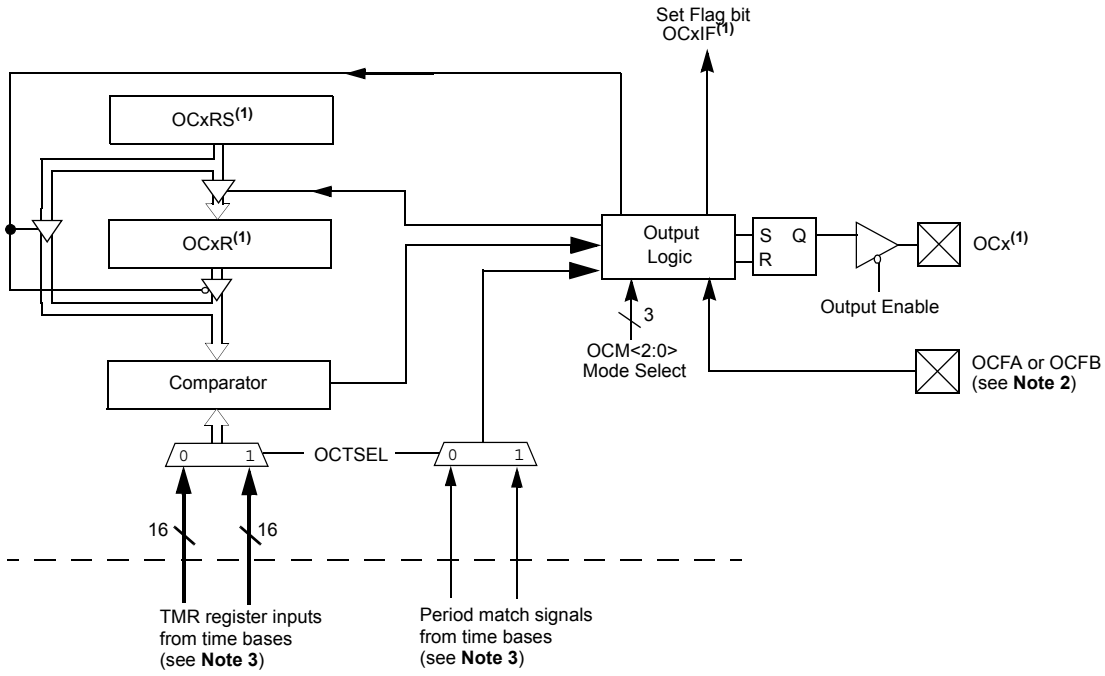
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Output Compare module (OCMP) is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the OCMP module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the OCMP module generates an event based on the selected mode of operation.

The following are some of the key features:

- Multiple output compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases.
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels 1 through 5.

2: The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

3: Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit timer base.

NOTES:

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

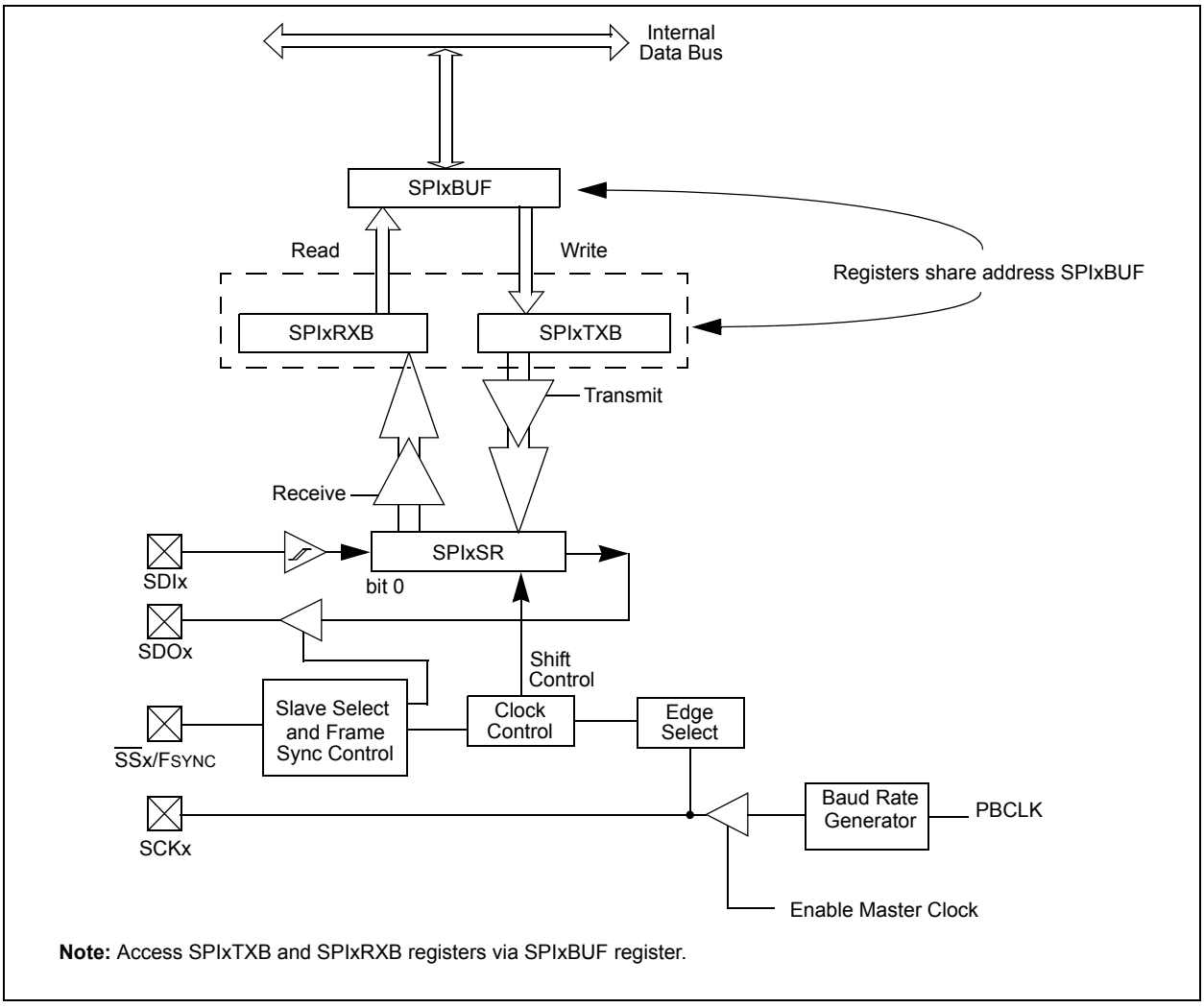
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The PIC32MX SPI module is compatible with Motorola® SPI and SIOP interfaces.

Following are some of the key features of this module:

- Master and Slave Modes Support
- Four Different Clock Formats
- Framed SPI Protocol Support
- User Configurable 8-bit, 16-bit and 32-bit Data Width
- Separate SPI Data Registers for Receive and Transmit
- Programmable Interrupt Event on every 8-bit, 16-bit and 32-bit Data Transfer
- Operation during CPU Sleep and Idle Mode
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 17-1: SPI MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB registers via SPIxBUF register.

NOTES:

18.0 INTER-INTEGRATED CIRCUIT (I^2C™)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C™)"** (DS61116) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

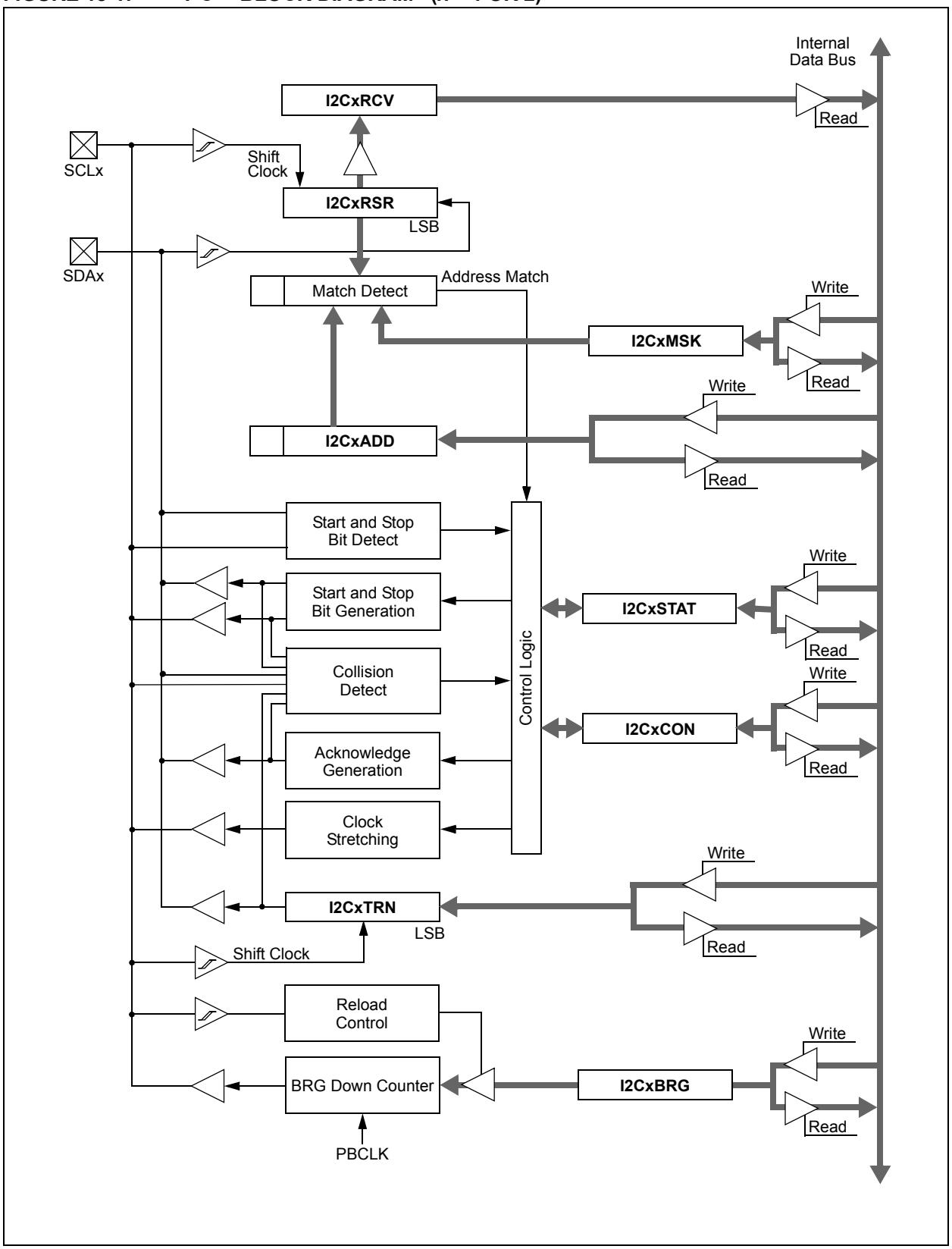
The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 18-1 illustrates the I^2C module block diagram.

The PIC32MX3XX/4XX devices have up to two I^2C interface modules, denoted as I2C1 and I2C2. Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I^2C module, 'I2Cx' (x = 1 or 2), offers the following key features:

- I^2C Interface Supporting both Master and Slave Operation.
- I^2C Slave Mode Supports 7 and 10-bit Address.
- I^2C Master Mode Supports 7 and 10-bit Address.
- I^2C Port allows Bidirectional Transfers between Master and Slaves.
- Serial Clock Synchronization for I^2C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I^2C Supports Multi-master Operation; Detects Bus Collision and Arbitrates Accordingly.
- Provides Support for Address Bit Masking.

FIGURE 18-1: I²C™ BLOCK DIAGRAM (x = 1 OR 2)



19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS61107) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The UART module is one of the serial I/O modules available in PIC32MX3XX/4XX family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 4-level-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-level-deep FIFO Receive Data Buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN 1.2 protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART.

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM

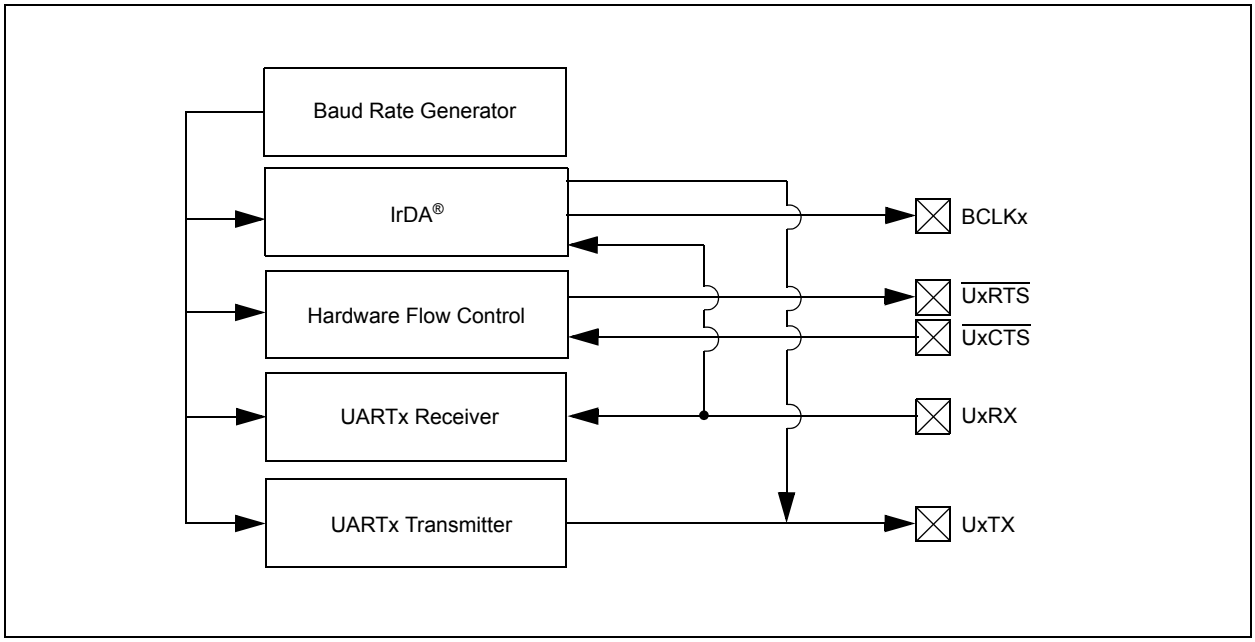


FIGURE 19-2: TRANSMISSION (8-BIT OR 9-BIT DATA)

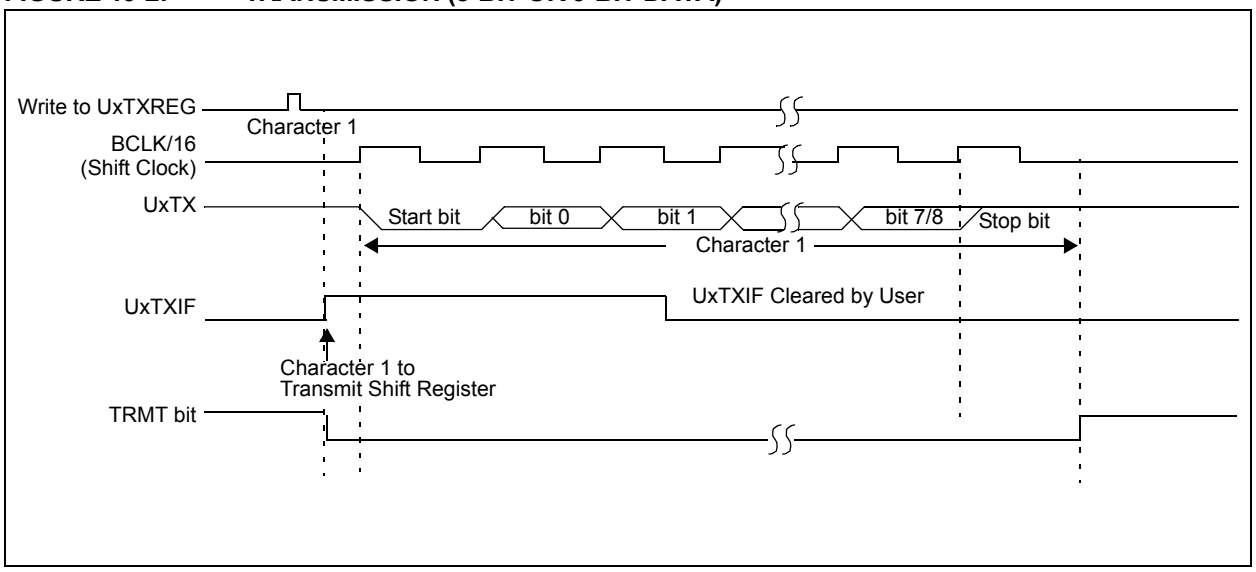


FIGURE 19-3: TWO CONSECUTIVE TRANSMISSIONS

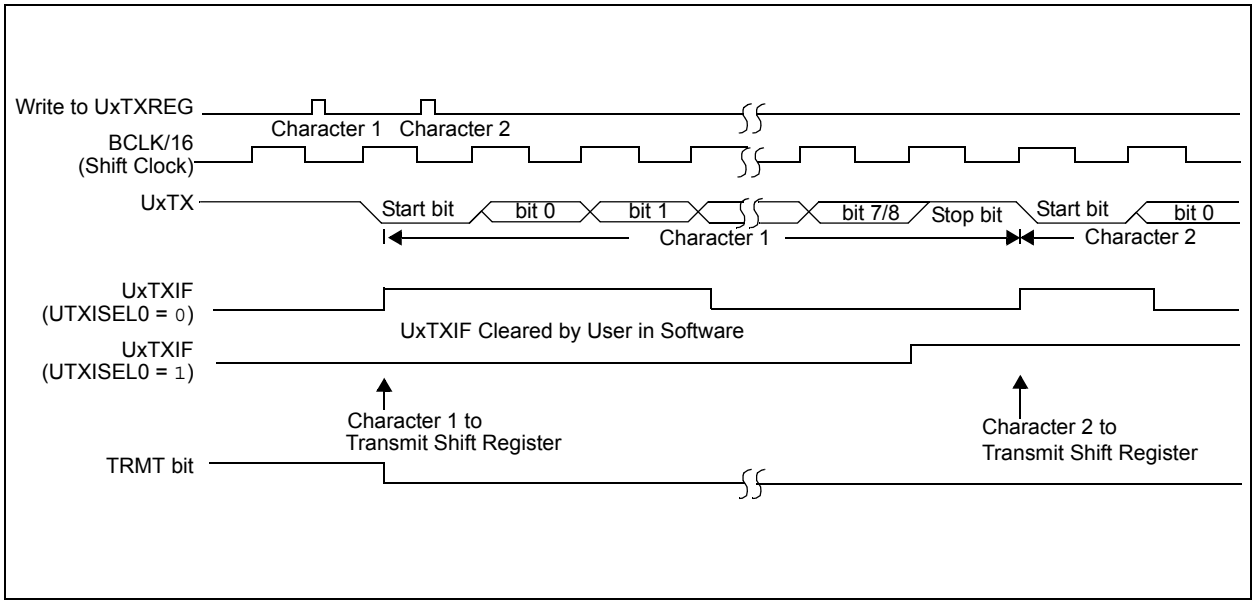
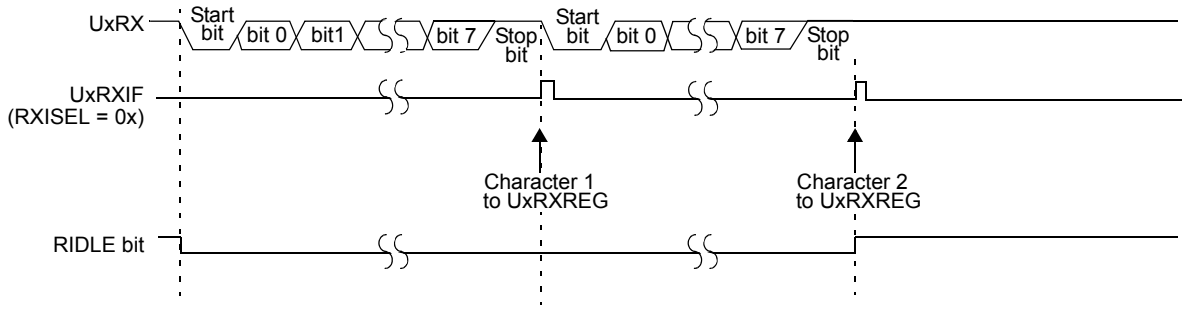
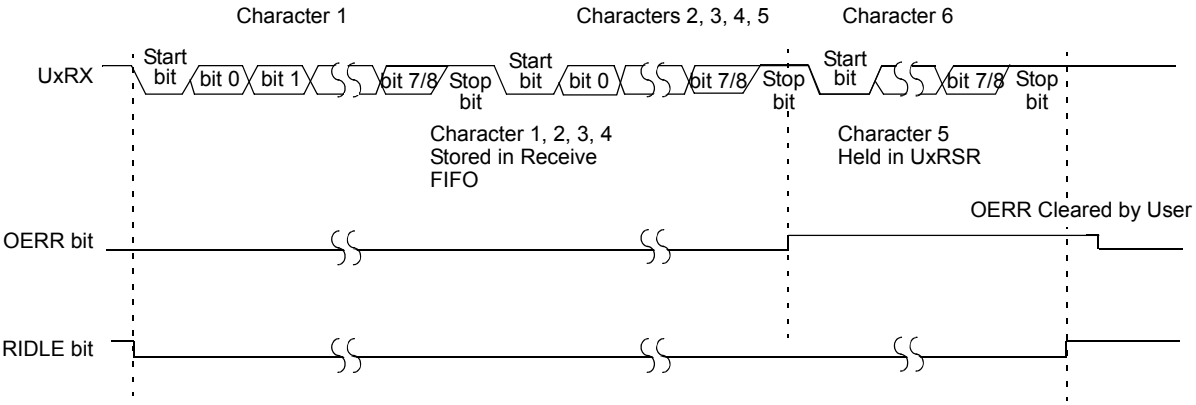


FIGURE 19-4: UART RECEPTION



Note: This timing diagram shows 2 characters received on the UxRX input.

FIGURE 19-5: UART RECEPTION WITH RECEIVE OVERRUN



Note: This diagram shows 6 characters received without the user reading the input buffer. The 5th character received is held in the Receive Shift register. An overrun error occurs at the start of the 6th character.

NOTES:

20.0 PARALLEL MASTER PORT (PMP)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS61128) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

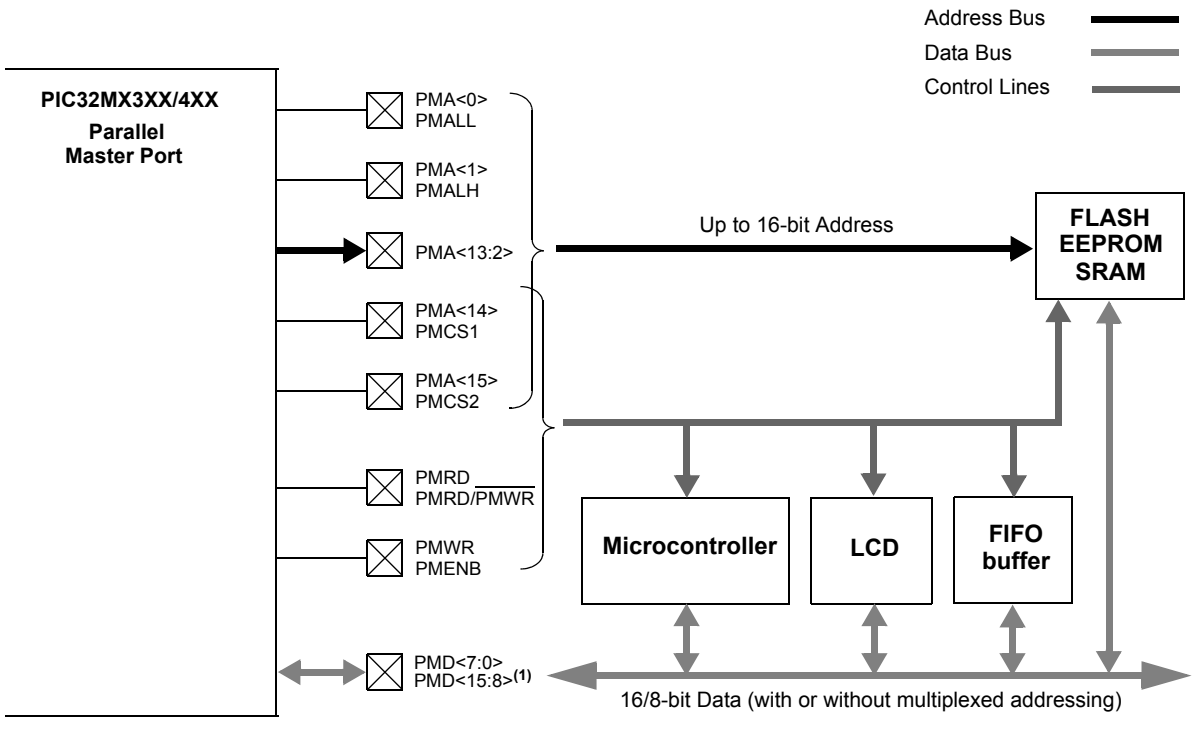
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
  - Individual read and write strobes, or
  - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
  - Legacy addressable
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> are not available.

FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Note 1: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

NOTES:

21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

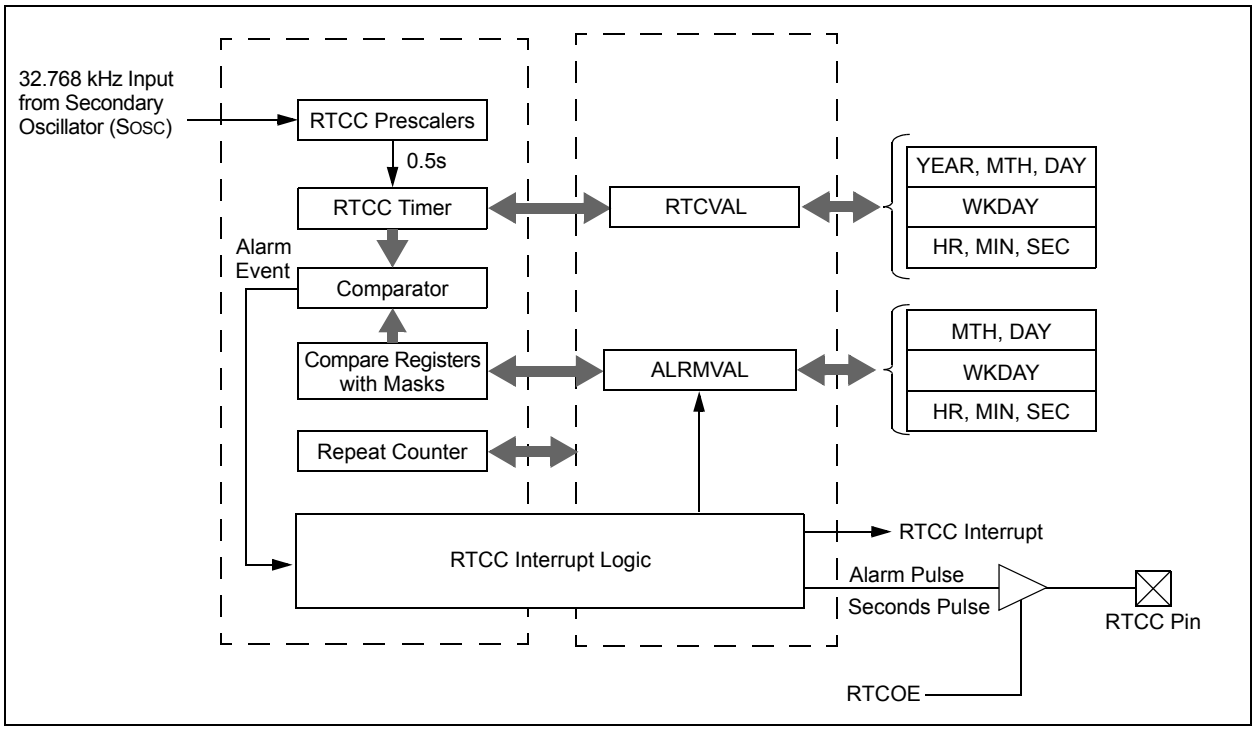
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC32MX RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are some of the key features of this module:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (Military Time)
- Visibility of One-Half-Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are configurable for Half of a Second, One Second, 10 Seconds, One Minute, 10 Minutes, One Hour, One Day, One Week, One Month and One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Calibration Range: ±0.66 Seconds Error per Month
- Calibrates up to 260 ppm of Crystal Error
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC pin

FIGURE 21-1: RTCC BLOCK DIAGRAM



NOTES:

22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS61104) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC32MX3XX/4XX 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1000 kilo samples per second (ksps) conversion speed
- Up to 16 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample-and-Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable Buffer Fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

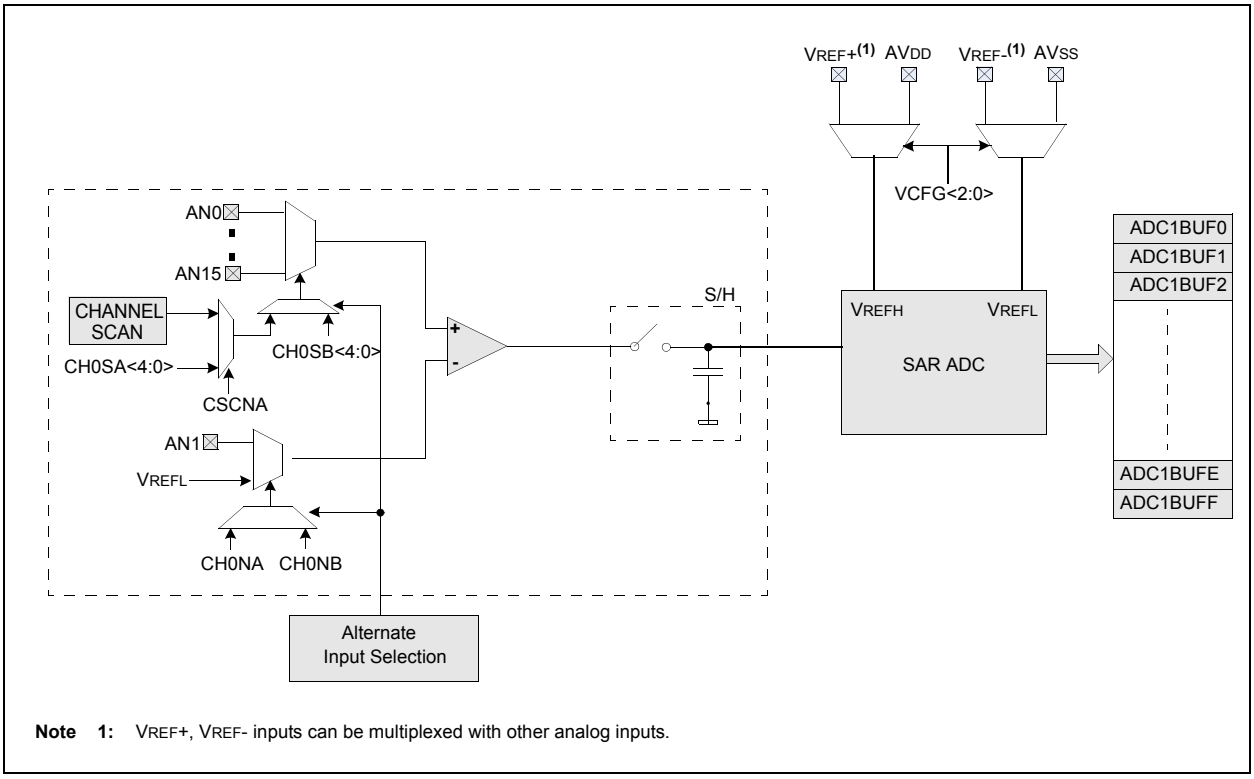
A block diagram of the 10-bit ADC is illustrated in Figure 22-1. The 10-bit ADC has 16 analog input pins, designated AN0-AN15. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

The analog inputs are connected through two multiplexers (MUXs) to one SHA. The analog input MUXs can be switched between two sets of analog inputs between conversions. Unipolar differential conversions are possible on all channels, other than the pin used as the reference, using a reference input pin (see Figure 22-1).

The Analog Input Scan mode sequentially converts user-specified channels. A control register specifies which analog input channels will be included in the scanning sequence.

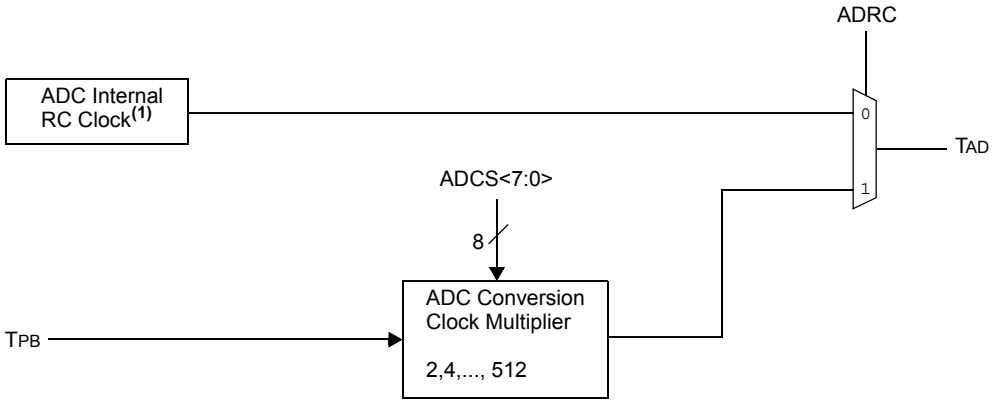
The 10-bit ADC is connected to a 16-word result buffer. Each 10-bit result is converted to one of eight, 32-bit output formats when it is read from the result buffer.

FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM



Note 1: VREF+, VREF- inputs can be multiplexed with other analog inputs.

FIGURE 22-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: See the ADC electrical characteristics for the exact RC clock value.

23.0 COMPARATOR

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to **Section 19. "Comparator"** (DS61110) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

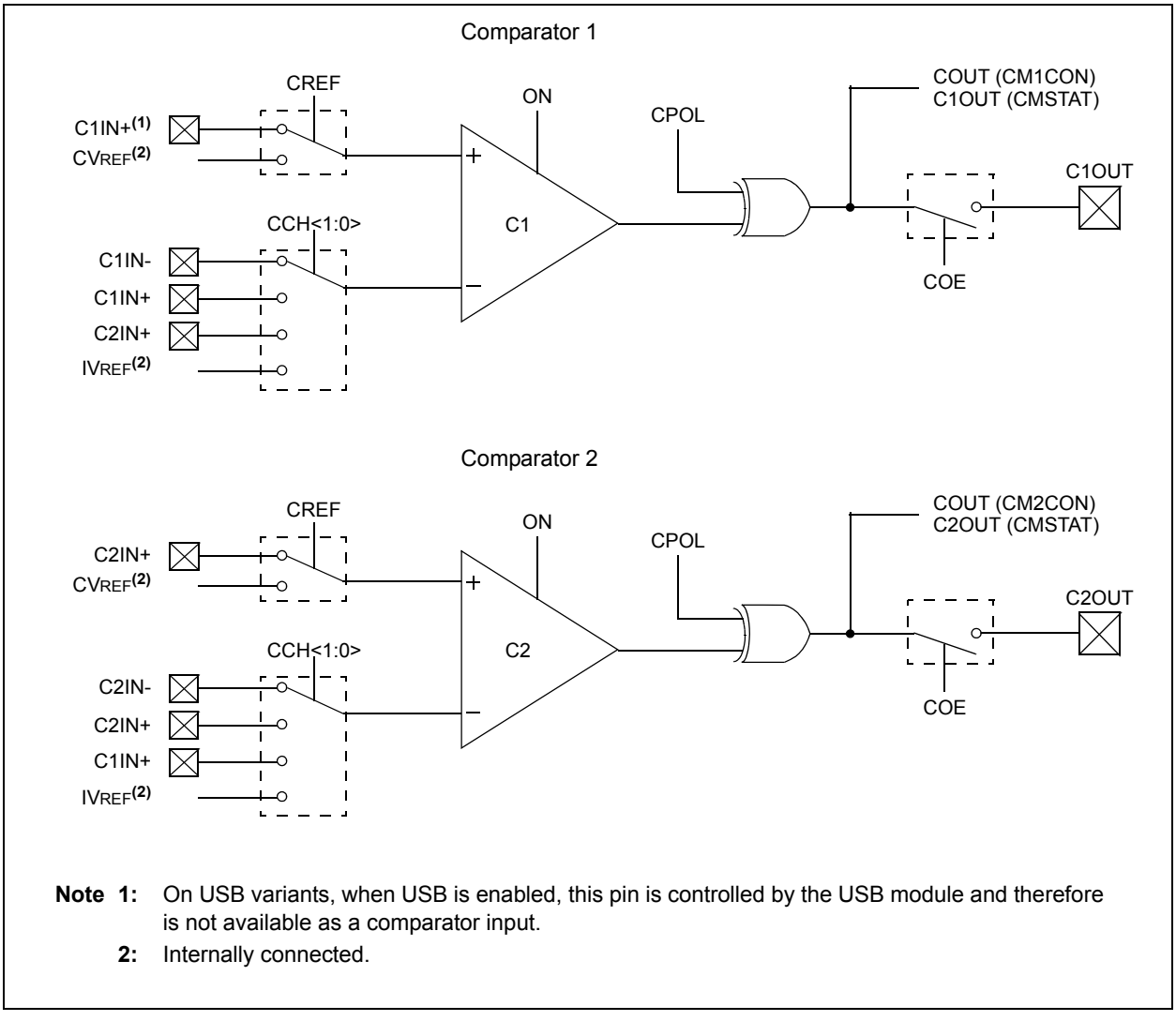
The PIC32MX3XX/4XX Analog Comparator module contains one or more comparator(s) that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IV_{REF})
  - Comparator voltage reference (CV_{REF})
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 23-1.

FIGURE 23-1: COMPARATOR BLOCK DIAGRAM



Note 1: On USB variants, when USB is enabled, this pin is controlled by the USB module and therefore is not available as a comparator input.

2: Internally connected.

NOTES:

24.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS61109) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

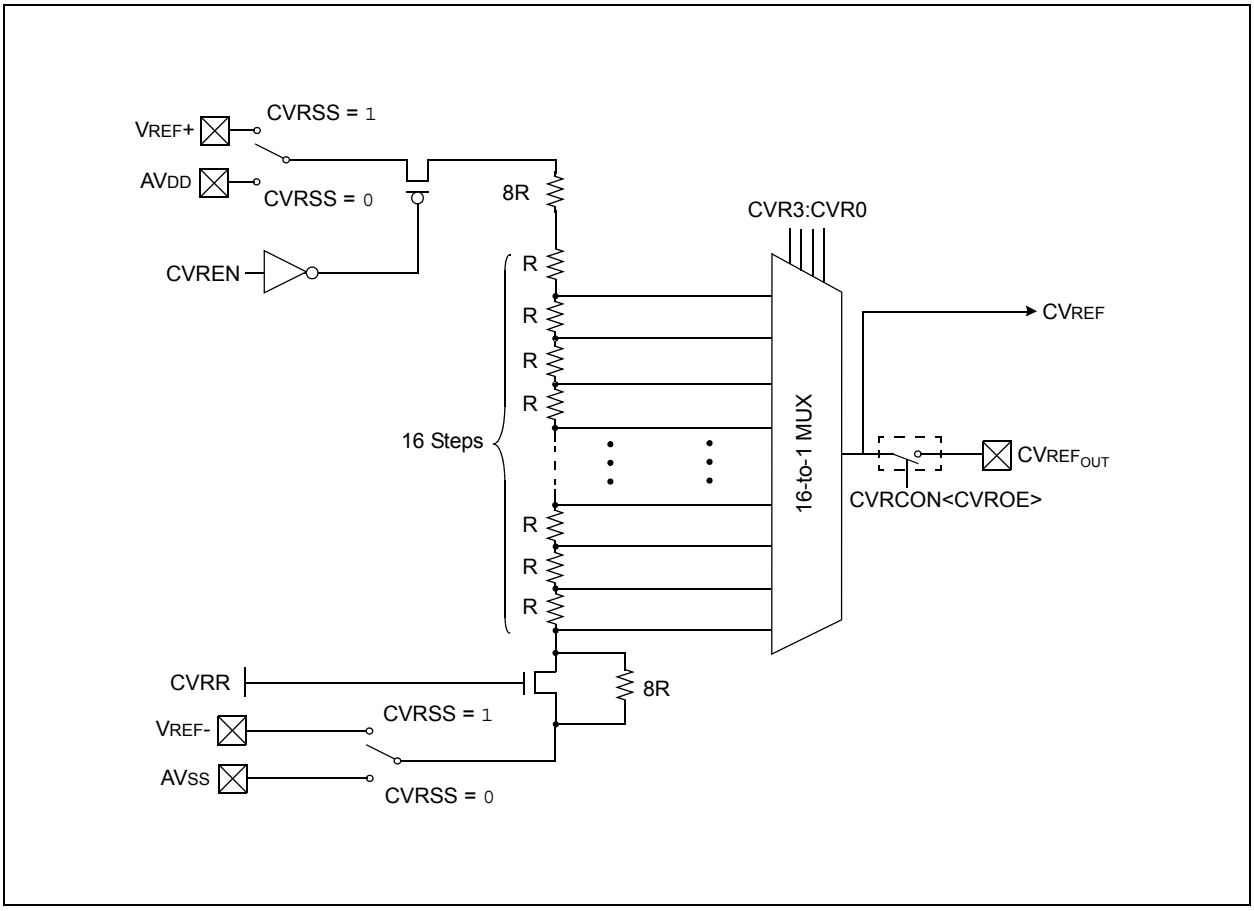
The CVREF is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 24-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

FIGURE 24-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



NOTES:

25.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS61130) of the *"PIC32MX Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This section describes power-saving for the PIC32MX3XX/4XX. The PIC32MX devices offer a total of nine methods and modes that are organized into two categories that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

25.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK, and by individually disabling modules. These methods are grouped into the following modes:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.
- Peripheral Bus Scaling mode: peripherals are clocked at programmable fraction of the CPU clock (SYSCLK).

25.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- POSC Idle Mode: the system clock is derived from the POSC. The system clock source continues to operate.

  Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle Mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle Mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle Mode: the system clock is derived from the LPRC.

  Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep Mode: the CPU, the system clock source, and any peripherals that operate from the system clock source, are halted.

  Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

25.3 Power-Saving Operation

The purpose of all power-saving is to reduce power consumption by reducing the device clock frequency. To achieve this, low-frequency clock sources can be selected. In addition, the peripherals and CPU can be halted or disabled to further reduce power consumption.

25.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device Power-Saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- The CPU is halted.
- The system clock source is typically shut down. See **Section 25.3.2 "Idle Mode"** for specific information.
- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit, if enabled, remains operative during Sleep mode.
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode.
- Some peripherals can continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator, e.g., RTCC and Timer 1.
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The USB module can override the disabling of the POSC or FRC. Refer to **Section 11.0 "USB On-The-Go (OTG)"** for specific details.
- Some modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption.

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out. See **Section 26.2 "Watchdog Timer (WDT)"**.

If the interrupt priority is lower than or equal to current priority, the CPU will remain halted, but the PBCLK will start running and the device will enter into Idle mode.

Note:	There is no FRZ mode for this module.

25.3.2 IDLE MODE

In the Idle mode, the CPU is halted but the System clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is halted. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency when exiting Idle mode is very low due to the CPU oscillator source remaining active.

Note:	Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in PB divisor ratio. Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator startup/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of CPU. If the priority of the interrupt event is lower than or equal to current priority of CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any source of device Reset.
- On a WDT time-out interrupt. See **Section 26.2 "Watchdog Timer (WDT)"**.

25.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK-to-PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as USB, Interrupt Controller, DMA, Bus Matrix and Prefetch Cache are clocked directly from SYSCLK, as a result, they are not affected by PBCLK divisor changes

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements such as baud rate accuracy should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

26.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"PIC32MX Family Reference Manual"* (DS61132), which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible Device Configuration
- Watchdog Timer
- JTAG Interface
- In-Circuit Serial Programming™ (ICSP™)

26.1 Configuration Bits

The Configuration bits can be programmed to select various device configurations.

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

r-0	r-1	r-1	R/P	r-1	r-1	r-1	R/P
—	—	—	CP	—	—	—	BWP
bit 31							bit 24

r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
—	—	—	—	PWP<7:4>			
bit 23							bit 16

R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
PWP<3:0>				—	—	—	—
bit 15							bit 8

r-1	r-1	r-1	r-1	R/P	r-1	R/P	R/P
—	—	—	—	ICESEL	—	DEBUG<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection disabled
0 = Protection enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 19-12 **PWP<7:0>:** Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages.

11111111 = Disabled
11111110 = 0xBD00_0FFF
11111101 = 0xBD00_1FFF
11111100 = 0xBD00_2FFF
11111011 = 0xBD00_3FFF
11111010 = 0xBD00_4FFF
11111001 = 0xBD00_5FFF
11111000 = 0xBD00_6FFF
11110111 = 0xBD00_7FFF
11110110 = 0xBD00_8FFF
11110101 = 0xBD00_9FFF
11110100 = 0xBD00_AFFF
11110011 = 0xBD00_BFFF
11110010 = 0xBD00_CFFF
11110001 = 0xBD00_DFFF
11110000 = 0xBD00_EFFF
11101111 = 0xBD00_FFFF
.
.
.
01111111 = 0xBD07_FFFF

bit 11-4 **Reserved:** Write '1'

bit 3 **ICESEL:** In-Circuit Emulator/Debugger Communication Channel Select bit

1 = PGEC2/PGED2 pair is used
0 = PGEC1/PGED1 pair is used

bit 2 **Reserved:** Write '1'

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = Debugger disabled
10 = Debugger enabled
01 = Reserved (same as '11' setting)
00 = Reserved (same as '11' setting)

REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31							bit 24

R/P	r-1	r-1	R/P	R/P	R/P	R/P	R/P
FWDTEN	—	—	WDTPS<4:0>				
bit 23							bit 16

R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
bit 15							bit 8

R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
IESO	—	FSOSCEN	—	—	FNOSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-24 **Reserved:** Write ‘1’

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = The WDT is enabled and cannot be disabled by software
0 = The WDT is not enabled; it can be enabled in software

bit 22-21 **Reserved:** Write ‘1’

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = ‘10100’

REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits
11 = PBCLK is SYSCLK divided by 8
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1

bit 11 **Reserved:** Write '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit
1 = CLKO output signal active on the OSCO pin; primary oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 OR 00)
0 = CLKO output disabled

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
11 = Primary oscillator disabled
10 = HS oscillator mode selected
01 = XT oscillator mode selected
00 = External clock mode selected

bit 7 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode enabled (Two-Speed Start-up enabled)
0 = Internal External Switchover mode disabled (Two-Speed Start-up disabled)

bit 6 **Reserved:** Write '1'

bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator

bit 4-3 **Reserved:** Write '1'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
111 = Fast RC Oscillator with divide-by-N (FRCDIV)
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XT+PLL, HS+PLL, EC+PLL)
010 = Primary Oscillator (XT, HS, EC)**(1)**
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
000 = Fast RC Oscillator (FRC)

Note 1: Do not disable POSC (POSCMOD = 00) when using this oscillator source.

REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31							bit 24

r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
—	—	—	—	—	FPLLODIV<2:0>		
bit 23							bit 16

R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
FUPLLEN	—	—	—	—	FUPLLIDIV<2:0>		
bit 15							bit 8

r-1	R/P	R/P	R/P	r-1	R/P	R/P	R/P
—	FPLLMULT<2:0>			—	FPLLIDIV<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-19 **Reserved:** Write ‘1’

bit 18-16 **FPLLODIV<2:0>:** Default Postscaler for PLL bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **FUPLLEN:** USB PLL Enable bit
- 1 = Enable USB PLL
- 0 = Disable and bypass USB PLL

bit 14-11 **Reserved:** Write ‘1’

bit 10-8 **FUPLLIDIV<2:0>:** PLL Input Divider bits
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write ‘1’

REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 6-4 **FPLLMULT<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

REGISTER 26-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31							bit 24

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
USERID<15:8>							
bit 15							bit 8

R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
USERID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31-16 **Reserved:** Write '1'

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user defined and is readable via ICSP™ and JTAG

REGISTER 26-5: DEVID: DEVICE AND REVISION ID REGISTER

R	R	R	R	R	R	R	R
VER<3:0>(1)				DEVID<27:24>(1)			
bit 31							bit 24

R	R	R	R	R	R	R	R
DEVID<23:16>(1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID<15:8>(1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID<7:0>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID(1)

Note 1: See the “*PIC32MX Flash Programming Specification*” (DS61145) for a list of Revision and Device ID values.

26.2 Watchdog Timer (WDT)

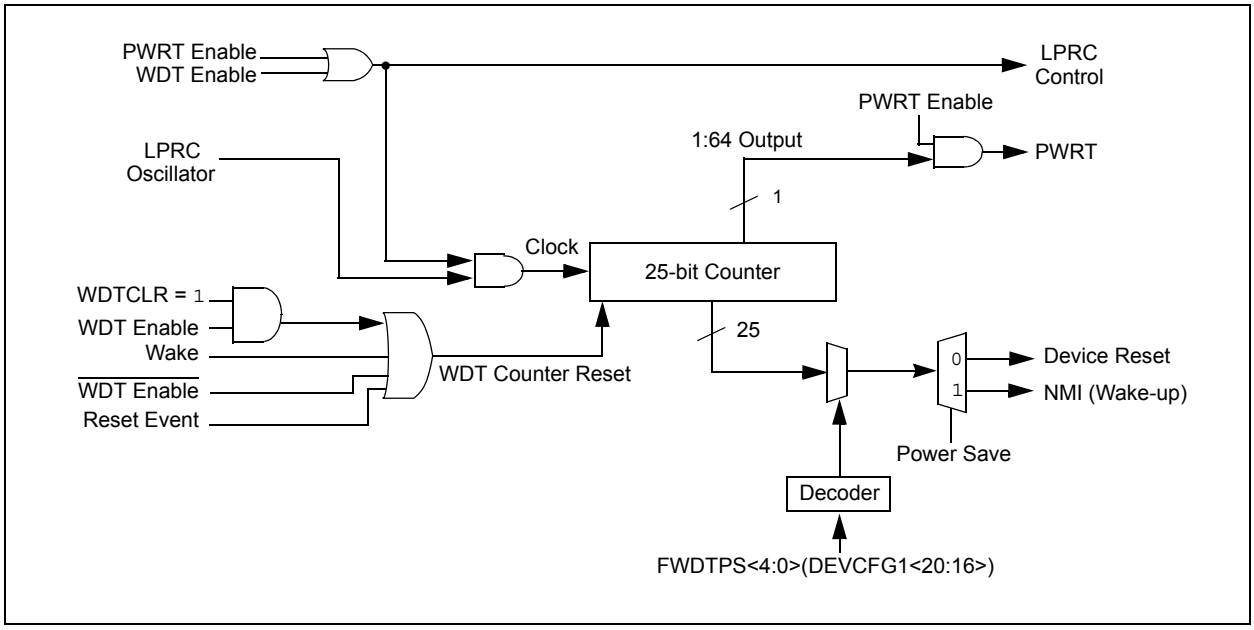
This section describes the operation of the WDT and Power-Up Timer of the PIC32MX3XX/4XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 26-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM



26.3 On-Chip Voltage Regulator

All PIC32MX3XX/4XX device's core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX3XX/4XX incorporate an on-chip regulator providing the required core logic voltage from VDD.

The internal 1.8V regulator is controlled by the ENVREG pin. Tying this pin to VDD enables the regulator, which in turn provides power to the core. A low ESR capacitor (such as tantalum) must be connected to the VDDCORE/VCAP pin (Figure 26-2). This helps to maintain the stability of the regulator. The recommended value for the filer capacitor is provided in **Section 29.1 "DC Characteristics"**.

Note:	It is important that the low ESR capacitor is placed as close as possible to the VDDCORE/VCAP pin.

Tying the ENVREG pin to VSS disables the regulator. In this case, separate power for the core logic at a nominal 1.8V must be supplied to the device on the VDDCORE/VCAP pin.

Alternatively, the VDDCORE/VCAP and VDD pins can be tied together to operate at a lower nominal voltage. Refer to Figure 26-2 for possible configurations.

26.3.1 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes fixed delay for it to generate output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of TPWRT at device start-up. See **Section 29.0 "Electrical Characteristics"** for more information on TPU AND TPWRT.

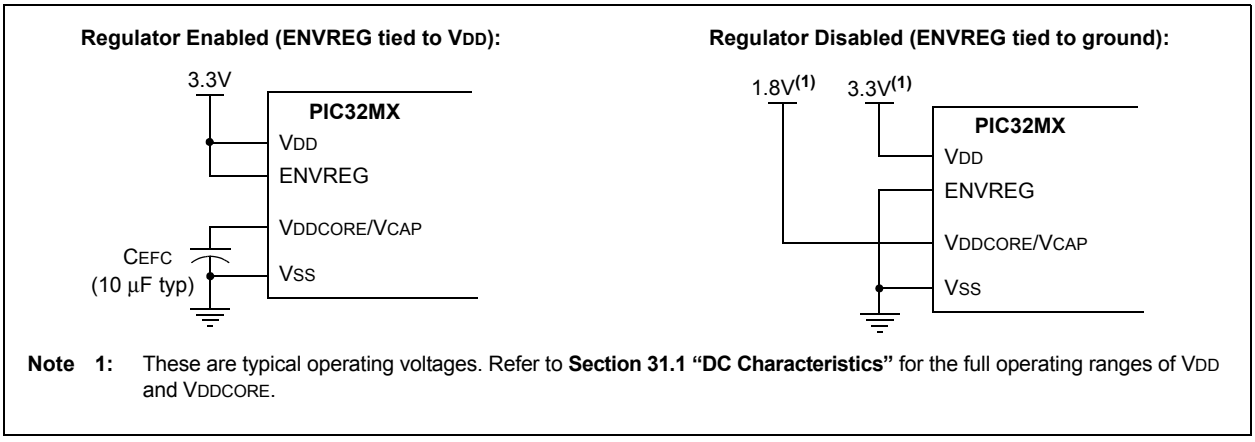
26.3.2 ON-CHIP REGULATOR AND BOR

When the on-chip regulator is enabled, PIC32MX3XX/4XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 29.1 "DC Characteristics"**.

26.3.3 POWER-UP REQUIREMENTS

The on-chip regulator is designed to meet the power-up requirements for the device. If the application does not use the regulator, then strict power-up conditions must be adhered to. While powering up, VDDCORE must never exceed VDD by 0.3 volts.

FIGURE 26-2: CONNECTIONS FOR THE ON-CHIP REGULATOR



Note 1: These are typical operating voltages. Refer to **Section 31.1 "DC Characteristics"** for the full operating ranges of VDD and VDDCORE.

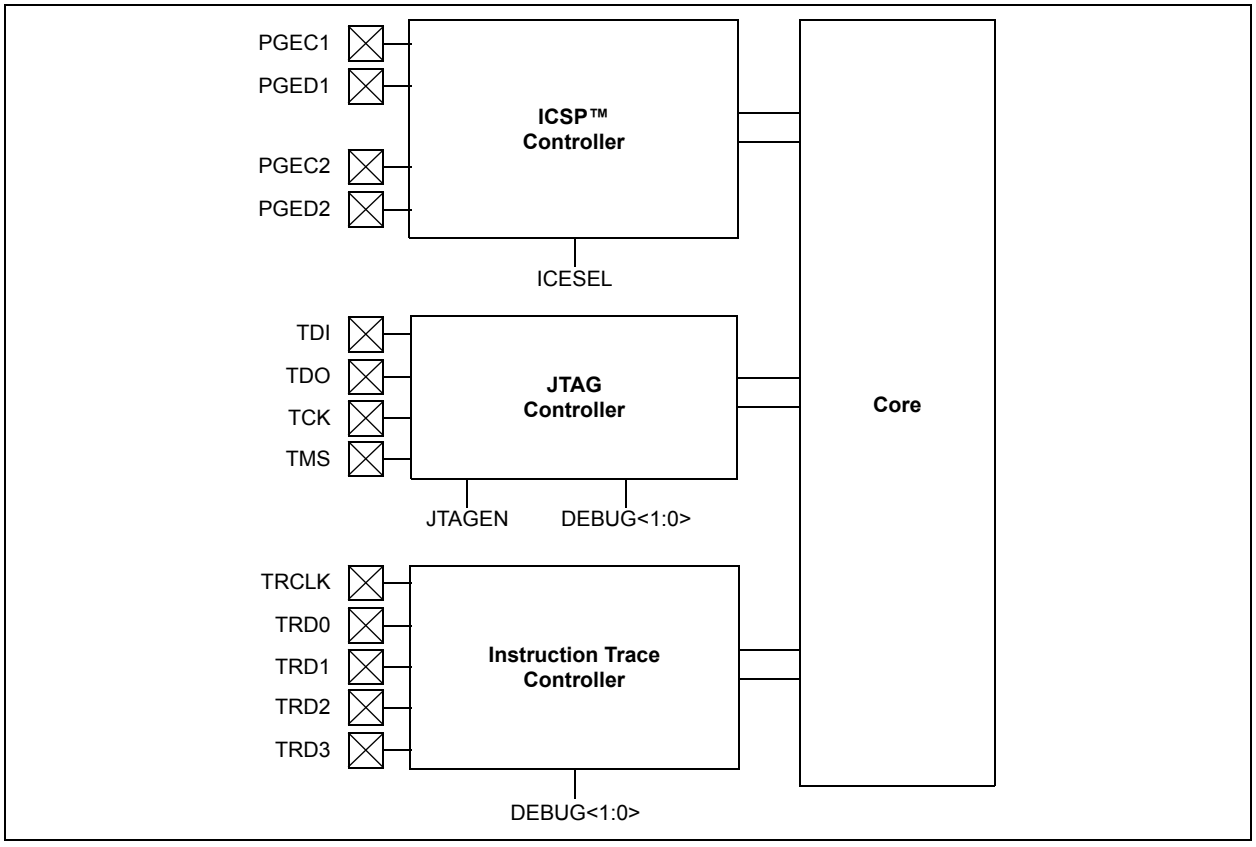
26.4 Programming and Diagnostics

PIC32MX3XX/4XX devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32MX devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 26-3: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS



REGISTER 26-6: DDPCON: DEBUG DATA PORT CONTROL REGISTER

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	r-x	r-x
DDPUSB	DDPU1	DDPU2	DDPSPI1	JTAGEN	TROEN	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-8 **Reserved:** Write ‘0’; ignore read

bit 7 **DDPUSB:** Debug Data Port Enable for USB bit
1 = USB peripheral ignores USBFRZ (U1CNFG1<5>) setting
0 = USB peripheral follows USBFRZ setting

bit 6 **DDPU1:** Debug Data Port Enable for UART1 bit
1 = UART1 peripheral ignores FRZ (U1MODE<14>) setting
0 = UART1 peripheral follows FRZ setting

bit 5 **DDPU2:** Debug Data Port Enable for UART2 bit
1 = UART2 peripheral ignores FRZ (U2MODE<14>) setting
0 = UART2 peripheral follows FRZ setting

bit 4 **DDPSPI1:** Debug Data Port Enable for SPI1 bit
1 = SPI1 peripheral ignores FRZ (SPI1CON<14>) setting
0 = SPI1 peripheral follows FRZ setting

bit 3 **JTAGEN:** JTAG Port Enable bit
1 = Enable JTAG Port
0 = Disable JTAG Port

bit 2 **TROEN:** Trace Output Enable bit
1 = Enable Trace Port
0 = Disable Trace Port

bit 1-0 **Reserved:** Write ‘1’; ignore read

NOTES:

27.0 INSTRUCTION SET

The PIC32MX3XX/4XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. PIC32MX does not support the following features:

- CoreExtend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Table 27-1 provides a summary of the instructions that are implemented by the PIC32MX3XX/4XX family core.

Note: Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.mips.com for more information.

TABLE 27-1: MIPS32® INSTRUCTION SET

Instruction	Description	Function
ADD	Integer Add	Rd = Rs + Rt
ADDI	Integer Add Immediate	Rt = Rs + Immed
ADDIU	Unsigned Integer Add Immediate	Rt = Rs $+_U$ Immed
ADDU	Unsigned Integer Add	Rd = Rs $+_U$ Rt
AND	Logical AND	Rd = Rs & Rt
ANDI	Logical AND Immediate	Rt = Rs & (0_{16} || Immed)
B	Unconditional Branch (Assembler idiom for: BEQ r0, r0, offset)	PC += (int)offset
BAL	Branch and Link (Assembler idiom for: BGEZAL r0, offset)	GPR[31] = PC + 8 PC += (int)offset
BEQ	Branch on Equal	if Rs == Rt PC += (int)offset

BEQL	Branch on Equal Likely(1)	if Rs == Rt
		  PC += (int)offset
		else
		  Ignore Next Instruction

BGEZ	Branch on Greater Than or Equal to Zero	if !Rs[31] PC += (int)offset
BGEZAL	Branch on Greater Than or Equal to Zero and Link	GPR[31] = PC + 8 if !Rs[31] PC += (int)offset

BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely(1)	GPR[31] = PC + 8
		if !Rs[31]
		  PC += (int)offset
		else
		  Ignore Next Instruction

BGEZL	Branch on Greater Than or Equal to Zero Likely(1)	if !Rs[31]
		  PC += (int)offset
		else
		  Ignore Next Instruction

BGTZ	Branch on Greater Than Zero	if !Rs[31] && Rs != 0 PC += (int)offset

BGTZL	Branch on Greater Than Zero Likely(1)	if !Rs[31] && Rs != 0
		  PC += (int)offset
		else
		  Ignore Next Instruction

BLEZ	Branch on Less Than or Equal to Zero	if Rs[31] || Rs == 0 PC += (int)offset

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function

BLEZL	Branch on Less Than or Equal to Zero Likely(1)	if Rs[31] || Rs == 0
		  PC += (int)offset
		else
		  Ignore Next Instruction

BLTZ	Branch on Less Than Zero	if Rs[31] PC += (int)offset
BLTZAL	Branch on Less Than Zero and Link	GPR[31] = PC + 8 if Rs[31] PC += (int)offset

BLTZALL	Branch on Less Than Zero and Link Likely(1)	GPR[31] = PC + 8
		if Rs[31]
		  PC += (int)offset
		else
		  Ignore Next Instruction

BLTZL	Branch on Less Than Zero Likely(1)	if Rs[31]
		  PC += (int)offset
		else
		  Ignore Next Instruction

BNE	Branch on Not Equal	if Rs != Rt PC += (int)offset

BNEL	Branch on Not Equal Likely(1)	if Rs != Rt
		  PC += (int)offset
		else
		  Ignore Next Instruction

BREAK	Breakpoint	Break Exception
CLO	Count Leading Ones	Rd = NumLeadingOnes(Rs)
CLZ	Count Leading Zeroes	Rd = NumLeadingZeroes(Rs)
DERET	Return from Debug Exception	PC = DEPC Exit Debug Mode
DI	Atomically Disable Interrupts	Rt = Status; $Status_{IE}$ = 0
DIV	Divide	LO = (int)Rs / (int)Rt HI = (int)Rs % (int)Rt
DIVU	Unsigned Divide	LO = (uns)Rs / (uns)Rt HI = (uns)Rs % (uns)Rt
EHB	Execution Hazard Barrier	Stop instruction execution until execution hazards are cleared
EI	Atomically Enable Interrupts	Rt = Status; $Status_{IE}$ = 1

ERET	Return from Exception	if $Status_{ERL}$
		  PC = ErrorEPC
		else
		  PC = EPC
		  $Status_{EXL}$ = 0
		$Status_{ERL}$ = 0
		LL = 0

EXT	Extract Bit Field	Rt = ExtractField(Rs, pos, size)
INS	Insert Bit Field	Rt = InsertField(Rs, Rt, pos, size)
J	Unconditional Jump	PC = PC[31:28] || offset<<2

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
JAL	Jump and Link	GPR[31] = PC + 8 PC = PC[31:28] || offset<<2
JALR	Jump and Link Register	Rd = PC + 8 PC = Rs
JALR.HB	Jump and Link Register with Hazard Barrier	Like JALR, but also clears execution and instruction hazards
JR	Jump Register	PC = Rs
JR.HB	Jump Register with Hazard Barrier	Like JR, but also clears execution and instruction hazards
LB	Load Byte	Rt = (byte)Mem[Rs+offset]
LBU	Unsigned Load Byte	Rt = (ubyte))Mem[Rs+offset]
LH	Load Halfword	Rt = (half)Mem[Rs+offset]
LHU	Unsigned Load Halfword	Rt = (uhalf)Mem[Rs+offset]
LL	Load Linked Word	Rt = Mem[Rs+offset> LL_{bit} = 1 LLAdr = Rs + offset
LUI	Load Upper Immediate	Rt = immediate << 16
LW	Load Word	Rt = Mem[Rs+offset]
LWPC	Load Word, PC relative	Rt = Mem[PC+offset]
LWL	Load Word Left	Re = Re MERGE Mem[Rs+offset]
LWR	Load Word Right	Re = Re MERGE Mem[Rs+offset]
MADD	Multiply-Add	HI | LO += (int)Rs * (int)Rt
MADDU	Multiply-Add Unsigned	HI | LO += (uns)Rs * (uns)Rt
MFC0	Move from Coprocessor 0	Rt = CPR[0, Rd, sel]
MFHI	Move from HI	Rd = HI
MFLO	Move from LO	Rd = LO
MOVN	Move Conditional on Not Zero	if Rt ¼ 0 then Rd = Rs
MOVZ	Move Conditional on Zero	if Rt = 0 then Rd = Rs
MSUB	Multiply-Subtract	HI | LO -= (int)Rs * (int)Rt
MSUBU	Multiply-Subtract Unsigned	HI | LO -= (uns)Rs * (uns)Rt
MTC0	Move to Coprocessor 0	CPR[0, n, Sel] = Rt
MTHI	Move to HI	HI = Rs
MTLO	Move to LO	LO = Rs
MUL	Multiply with register write	HI | LO =Unpredictable Rd = ((int)Rs * (int)Rt)$_{31..0}$
MULT	Integer Multiply	HI | LO = (int)Rs * (int)Rd
MULTU	Unsigned Multiply	HI | LO = (uns)Rs * (uns)Rd
NOP	No Operation (Assembler idiom for: SLL r0, r0, r0)	
NOR	Logical NOR	Rd = ~(Rs | Rt)
OR	Logical OR	Rd = Rs | Rt
ORI	Logical OR Immediate	Rt = Rs | Immed
RDHWR	Read Hardware Register (if enabled by $HWRE_{na}$ Register)	Re = HWR[Rd]

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
RDPGPR	Read GPR from Previous Shadow Set	Rt = SGPR[SRSCtl$_{PSS}$, Rd]
ROTR	Rotate Word Right	Rd = Rt$_{sa-1..0}$ || Rt$_{31..sa}$
ROTRV	Rotate Word Right Variable	Rd = Rt$_{Rs-1..0}$ || Rt$_{31..Rs}$
SB	Store Byte	(byte)Mem[Rs+offset] = Rt
SC	Store Conditional Word	if LL$_{bit}$ = 1 mem[Rs+offset> = Rt Rt = LL$_{bit}$
SDBBP	Software Debug Break Point	Trap to SW Debug Handler
SEB	Sign-Extend Byte	Rd = SignExtend (Rs-7...0)
SEH	Sign-Extend Half	Rd = SignExtend (Rs-15...0)
SH	Store Half	(half)Mem[Rs+offset> = Rt
SLL	Shift Left Logical	Rd = Rt << sa
SLLV	Shift Left Logical Variable	Rd = Rt << Rs[4:0]

SLT	Set on Less Than	if (int)Rs < (int)Rt
		Rd = 1
		else
		Rd = 0

SLTI	Set on Less Than Immediate	if (int)Rs < (int)Immed
		Rt = 1
		else
		Rt = 0

SLTIU	Set on Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed
		Rt = 1
		else
		Rt = 0

SLTU	Set on Less Than Unsigned	if (uns)Rs < (uns)Immed
		Rd = 1
		else
		Rd = 0

SRA	Shift Right Arithmetic	Rd = (int)Rt >> sa
SRAV	Shift Right Arithmetic Variable	Rd = (int)Rt >> Rs[4:0]
SRL	Shift Right Logical	Rd = (uns)Rt >> sa
SRLV	Shift Right Logical Variable	Rd = (uns)Rt >> Rs[4:0]
SSNOP	Superscalar Inhibit No Operation	NOP
SUB	Integer Subtract	Rt = (int)Rs - (int)Rd
SUBU	Unsigned Subtract	Rt = (uns)Rs - (uns)Rd
SW	Store Word	Mem[Rs+offset] = Rt
SWL	Store Word Left	Mem[Rs+offset] = Rt
SWR	Store Word Right	Mem[Rs+offset] = Rt
SYNC	Synchronize	Orders the cached coherent and uncached loads and stores for access to the shared memory
SYSCALL	System Call	SystemCallException
TEQ	Trap if Equal	if Rs == Rt TrapException
TEQI	Trap if Equal Immediate	if Rs == (int)Immed TrapException

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	$SGPR[SRSCtl_{PSS}, Rd> = Rt$
WSBH	Word Swap Bytes Within Halfwords	$Rd = Rt_{23..16} \mid\mid Rt_{31..24} \mid\mid Rt_{7..0} \mid\mid Rt_{15..8}$
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

Note 1: This instruction is deprecated and should not be used.

NOTES:

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits

28.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

28.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

28.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

28.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

28.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

28.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

28.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

28.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and Microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

28.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement In-Circuit Debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

28.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

28.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

28.13 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC32MX3XX/4XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX3XX/4XX are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings (Note 1)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} WHEN $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} WHEN $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on V_{DDCORE} with respect to V_{SS} ..... -0.3V to 2.0V
Maximum current out of V_{SS} pin(s) ..... 300 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 300 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 29-2).

3: See the **"Pin Diagrams"** section for the 5V tolerant pins.

29.1 DC Characteristics

TABLE 29-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp. Range (in °C)	Max. Frequency
			PIC32MX3XX/4XX
DC5	2.3-3.6V	-40°C to +85°C	80 MHz **(Note 1)**

Note 1: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

TABLE 29-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
PIC32MX3XX/4XX					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S ({VDD – VOH} x IOH) + S (VOL x IOL))	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 29-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 121-Pin XBGA (10x10x1.1 mm)	θJA	40	—	°C/W	**1**
Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm)	θJA	43	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm)	θJA	47	—	°C/W	**1**
Package Thermal Resistance, 64-Pin QFN (9x9x0.9 mm)	θJA	28	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 29-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	**Supply Voltage**						
	VDD		2.3	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage (Note 1)**	1.75	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	1.75	—	1.95	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	—

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 29-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Parameter No.	**Typical(3)**	**Max.**	**Units**	**Conditions**	
Operating Current (IDD)(1,2)					
DC20	8.5	13	mA	Code executing from Flash	—	4 MHz
DC20c	4.0	—	mA	Code executing from SRAM	—	
DC21	23.5	32	mA	Code executing from Flash	—	20 MHz **(Note 4)**
DC21c	16.4	—	mA	Code executing from SRAM	—	
DC22	48	61	mA	Code executing from Flash	—	60 MHz **(Note 4)**
DC22c	45	—	mA	Code executing from SRAM	—	
DC23	55	75	mA	Code executing from Flash	2.3V	80 MHz
DC23c	55	—	mA	Code executing from SRAM	—	
DC24	—	100	µA	-40°C	2.3V	LPRC (31 kHz) **(Note 4)**
DC24a	—	130	µA	+25°C		
DC24b	—	670	µA	+85°C		
DC25	94	—	µA	-40°C	3.3V	
DC25a	125	—	µA	+25°C		
DC25b	302	—	µA	+85°C		
DC25c	71	—	µA	Code executing from SRAM		
DC26	—	110	µA	-40°C	3.6V	
DC26a	—	180	µA	+25°C		
DC26b	—	700	µA	+85°C		

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type as well as temperature can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows: Oscillator mode = EC+PLL with OSC1 driven by external square wave from rail to rail and PBCLK divisor = 1:8. CPU, Program Flash and SRAM data memory are operational, Program Flash memory Wait states = 7, program cache and prefetch are disabled and SRAM data memory Wait states = 1. All peripheral modules are disabled (ON bit = 0). WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to VSS. $\overline{MCLR}$ = VDD.

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

TABLE 29-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(2)**	**Max.**	**Units**	**Conditions**		
Idle Current (I_{IDLE}): Core OFF, Clock ON Base Current (Note 1)						
DC30	—	5	mA	—	2.3V	4 MHz
DC30a	1.4	—	mA	—	—	
DC30b	—	5	mA	—	3.6V	
DC31	—	15	mA	—	2.3V	20 MHz **(Note 3)**
DC31a	13	—	mA	—	—	
DC31b	—	17	mA	—	3.6V	
DC32	—	22	mA	—	2.3V	60 MHz **(Note 3)**
DC32a	20	—	mA	—	—	
DC32b	—	25	mA	—	3.6V	
DC33	—	29	mA	—	2.3V	80 MHz
DC33a	24	—	mA	—	—	
DC33b	—	32	mA	—	3.6V	
DC34	—	36	µA	-40°C	2.3V	LPRC (31 kHz) **(Note 3)**
DC34a	—	62	µA	+25°C		
DC34b	—	392	µA	+85°C		
DC35	35	—	µA	-40°C	3.3V	
DC35a	65	—	µA	+25°C		
DC35b	242	—	µA	+85°C		
DC36	—	43	µA	-40°C	3.6V	
DC36a	—	106	µA	+25°C		
DC36b	—	414	µA	+85°C		

Note 1: The test conditions for base I_{IDLE} current measurements are as follows: System clock is enabled and PBCLK divisor = 1:8. CPU in Idle mode (CPU core halted). Only digital peripheral modules are enabled (ON bit = 1) and being clocked. WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to V_{SS}. $\overline{MCLR}$ = V_{DD}.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(2)**	**Max.**	**Units**	**Conditions**		
Power-Down Current (I_{PD}) (Note 1)						
DC40	7	30	µA	-40°C	2.3V	Base Power-Down Current **(Note 6)**
DC40a	24	30	µA	+25°C		
DC40b	205	300	µA	+85°C		
DC40c	25	—	µA	+25°C	3.3V	Base Power-Down Current
DC40d	9	70	µA	-40°C	3.6V	Base Power-Down Current
DC40e	25	70	µA	+25°C		
DC40g	115	200 **(Note 5)**	µA	+70°C		
DC40f	200	400	µA	+85°C		
Module Differential Current						
DC41	—	10	µA	-40°C	2.3V	Watchdog Timer Current: ΔI_{WDT} **(Notes 3,6)**
DC41a	—	10	µA	+25°C		
DC41b	—	10	µA	+85°C		
DC41c	5	—	µA	+25°C	3.3V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC41d	—	10	µA	-40°C	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC41e	—	10	µA	+25°C		
DC41f	—	12	µA	+85°C		
DC42	—	10	µA	-40°C	2.3V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Notes 3,6)**
DC42a	—	17	µA	+25°C		
DC42b	—	37	µA	+85°C		
DC42c	23	—	µA	+25°C	3.3V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC42e	—	10	µA	-40°C	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC42f	—	30	µA	+25°C		
DC42g	—	44	µA	+85°C		
DC42	—	1100	µA	-40°C	2.5V	ADC: ΔI_{ADC} **(Notes 3,4,6)**
DC42a	—	1100	µA	+25°C		
DC42b	—	1000	µA	+85°C		
DC42c	880	—	µA	—	—	ADC: ΔI_{ADC} **(Notes 3,4)**
DC42e	—	1100	µA	-40°C	3.6V	ADC: ΔI_{ADC} **(Notes 3,4)**
DC42f	—	1100	µA	+25°C		
DC42g	—	1000	µA	+85°C		

Note 1: Base I_{PD} is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: Data is characterized at +70°C and not tested. Parameter is for design guidance only.

6: This parameter is characterized, but not tested in manufacturing.

TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O pins:					
		with TTL Buffer	VSS	—	0.15 VDD	V	**(Note 4)**
		with Schmitt Trigger Buffer	VSS	—	0.2 VDD	V	**(Note 4)**
DI15		$\overline{MCLR}$	VSS	—	0.2 VDD	V	**(Note 4)**
DI16		OSC1 (XT mode)	VSS	—	0.2 VDD	V	**(Note 4)**
DI17		OSC1 (HS mode)	VSS	—	0.2 VDD	V	**(Note 4)**
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
	VIH	**Input High Voltage**					
DI20		I/O pins:					
		with Analog Functions	0.8 VDD	—	VDD	V	**(Note 4)**
		Digital Only	0.8 VDD	—		V	**(Note 4)**
		with TTL Buffer	0.25VDD + 0.8V	—	5.5	V	**(Note 4)**
		with Schmitt Trigger Buffer	0.8 VDD	—	5.5	V	**(Note 4)**
DI25		$\overline{MCLR}$	0.8 VDD	—	VDD	V	**(Note 4)**
DI26		OSC1 (XT mode)	0.7 VDD	—	VDD	V	**(Note 4)**
DI27		OSC1 (HS mode)	0.7 VDD	—	VDD	V	**(Note 4)**
DI28		SDAx, SCLx	0.7 VDD	—	5.5	V	SMBus disabled **(Note 4)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4)**
DI30	ICNPU	**CNxx Pull up Current**	50	250	400	µA	VDD = 3.3V, VPIN = VSS
	IIL	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{MCLR}$	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

TABLE 29-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
	VOL	**Output Low Voltage**					
DO10		I/O Ports	—	—	0.4	V	IOL = 7 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 6 mA, VDD = 2.3V
DO16		OSC2/CLKO	—	—	0.4	V	IOL = 3.5 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 2.5 mA, VDD = 2.3V
	VOH	**Output High Voltage**					
DO20		I/O Ports	2.4	—	—	V	IOH = -12 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -12 mA, VDD = 2.3V
DO26		OSC2/CLKO	2.4	—	—	V	IOH = -12 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -12 mA, VDD = 2.3V

TABLE 29-10: DC CHARACTERISTICS: PROGRAM MEMORY(3)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial Programming temperature 0°C ≤ TA ≤ +70°C (25°C recommended)				
Param. No.	Symbol	Characteristics	Min.	Typical(1)	Max.	Units	Conditions
		Program Flash Memory					
D130	EP	Cell Endurance	1000	—	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	0°C to +40°C
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	0°C to +40°C
	TWW	Word Write Cycle Time	20	—	40	µs	0°C to +40°C
D136	TRW	Row Write Cycle Time **(Note 2)** (128 words per row)	3	4.5	—	ms	0°C to +40°C
D137	TPE	Page Erase Cycle Time	20	—	—	ms	0°C to +40°C
	TCE	Chip Erase Cycle Time	80	—	—	ms	0°C to +40°C
D138	LVDstartup	Flash LVD Delay	—	—	6	µs	Flash LVD comparator delay from enable to output valid.

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to "*PIC32MX Flash Programming Specification*" (DS61145) for operating conditions during programming and erase cycles.

TABLE 29-11: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS

DC CHARACTERISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Required Flash wait states	**SYSCLK**	**Units**	**Comments**
0 Wait State	0 to 30	MHz	—
1 Wait State	31 to 60		
2 Wait States	61 to 80		

Note 1: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

TABLE 29-12: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±7.5	±25	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS **(Note 2)**
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max VICM = (VDD - 1)V **(Note 2)**
D303	TRESP	Response Time	—	150	400	nsec	AVDD = VDD, AVSS = VSS **(Notes 1,2)**
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	µs	Comparator module is configured before setting the comparator ON bit. **(Note 2)**
D305	IVREF	Internal Voltage Reference	1.14	1.2	1.26	V	—

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

TABLE 29-13: VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D310	VRES	Resolution	VDD/24	—	VDD/32	LSb	—
D311	VRAA	Absolute Accuracy	—	—	1/2	LSb	—
D312	TSET	Settling Time(1)	—	—	10	µs	—

Note 1: Settling time measured while CVRR = 1 and CVR3:CVR0 transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

TABLE 29-14: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D320	VDDCORE	Regulator Output Voltage	1.62	1.80	1.98	V	—
D321	CEFC	External Filter Capacitor Value	8	10	—	µF	Capacitor must be low series resistance (< 1 Ohm)
D322	TPWRT	Power-up Timer Period	—	64	—	ms	ENVREG = 0

29.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX3XX/4XX AC characteristics and timing parameters.

TABLE 29-15: AC CHARACTERISTICS

AC CHARACTERISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial Operating voltage VDD range.

FIGURE 29-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

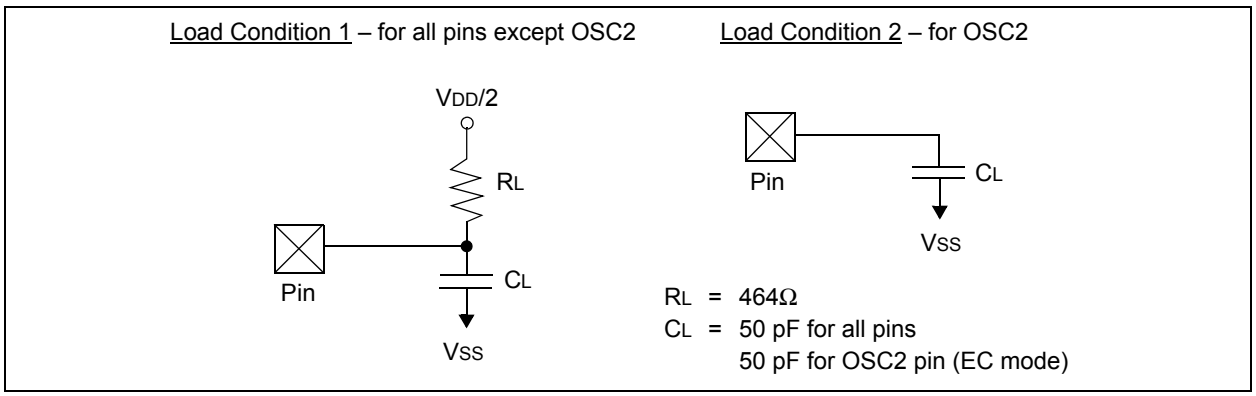


TABLE 29-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 29-2: EXTERNAL CLOCK TIMING

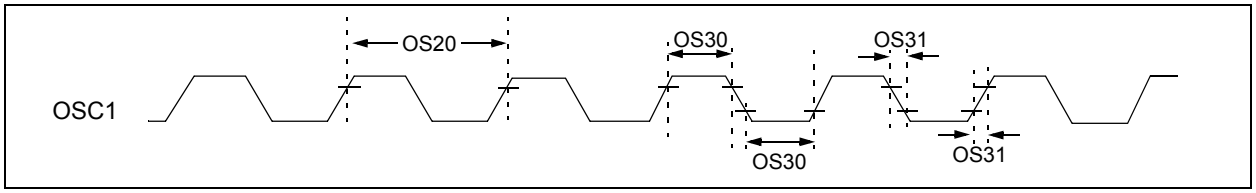


TABLE 29-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 **(Note 3)** 50 **(Note 5)**	MHz MHz	EC **(Note 5)** ECPLL **(Note 4)**
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT **(Note 5)**
OS12			4	—	10	MHz	XTPLL **(Notes 4,5)**
OS13			10	—	25	MHz	HS **(Note 5)**
OS14			10	—	25	MHz	HSPLL **(Notes 4,5)**
OS15			32	32.768	100	kHz	SOSC **(Note 5)**
OS20	TOSC	TOSC = 1/FOSC = TCY **(Note 2)**	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.45 x TOSC	—	—	nsec	EC **(Note 5)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x TOSC	nsec	EC **(Note 5)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 5)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 5)**
OS42	GM	External Oscillator Transconductance	—	12	—	mA/V	VDD = 3.3V TA = +25°C **(Note 5)**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

2: Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

3: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

4: PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

5: This parameter is characterized, but not tested in manufacturing.

TABLE 29-18: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.3V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	4	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—
OS53	DCLK	CLKO Stability (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 29-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param. No.	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz (Note 1)						
F20	FRC	-2	—	+2	%	—

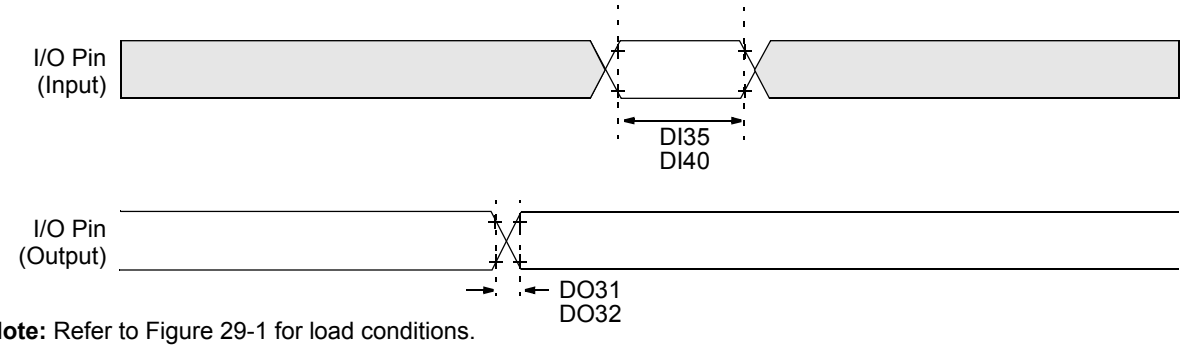
Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 29-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
LPRC @ 31.25 kHz (Note 1)						
F21	LPRC	-15	—	+15	%	—

Note 1: Change of LPRC frequency as V_{DD} changes.

FIGURE 29-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-21: I/O TIMING REQUIREMENTS

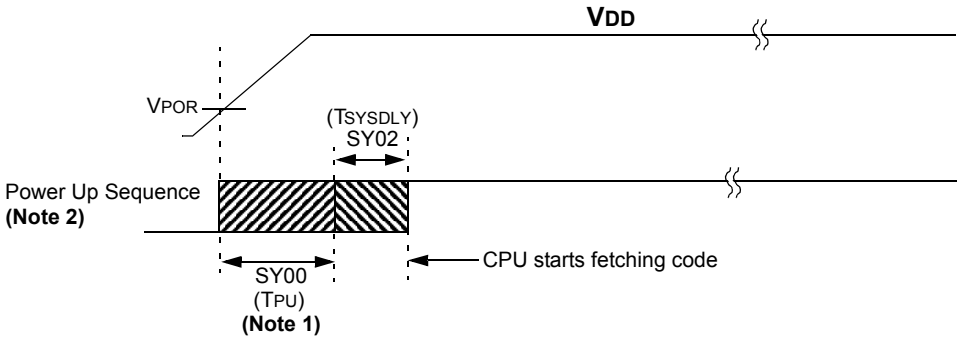
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	15	nsec	VDD < 2.5V
			—	5	10	nsec	VDD > 2.5V
DO32	TIOF	Port Output Fall Time	—	5	15	nsec	VDD < 2.5V
			—	5	10	nsec	VDD > 2.5V
DI35	TINP	INTx Pin High or Low Time	10	—	—	nsec	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TSYSCLK	—

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

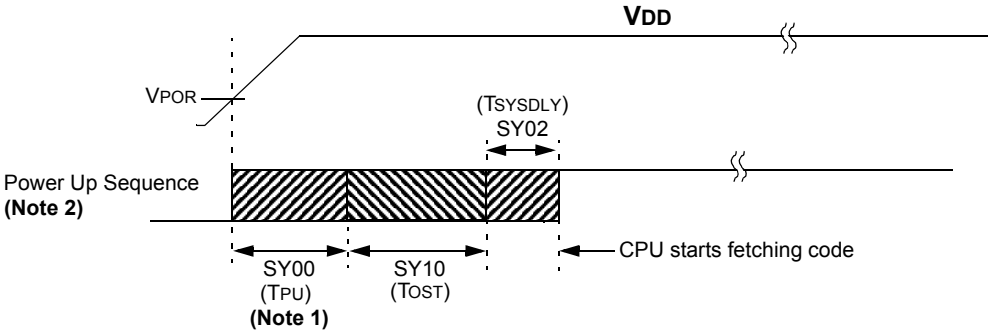
2: This parameter is characterized, but not tested in manufacturing.

FIGURE 29-4: POWER-ON RESET TIMING CHARACTERISTICS

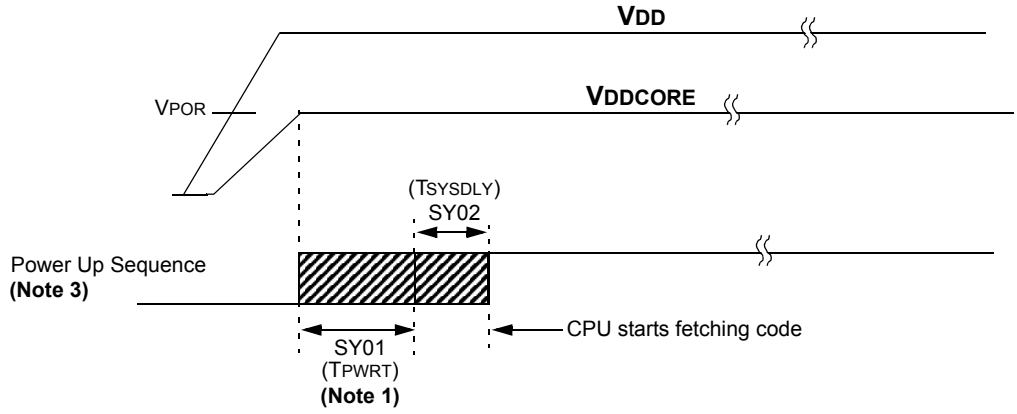
Internal Voltage Regulator Enabled
Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)



Internal Voltage Regulator Enabled
Clock Sources = (HS, HSPLL, XT, XTPLL and SOSC)



External VDDCORE Provided
Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)



Note 1: The Power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDD < VDDMIN).

2: Includes interval voltage regulator stabilization delay.

3: Power-up Timer (PWRT); only active when the internal voltage regulator is disabled

FIGURE 29-5: EXTERNAL RESET TIMING CHARACTERISTICS

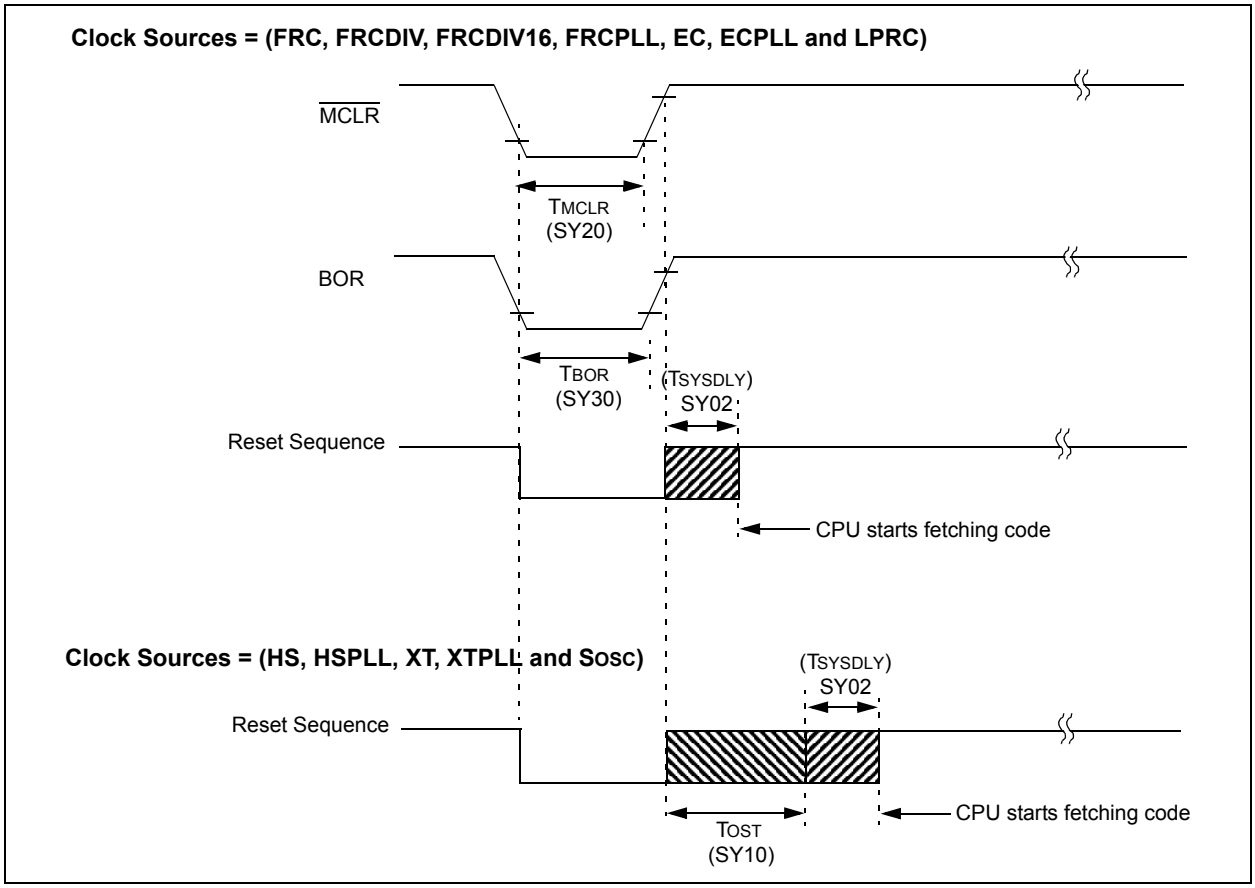


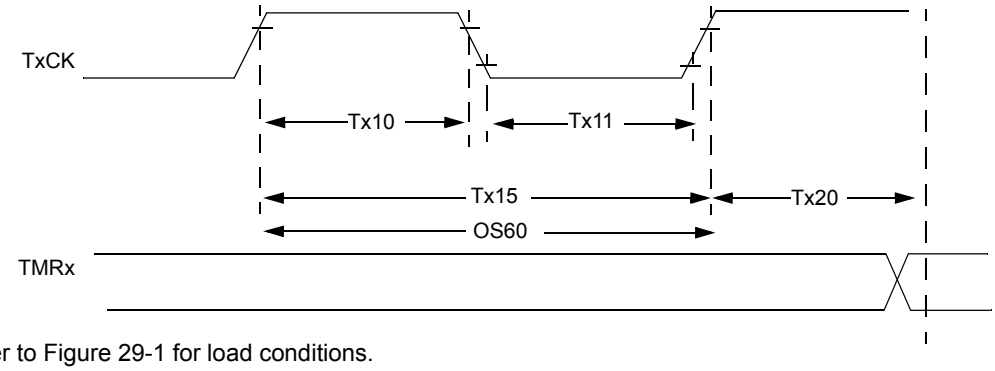
TABLE 29-22: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	-40°C to +85°C
SY01	TPWRT	Power-up Period External VDDCORE Applied (Power-Up-Timer Active)	48	64	80	ms	-40°C to +85°C
SY02	TSYSDLY	System Delay Period: Time required to reload Device Configuration Fuses plus SYSCLK delay before first instruction is fetched.	—	1 μs + 8 SYSCLK cycles	—	—	-40°C to +85°C
SY20	TMCLR	$\overline{\text{MCLR}}$ Pulse Width (low)	—	2	—	μs	-40°C to +85°C
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	-40°C to +85°C

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

FIGURE 29-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(2)**		**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 nsec or 1TPB)/N] + 25 nsec	—	—	nsec	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	nsec	
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 nsec or 1TPB)/N] + 25 nsec	—	—	nsec	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	nsec	—
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 nsec or 2TPB)/N] + 30 nsec	—	—	nsec	VDD > 2.7V
				[(Greater of 25 nsec or 2TPB)/N] + 50 nsec	—	—	nsec	VDD < 2.7V
			Asynchronous, with prescaler	20	—	—	nsec	VDD > 2.7V **(Note 3)**
				50	—	—	nsec	VDD < 2.7V **(Note 3)**
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	100	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPB	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

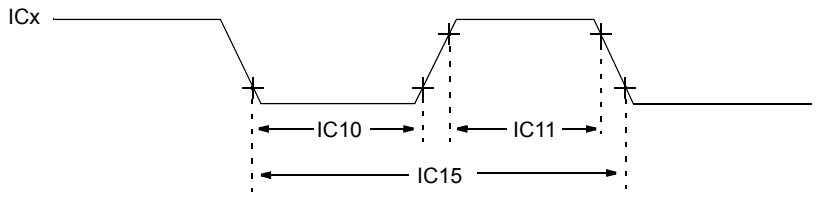
3: N = prescale value (1, 8, 64, 256)

TABLE 29-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**	
TB10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 nsec or 1TPB)/N] + 25 nsec	—	nsec	Must also meet parameter TB15.	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 nsec or 1TPB)/N] + 25 nsec	—	nsec	Must also meet parameter TB15.	
TB15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 nsec or 2 TPB)/N] + 30 nsec	—	nsec	VDD > 2.7V	
				[(Greater of 25 nsec or 2 TPB)/N] + 50 nsec	—	nsec	VDD < 2.7V	—
TB20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



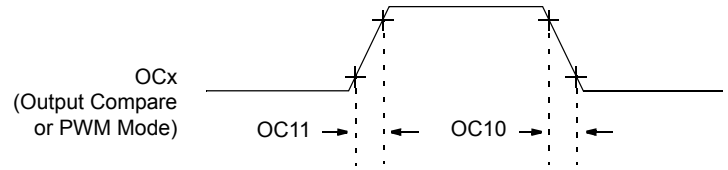
Note: Refer to Figure 29-1 for load conditions.

TABLE 29-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TCCL	ICx Input Low Time	[(12.5 nsec or 1TPB)/N] + 25 nsec	—	nsec	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TCCH	ICx Input High Time	[(12.5 nsec or 1TPB)/N] + 25 nsec	—	nsec	Must also meet parameter IC15.	
IC15	TCCP	ICx Input Period	[(25 nsec or 2TPB)/N] + 50 nsec	—	nsec	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

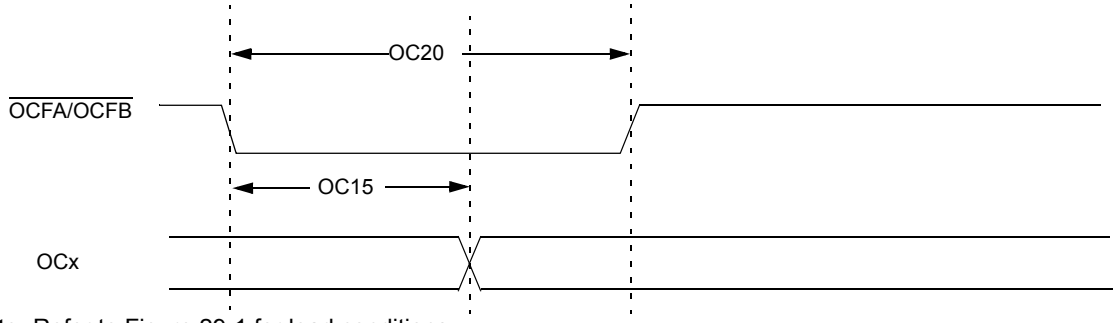
TABLE 29-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	nsec	See parameter DO32.
OC11	TccR	OCx Output Rise Time	—	—	—	nsec	See parameter DO31.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 29-9: OC/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

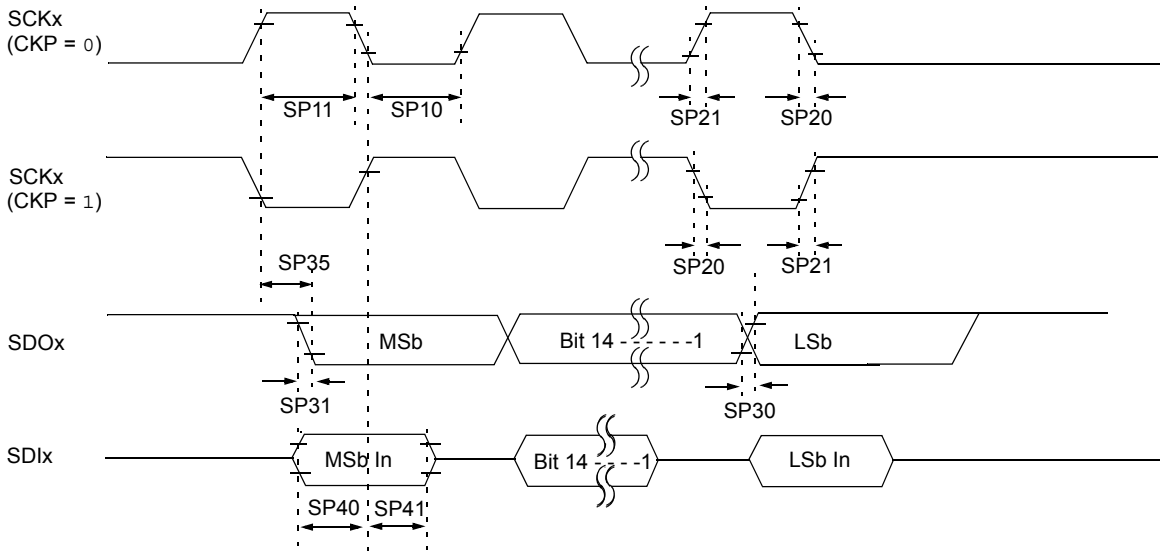
TABLE 29-27: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	nsec	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	nsec	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 29-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics(1)	Min.	Typical(2)	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP11	TscH	SCKx Output High Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP20	TscF	SCKx Output Fall Time **(Note 4)**	—	—	—	nsec	See parameter DO32.
SP21	TscR	SCKx Output Rise Time **(Note 4)**	—	—	—	nsec	See parameter DO31.
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	nsec	See parameter DO32.
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	nsec	See parameter DO31.
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	VDD > 2.7V
			—	—	20	nsec	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	—

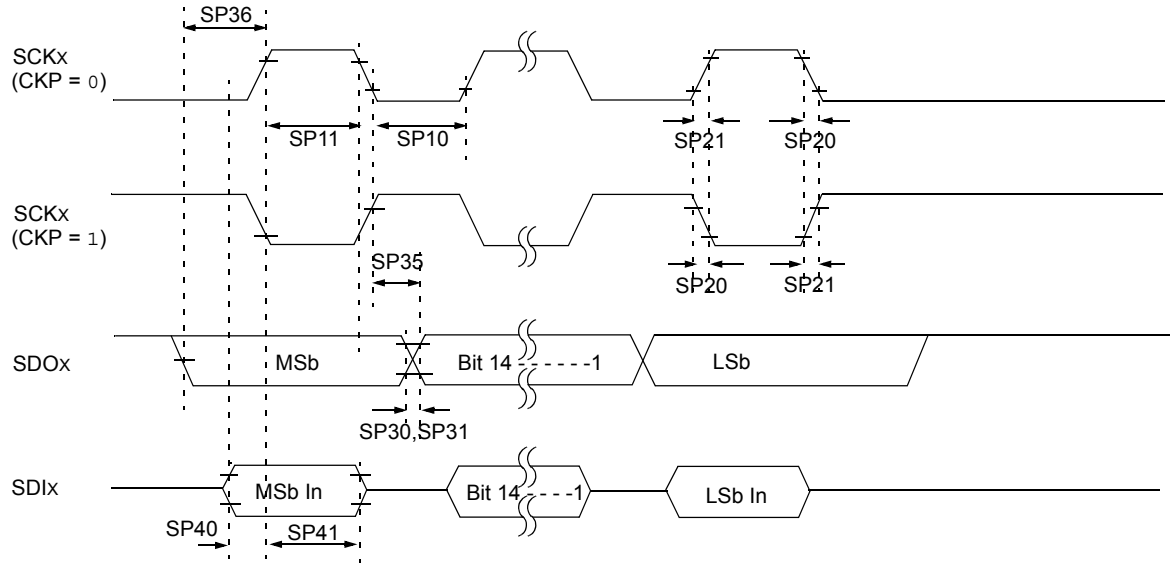
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 29-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°Cfor Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP11	TscH	SCKx Output High Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP20	TscF	SCKx Output Fall Time **(Note 4)**	—	—	—	nsec	See parameter DO32.
SP21	TscR	SCKx Output Rise Time **(Note 4)**	—	—	—	nsec	See parameter DO31.
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	nsec	See parameter DO32.
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	nsec	See parameter DO31.
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	VDD > 2.7V
			—	—	20	nsec	VDD < 2.7V
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	15	—	—	nsec	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	nsec	VDD > 2.7V
			20	—	—	nsec	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 29-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics(1)	Min.	Typical(2)	Max.	Units	Conditions
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	nsec	VDD > 2.7V
			20	—	—	nsec	VDD < 2.7V

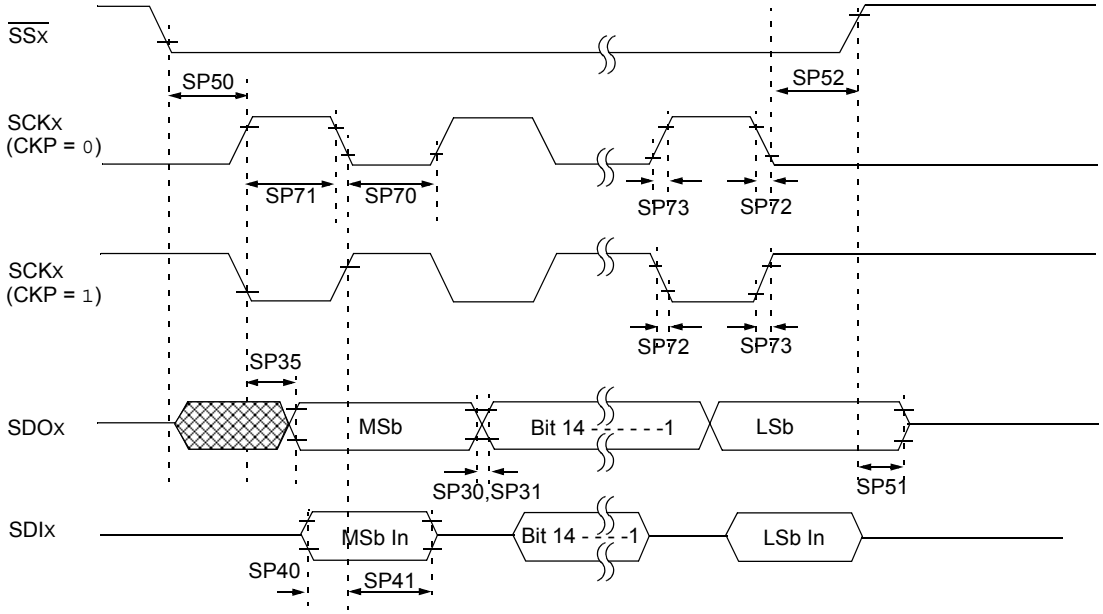
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 29-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP72	TscF	SCKx Input Fall Time	—	—	—	nsec	See parameter DO32.
SP73	TscR	SCKx Input Rise Time	—	—	—	nsec	See parameter DO31.
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	nsec	See parameter DO32.
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	nsec	See parameter DO31.
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	nsec	VDD > 2.7V
			—	—	20	nsec	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	175	—	—	nsec	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)**	5	—	25	nsec	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	Tsck + 20	—	—	nsec	—

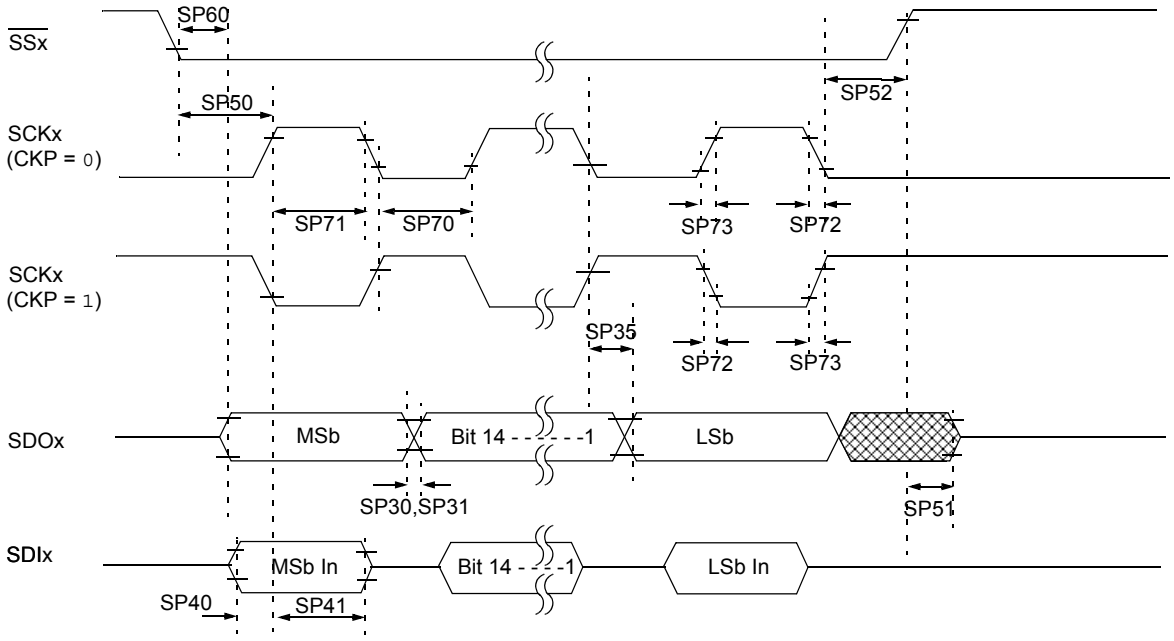
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 29-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	nsec	—
SP72	TscF	SCKx Input Fall Time	—	5	10	nsec	—
SP73	TscR	SCKx Input Rise Time	—	5	10	nsec	—
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	nsec	See parameter DO32.
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	nsec	See parameter DO31.
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	20	nsec	VDD > 2.7V
			—	—	30	nsec	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec.

4: Assumes 50 pF load on all SPIx pins.

TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics(1)	Min.	Typical(2)	Max.	Units	Conditions
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	nsec	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	nsec	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	5	—	25	nsec	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	Tsck + 20	—	—	nsec	—
SP60	TssL2doV	$\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge	—	—	25	nsec	—

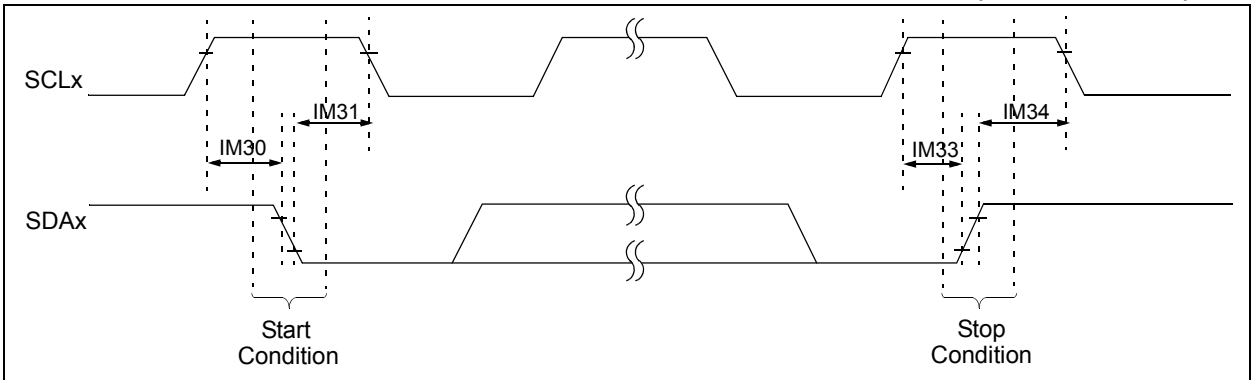
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 nsec.

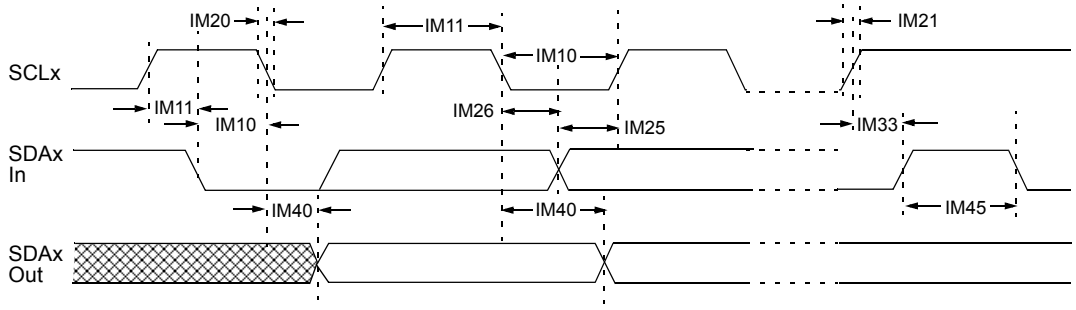
4: Assumes 50 pF load on all SPIx pins.

FIGURE 29-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 29-1 for load conditions.

FIGURE 29-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	nsec	CB is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 CB	300	nsec	
			1 MHz mode **(Note 2)**	—	100	nsec	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	nsec	CB is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 CB	300	nsec	
			1 MHz mode **(Note 2)**	—	300	nsec	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	nsec	—
			400 kHz mode	100	—	nsec	
			1 MHz mode **(Note 2)**	100	—	nsec	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	Only relevant for Repeated Start condition.
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	µs	After this period, the first clock pulse is generated.
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	nsec	—
			400 kHz mode	TPB * (BRG + 2)	—	nsec	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	nsec	

Note 1: BRG is the value of the I^2C™ Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

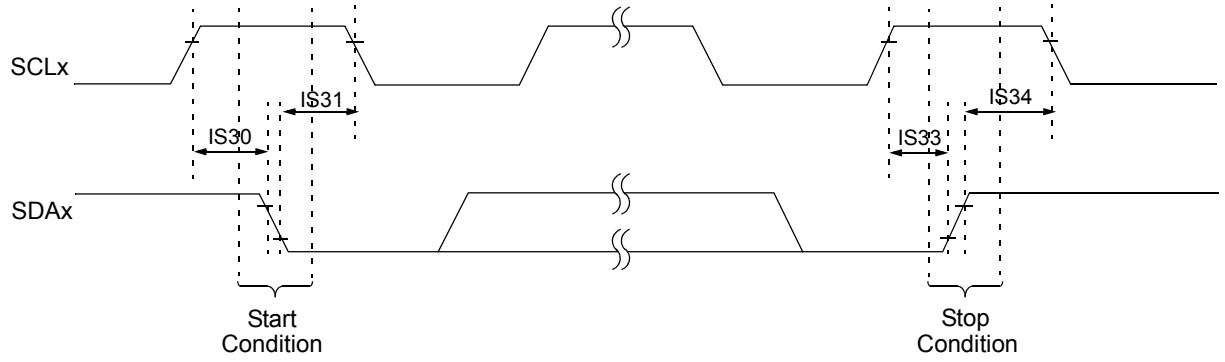
TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	Symbol	Characteristics		Min.(1)	Max.	Units	Conditions
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	nsec	—
			400 kHz mode	—	1000	nsec	—
			1 MHz mode (Note 2)	—	350	nsec	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	µs	
			1 MHz mode (Note 2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—

Note 1: BRG is the value of the I^2C™ Baud Rate Generator.

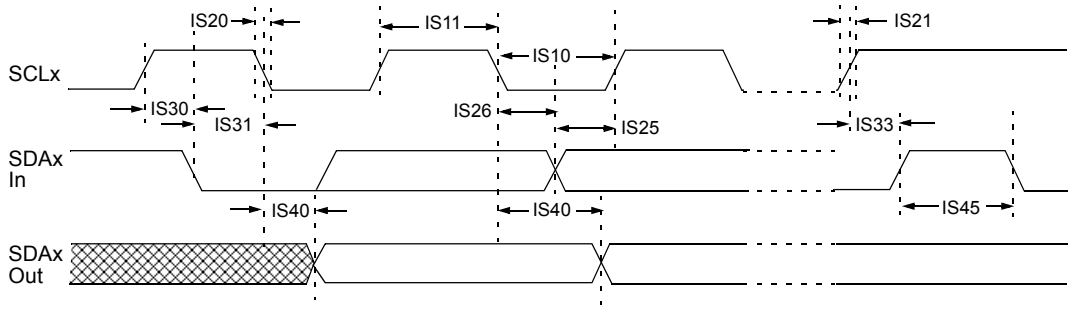
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 29-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 29-1 for load conditions.

FIGURE 29-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	PBCLK must operate at a minimum of 800 KHz.
			400 kHz mode	1.3	—	µs	PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode **(Note 1)**	0.5	—	µs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	PBCLK must operate at a minimum of 800 KHz.
			400 kHz mode	0.6	—	µs	PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode **(Note 1)**	0.5	—	µs	—
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	nsec	CB is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 CB	300	nsec	
			1 MHz mode **(Note 1)**	—	100	nsec	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	nsec	CB is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 CB	300	nsec	
			1 MHz mode **(Note 1)**	—	300	nsec	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	nsec	—
			400 kHz mode	100	—	nsec	
			1 MHz mode **(Note 1)**	100	—	nsec	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	nsec	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 1)**	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	µs	Only relevant for Repeated Start condition.
			400 kHz mode	600	—	µs	
			1 MHz mode **(Note 1)**	250	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	µs	After this period, the first clock pulse is generated.
			400 kHz mode	600	—	µs	
			1 MHz mode **(Note 1)**	250	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	µs	—
			400 kHz mode	600	—	µs	
			1 MHz mode **(Note 1)**	600	—	µs	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	nsec	—
			400 kHz mode	600	—	nsec	
			1 MHz mode (Note 1)	250		nsec	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	nsec	—
			400 kHz mode	0	1000	nsec	
			1 MHz mode (Note 1)	0	350	nsec	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	µs	
			1 MHz mode (Note 1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 29-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	**(Note 1)**
AD05a			2.5	—	3.6	V	VREFH = AVDD **(Note 3)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	**(Note 3)**
AD08	IREF	Current Drain	—	250 —	400 3	µA µA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with 1 kHz sinewave.

TABLE 29-34: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
		Leakage Current	—	±0.001	±0.610	µA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10KΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	**(Note 1)**
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V **(Note 2)**
AD23c	GERR	Gain Error	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24n	EOFF	Offset Error	—	—	<±1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed
ADC Accuracy – Measurements with Internal VREF+/VREF-							
AD20d	Nr	Resolution	10 data bits			bits	**(Note 3)**
AD21d	INL	Integral Nonlinearity	—	—	<±1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD22d	DNL	Differential Nonlinearity	—	—	<±1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Notes 2,3)**
AD23d	GERR	Gain Error	—	—	<±4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD24d	EOFF	Offset Error	—	—	<±2	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD25d	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	55	58.5	—	dB	**(Notes 3,4)**
AD34b	ENOB	Effective Number of Bits	9.0	9.5	—	bits	**(Notes 3,4)**

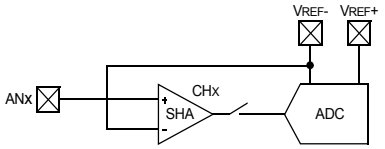
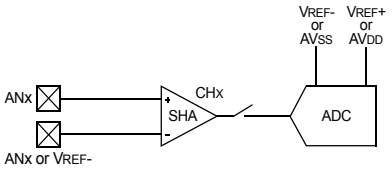
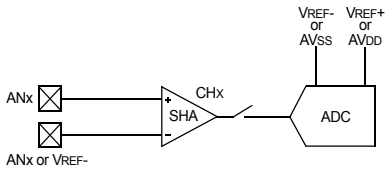
Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with 1 kHz sinewave.

TABLE 29-35: 10-BIT CONVERSION RATE PARAMETERS

PIC32MX 10-bit A/D Converter Conversion Rates (Note 2)						
ADC Speed	**TAD Minimum**	**Sampling Time Min**	**RS Max**	**VDD**	**Temperature**	**ADC Channels Configuration**
1 MIPS to 400 ksps **(Note 1)**	65 ns	132 ns	500Ω	3.0V to 3.6V	-40°C to +85°C	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	-40°C to +85°C	
Up to 300 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	-40°C to +85°C	

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

TABLE 29-36: A/D CONVERSION TIMING REQUIREMENTS

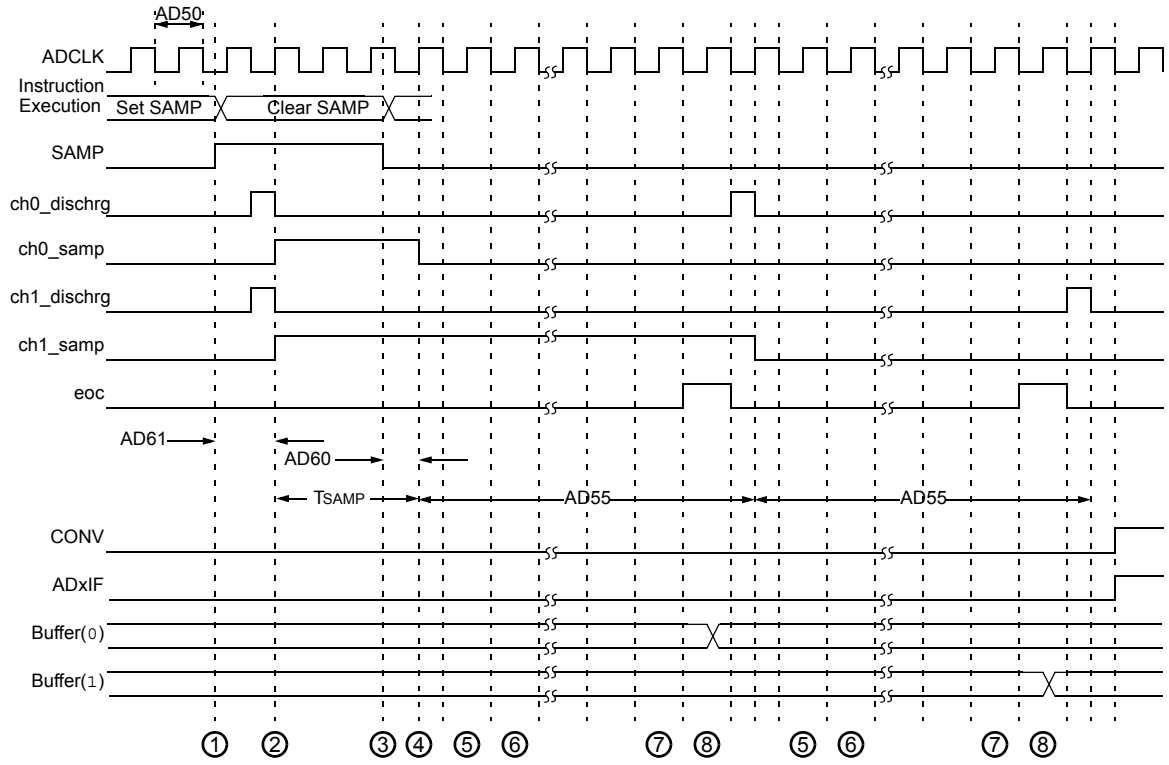
AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	A/D Clock Period **(Note 2)**	65	—	—	nsec	See Table 29-35.
AD51	TRC	A/D Internal RC Oscillator Period	—	250	—	nsec	**(Note 3)**
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	KSPS	AVDD = 3.0V to 3.6V
			—	—	400	KSPS	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1	—	31	TAD	TSAMP must be ≥ 132 nsec.
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger(3)	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected.
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) **(Note 3)**	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from A/D OFF to A/D ON **(Note 3)**	—	—	2	µs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

FIGURE 29-18: A/D CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000)



① – Software sets ADxCON. SAMP to start sampling.

② – Sampling starts after discharge period. TSAMP is described in the *"PIC32MX Family Reference Manual"* (DS61132).

③ – Software clears ADxCON. SAMP to start conversion.

④ – Sampling ends, conversion sequence starts.

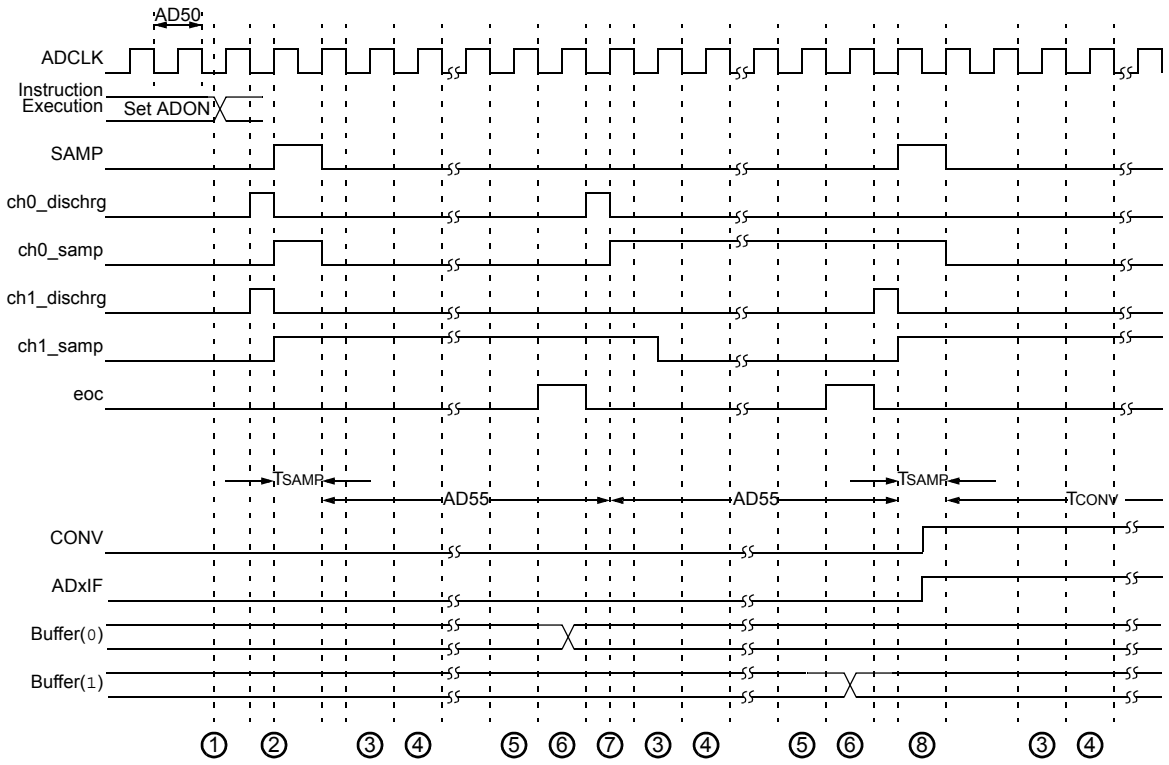
⑤ – Convert bit 9.

⑥ – Convert bit 8.

⑦ – Convert bit 0.

⑧ – One TAD for end of conversion.

FIGURE 29-19: A/D CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)



(1) – Software sets ADxCON. ADON to start AD operation.

(2) – Sampling starts after discharge period. TSAMP is described in the *"PIC32MX Family Reference Manual"* (DS61132).

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.

FIGURE 29-20: PARALLEL SLAVE PORT TIMING

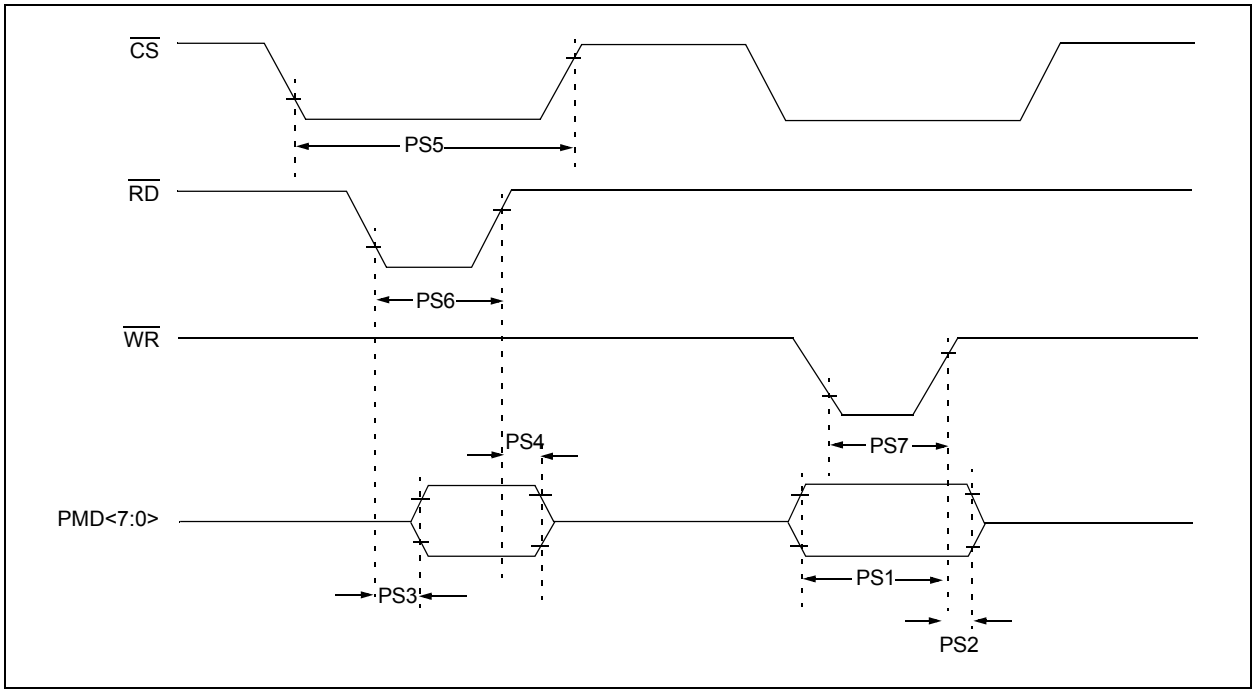


TABLE 29-37: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	nsec	—
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data – In Invalid (hold time)	40	—	—	nsec	—
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data – Out Valid	—	—	60	nsec	—
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data – Out Invalid	0	—	10	nsec	—
PS5	Tcs	$\overline{CS}$ Active Time	TPB + 40	—	—	nsec	—
PS6	TWR	$\overline{WR}$ Active Time	TPB + 25	—	—	nsec	—
PS7	TRD	$\overline{RD}$ Active Time	TPB + 25	—	—	nsec	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-21: PARALLEL MASTER PORT READ TIMING DIAGRAM

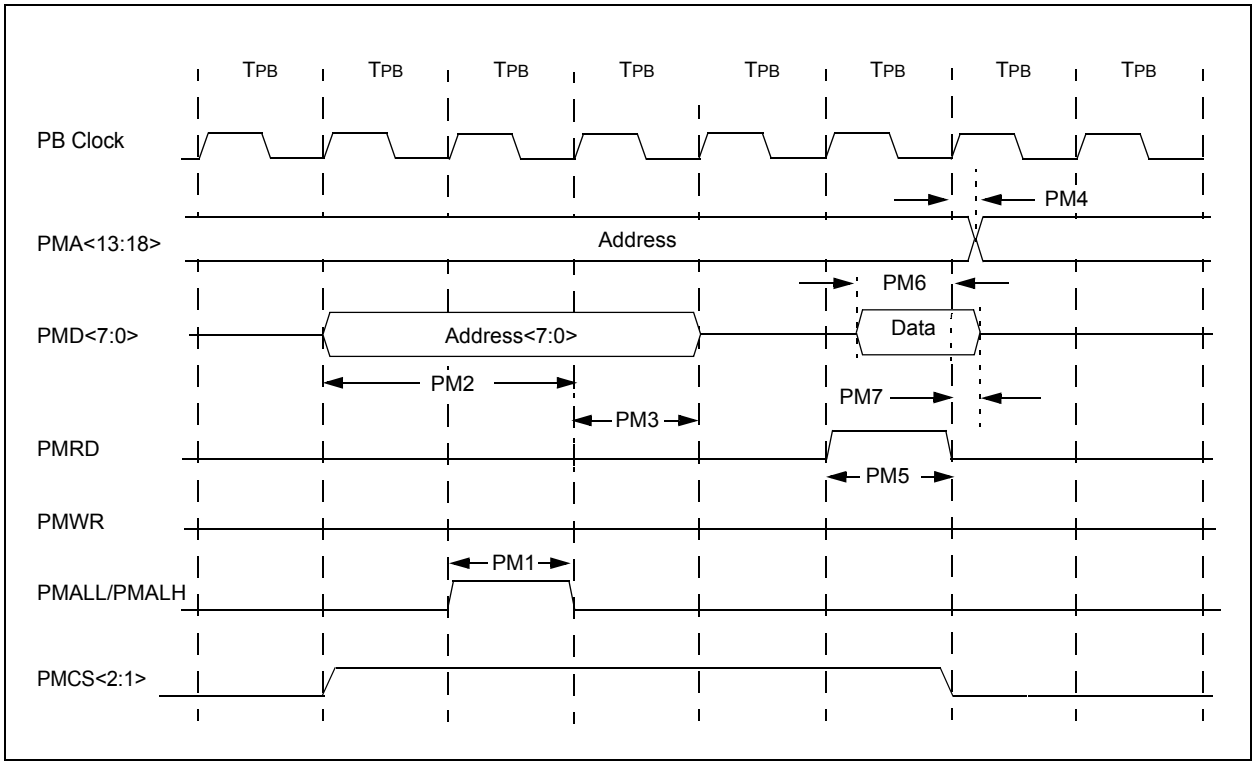


TABLE 29-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	nsec	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	nsec	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	nsec	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

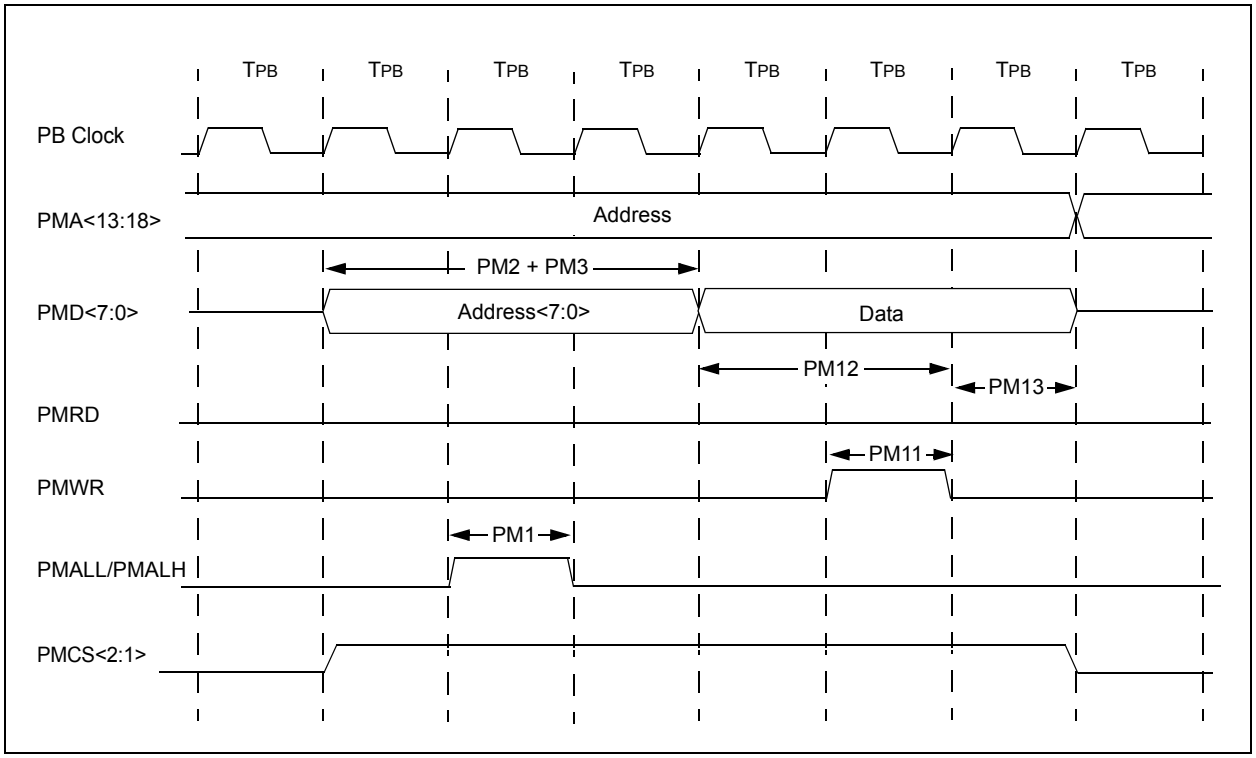


TABLE 29-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
PM11	TWR	PMWR Pulse Width	—	1 TPB	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPB	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPB	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 29-40: OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics(1)	Min.	Typ	Max.	Units	Conditions
USB313	VUSB	USB Voltage	3.0	—	3.6	V	Voltage on bus must be in this range for proper USB operation.
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	—
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	The difference between D+ and D- must exceed this value while VCM is met.
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	1.5 kΩ load connected to 3.6V.
USB322	VOH	Voltage Output High	2.8	—	3.6	V	1.5 kΩ load connected to ground.

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-23: EJTAG TIMING CHARACTERISTICS

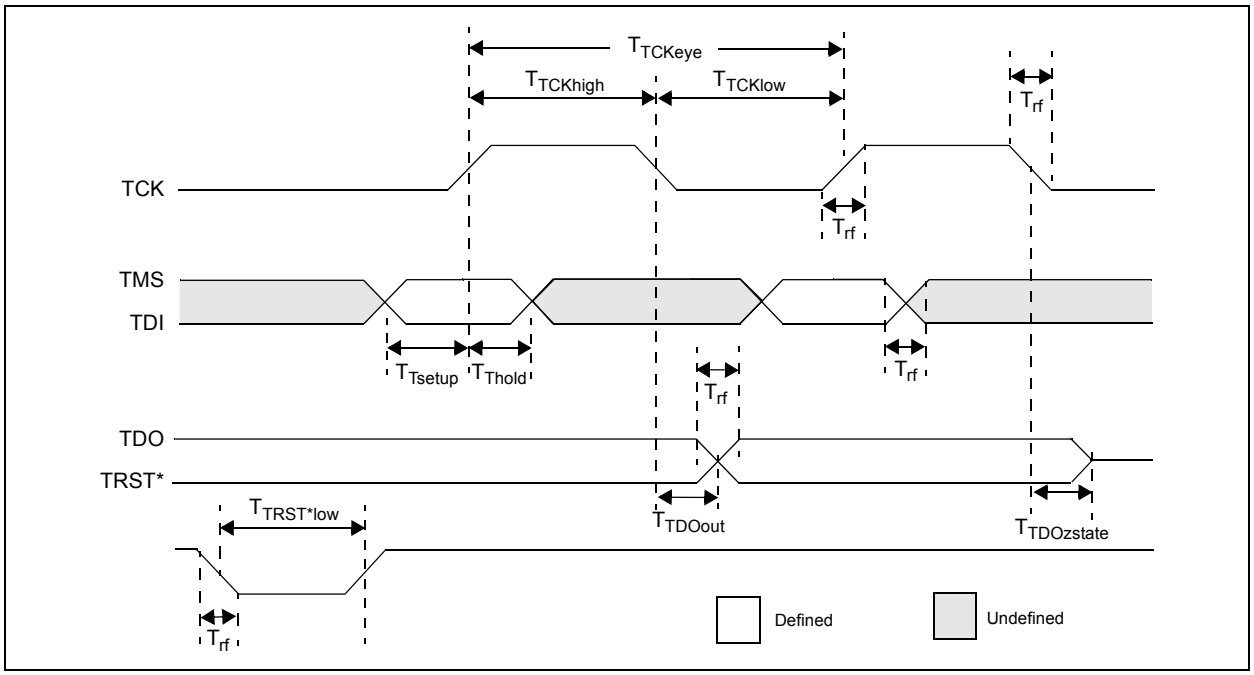


TABLE 29-41: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	Symbol	Description(1)	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	nsec	—
EJ2	TTCKHIGH	TCK High Time	10	—	nsec	—
EJ3	TTCKLOW	TCK Low Time	10	—	nsec	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	nsec	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	nsec	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	nsec	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	nsec	—
EJ8	TTRSTLOW	TRST Low Time	25	—	nsec	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	nsec	—

Note 1: These parameters are characterized, but not tested in manufacturing.

30.0 PACKAGING INFORMATION

30.1 Package Marking Information

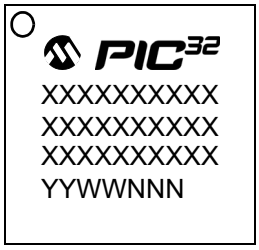
64-Lead TQFP (10x10x1 mm)

Example

100-Lead TQFP (12x12x1 mm)

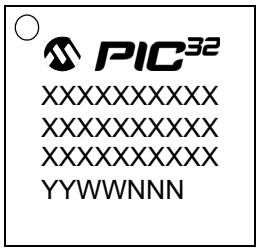
Example

64-Lead QFN (9x9x0.9 mm)



Example

121-Lead XBGA (10x10x1.1 mm)



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

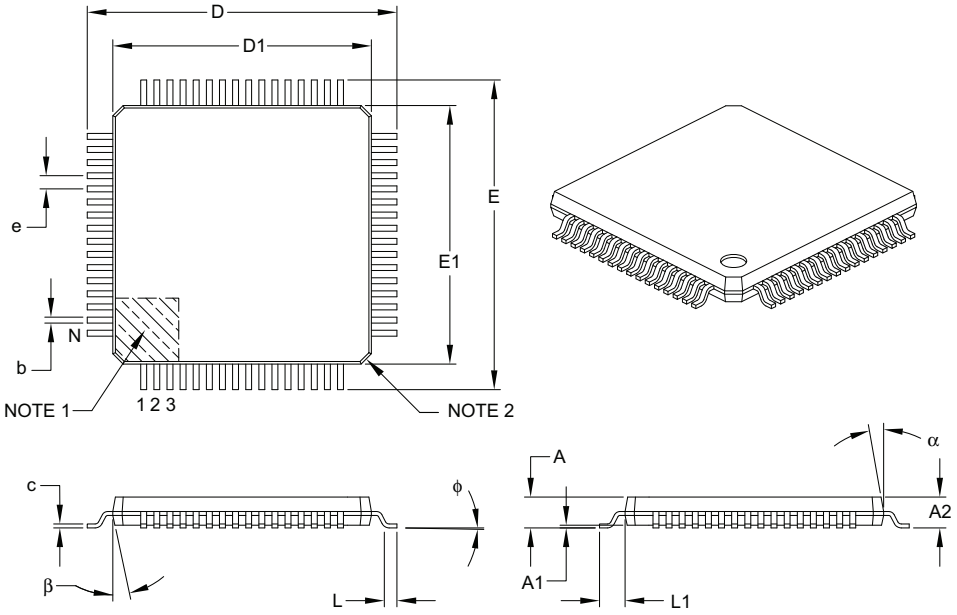
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

30.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

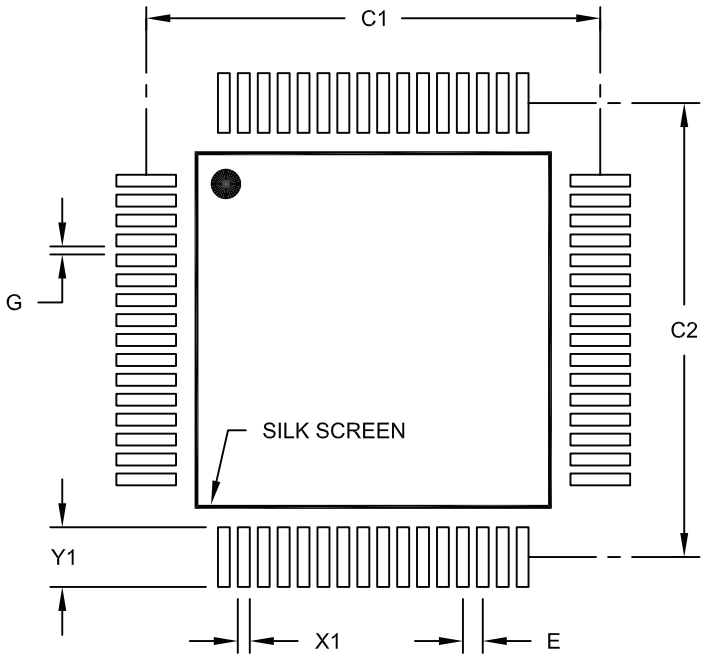
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

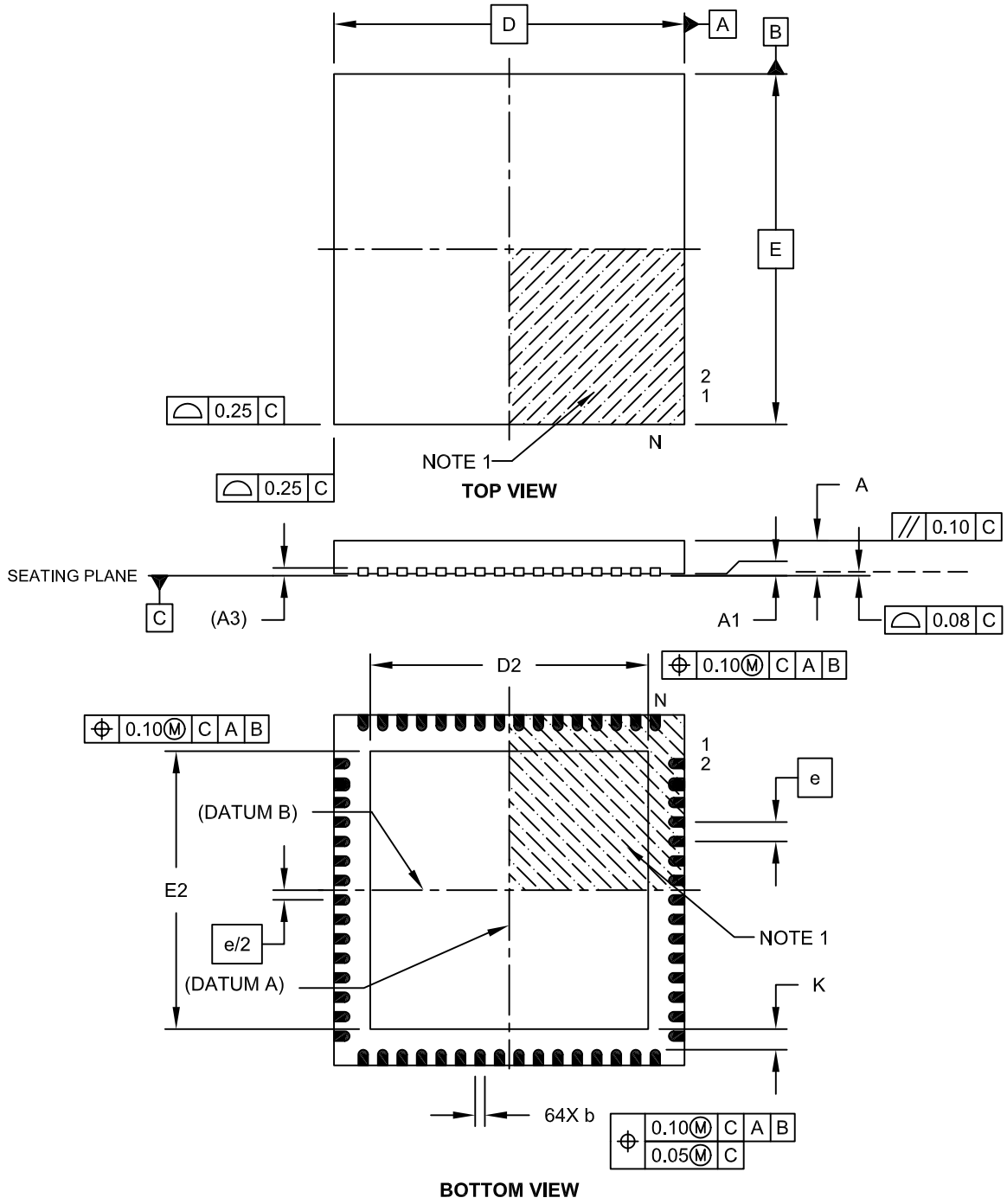
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085A

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

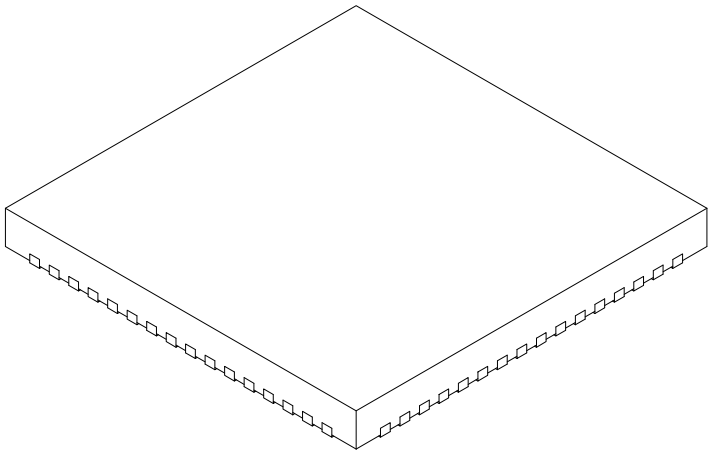
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149B Sheet 1 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

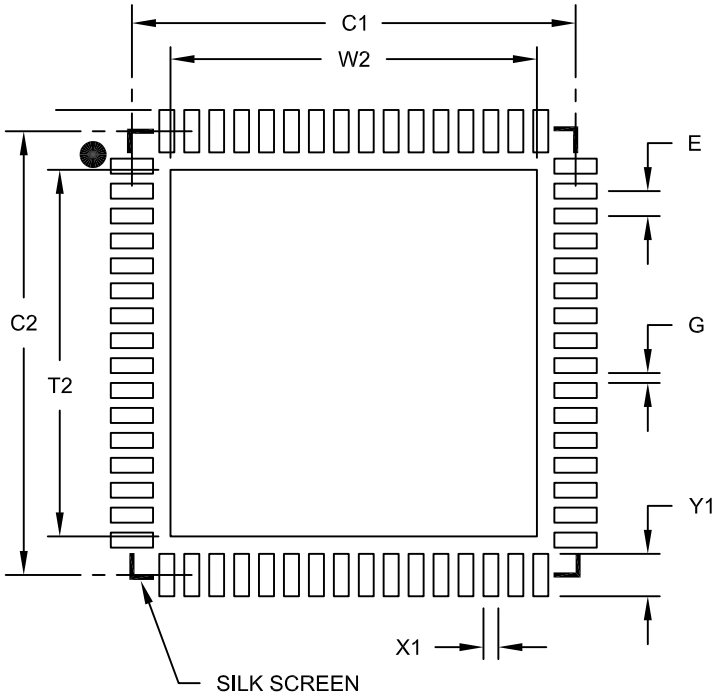
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149B Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

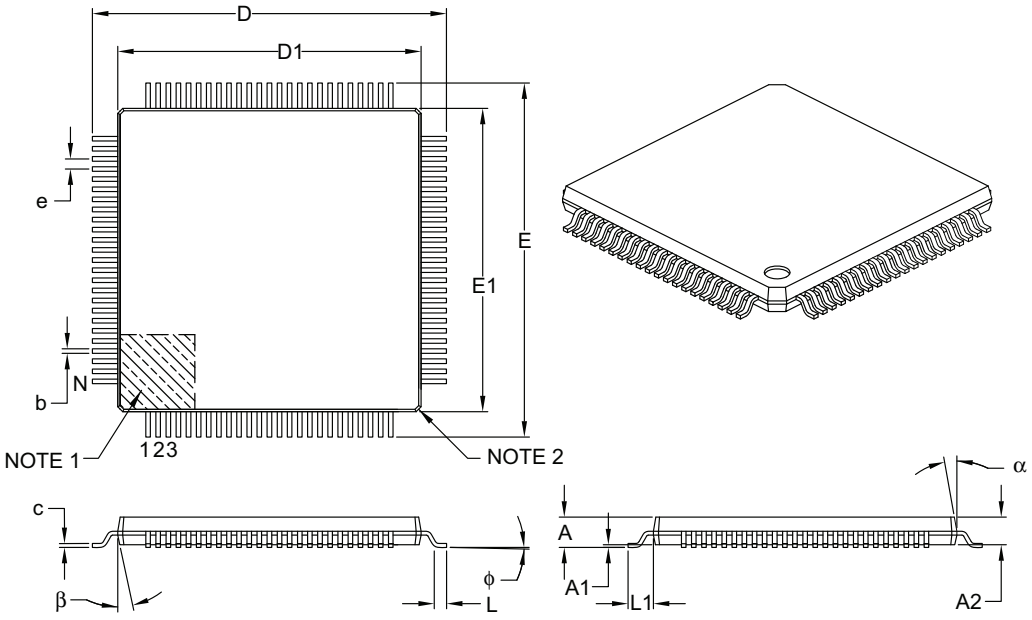
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

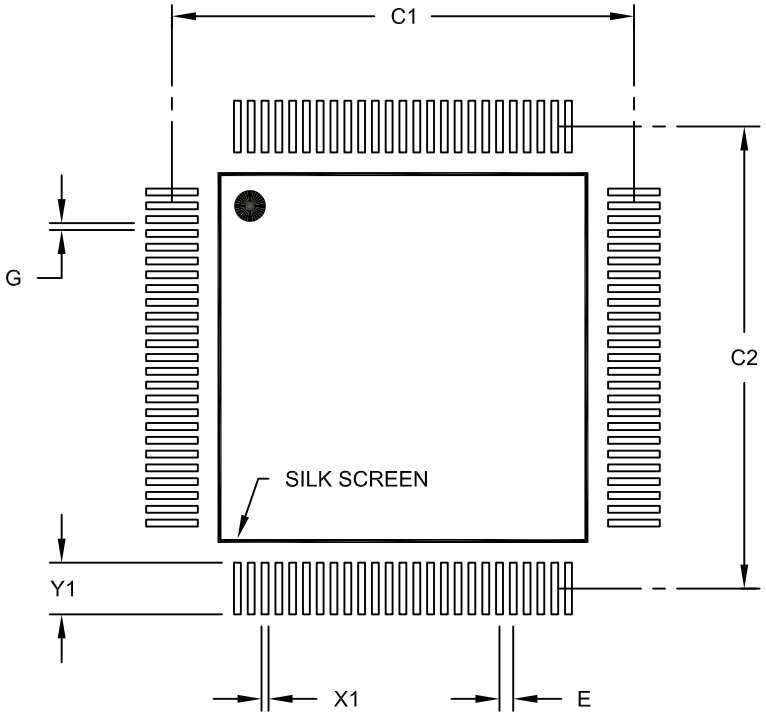
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

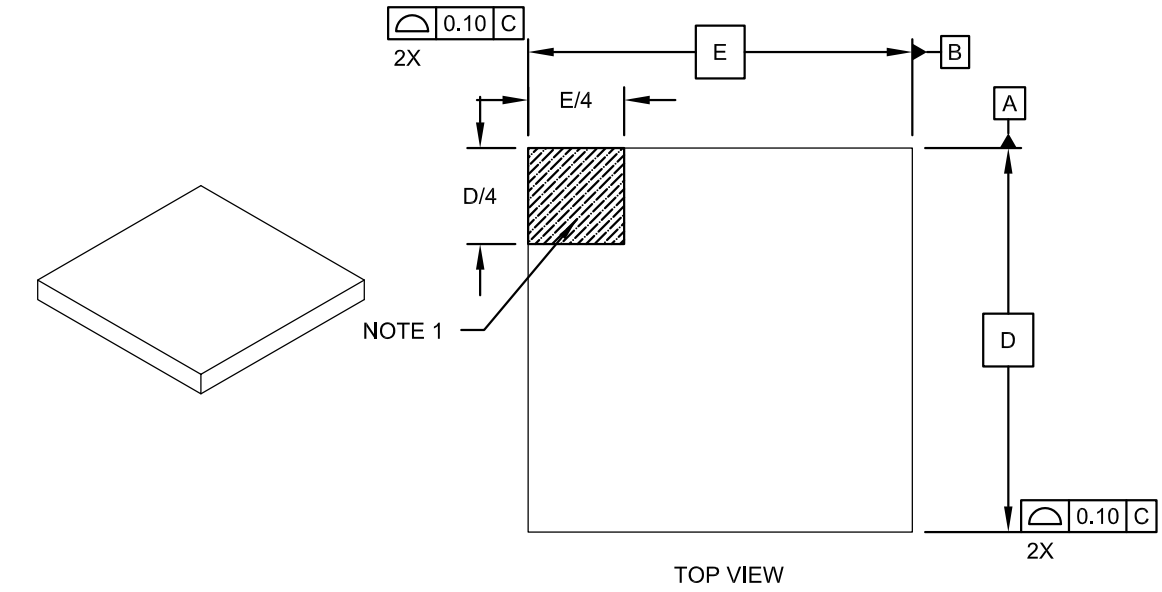
1. Dimensioning and tolerancing per ASME Y14.5M

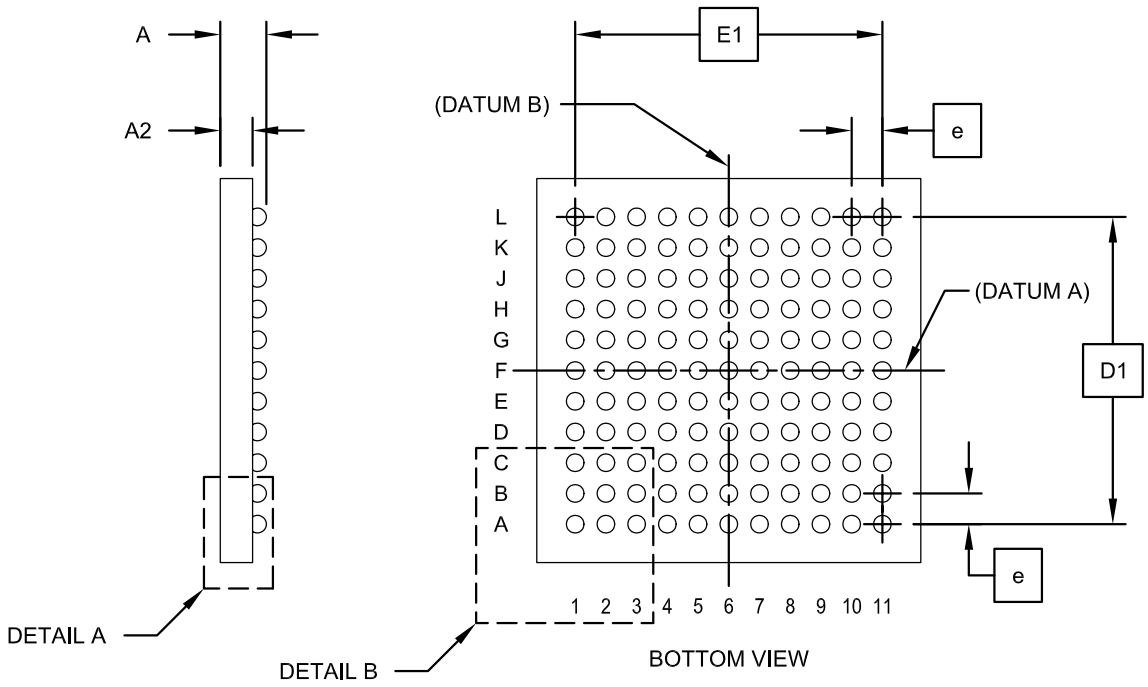
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100A

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

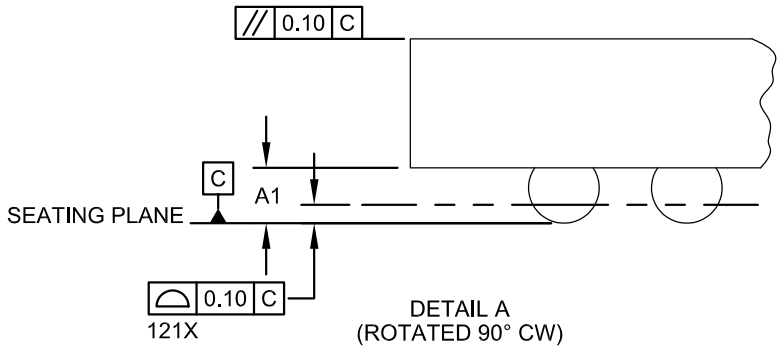


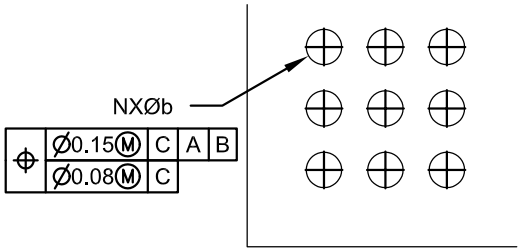


Microchip Technology Drawing C04-148A Sheet 1 of 2

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N		121	
Contact Pitch	e		0.80 BSC	
Overall Height	A	1.00	1.10	1.20
Standoff	A1	0.25	0.30	0.35
Molded Package Thickness	A2	0.55	0.60	0.65
Overall Width	E		10.00 BSC	
Array Width	E1		8.00 BSC	
Overall Length	D		10.00 BSC	
Array Length	D1		8.00 BSC	
Contact Diameter	b		0.40 TYP	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and colums of balls are located with respect to datums A and B.

Microchip Technology Drawing C04-148 Rev A Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision E (July 2008)

- Updated the PIC32MX340F128H features in Table 1 to include 4 programmable DMA channels.

Revision F (June 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSCI to OSC1 and OSCO to OSC2
- Changed all instances of V_{DDCORE} and V_{DDCORE}/V_{CAP} to V_{CAP}/V_{DDCORE}
- Deleted registers in most sections, refer to the related section of the *"PIC32MX Family Reference Manual"* (DS61132).

The other changes are referenced by their respective section in the following table.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, General Purpose and USB 32-bit Flash Microcontrollers"	Added a "Packages" column to Table 1 and Table 2. Corrected all pin diagrams to update the following pin names. • Changed PGC1/EMUC1 to PGEC1 • Changed PGD1/EMUD1 to PGED1 • Changed PGC2/EMUC2 to PGEC2 • Changed PGD2/EMUD2 to PGED2 Shaded appropriate pins in each diagram to indicate which pins are 5V tolerant. Added 64-Lead QFN package pin diagrams, one for General Purpose and one for USB.
Section 1.0 "Device Overview"	Reconstructed Figure 1-1 to include Timers, ADC and RTCC in the block diagram.
Section 2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Added a new section to the data sheet that provides the following information: • Basic Connection Requirements • Capacitors • Master Clear Pin • ICSP™ Pins • External Oscillator Pins • Configuration of Analog and Digital Pins • Unused I/Os
Section 4.0 "Memory Organization"	Updated the memory maps, Figure 4-1 through Figure 4-6. All summary peripheral register maps were relocated to **Section 4.0 "Memory Organization"**.
Section 7.0 "Interrupt Controller"	Removed the "Address" column from Table 7-1.
Section 12.0 "I/O Ports"	Added a second paragraph in **Section 12.1.3 "Analog Inputs"** to clarify that all pins that share ANx functions are analog by default, because the AD1PCFG register has a default value of 0x0000.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 26.0 "Special Features"	Modified bit names and locations in **Register 26-5 "DEVID: Device and Revision ID Register"**. Replaced "TSTARTUP" with "TPU", and "64-ms nominal delay" with "TPWRT", in **Section 26.3.1 "On-Chip Regulator and POR"**. The information that appeared in the Watchdog Timer and the Programming and Diagnostics sections of 61143E version of this data sheet has been incorporated into the Special Features section: • **Section 26.2 "Watchdog Timer (WDT)"** • **Section 26.4 "Programming and Diagnostics"**
Section 29.0 "Electrical Characteristics"	Added the 64-Lead QFN package to Table 29-3. Updated data in Table 29-5. Updated data in Table 29-7. Updated data in Table 29-4, Table 29-5, Table 29-7 and Table 29-8. Updated data in Table 29-10. Added OS42 parameter to Table 29-17. Replaced Table 29-23. Replaced Table 29-24. Replaced Table 29-25. Updated Table 29-36.
Section 30.0 "Packaging Information"	Added 64-Lead QFN package marking information to **Section 30.1 "Package Marking Information"**. Added the 64-Lead QFN (MR) package drawing and land pattern to **Section 30.2 "Package Details"**.
"Product Identification System"	Added the MR package designator for the 64-Lead (9x9x0.9) QFN.

Revision G (April 2010)

The revision includes the following global update:

- Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

This revision also includes minor typographical and formatting changes throughout the data sheet text. Major updates are referenced by their respective section in the following table.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, General Purpose and USB 32-bit Flash Microcontrollers"	Updated the crystal oscillator range to 3 MHz to 25 MHz (see **Peripheral Features:**) Added the 121-pin Ball Grid Array (XBGA) pin diagram. Updated Table 1: "PIC32MX General Purpose – Features" and Table 2: "PIC32MX USB – Features" Added the following tables: - Table 3: "Pin Names: PIC32MX320F128L, PIC32MX340F128L, and PIC32MX360F128L, and PIC32MX360F512L Devices", - Table 4: "Pin Names: PIC32MX440F128L, PIC32MX460F256L and PIC32MX460F512L Devices" Updated the following pins as 5V tolerant: - 64-pin QFN (USB): Pin 34 (VBUS), Pin 36 (D-/RG3) and Pin 37 (D+/RG2) - 64-pin TQFP (USB): Pin 34 (Vbus), Pin 36 (D-/RG3), Pin 37 (D+/RG2) and Pin 42 (IC1/RTCC/INT1/RD8) - 100-pin TQFP (USB): Pin 54 (VBUS), Pin 56 (D-/RG3) and Pin 57 (D+/RG2)
Section 1.0 "Device Overview"	Updated the Pinout I/O Descriptions table to include the device pin numbers (see Table 1-1)
Section 2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Updated the Ohm value for the low-ESR capacitor from less than 5 to less than 1 (see **Section 2.3.1 "Internal Regulator Mode"**). Labeled the capacitor on the VCAP/VDDCORE pin as CEFC in Figure 2-1. Changed 10 µF capacitor to CEFC capacitor in **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP/VDDCORE)"**.
Section 4.0 "Memory Organization"	Updated all register map tables to include the "All Resets" column. Separated the PORT register maps into individual tables (see Table 4-21 through Table 4-34). In addition, formatting changes were made to improve readability.
Section 12.0 "I/O Ports"	Updated the second paragraph of **Section 12.1.2 "Digital Inputs"** and removed Table 12-1.
Section 22.0 "10-bit Analog-to-Digital Converter (ADC)"	Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2).
Section 26.0 "Special Features"	Extensive updates were made to **Section 26.2 "Watchdog Timer (WDT)"** and **Section 26.3 "On-Chip Voltage Regulator"**.

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

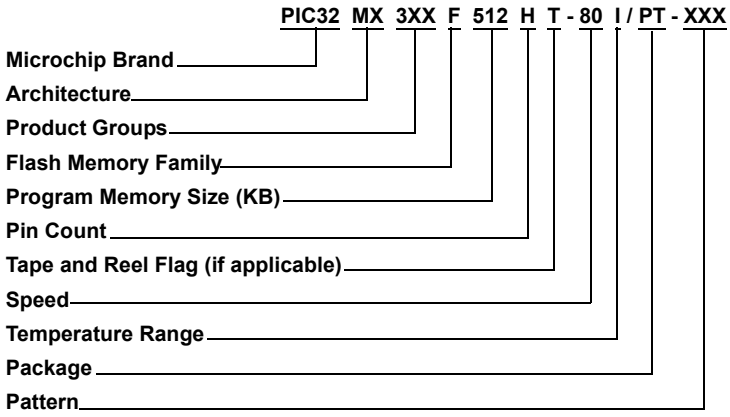
Section Name	Update Description
Section 29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings and added Note 3. Added Thermal Packaging Characteristics for the 121-pin XBGA package (see Table 29-3). Updated the conditions for parameters DC20, DC21, DC22 and DC23 in Table 29-5. Updated the comments for parameter D321 (CEFC) in Table 29-14. Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics, changing SP52 to SP35 between the MSb and Bit 14 on SDOx (see Figure 29-13).
Section 30.0 "Packaging Information"	Added the 121-pin XBGA package marking information and package details.
"Product Identification System"	Added the definition for BG (121-lead 10x10x1.1 mm, XBGA). Added the definition for Speed.

INDEX

W

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples:

PIC32MX320F032H-40I/PT:
General purpose PIC32MX,
32 KB program memory,
64-pin, Industrial temperature,
TQFP package.

PIC32MX360F256L-80I/PT:
General purpose PIC32MX,
256 KB program memory,
100-pin, Industrial temperature,
TQFP package.

	Flash Memory Family
Architecture	MX = 32-bit RISC MCU core
Product Groups	3XX = General purpose microcontroller family 4XX = USB
Flash Memory Family	F = Flash program memory
Program Memory Size	32 = 32K 64 = 64K 128 = 128K 256 = 256K 512 = 512K
Speed	40 = 40 MHz 80 = 80 MHz
Pin Count	H = 64-pin L = 100-pin
Temperature Range	I = -40°C to +85°C (Industrial)
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BG = 121-Lead (10x10x1.1 mm) XBGA (Plastic Thin Profile Ball Grid Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

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