PiRA RTC HAT

Power in Responsive Applications with RTC sleep mode.
Designed as a Raspberry Pi Zero HAT.

CONTENTS:

Version Revision:

v0.1   - 20.09.2017.
v0.2   - 31.10.2017.
v0.3   - 08.12.2017.

POWER DIAGRAM

IN: 5 VDC → Micro USB

IN: 6 VDC → Solar panel

Micro USB → LiPo CHARGER → LiPo BATTERY → BUCK BOOST OUT: 5 VDC → 5VDC
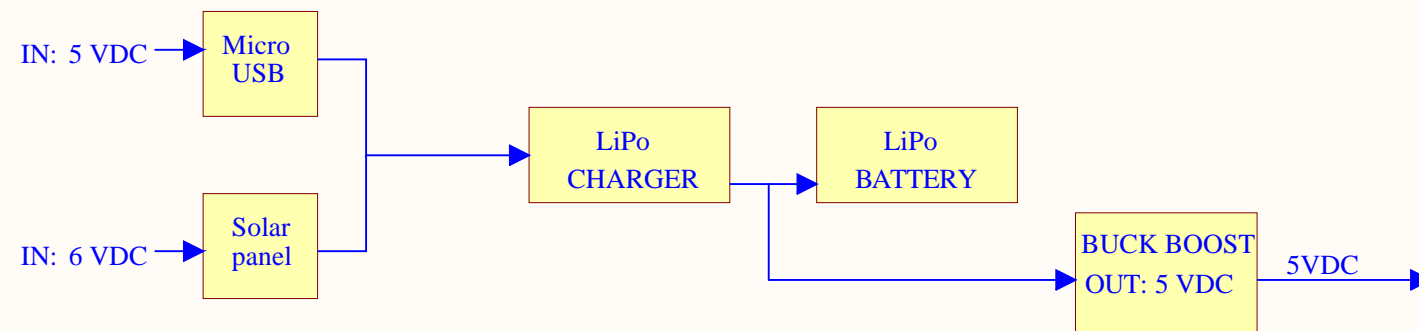
Solar panel → LiPo CHARGER

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational
design notes.

DESIGN NOTE:
Example text for critical
design notes.

LAYOUT NOTE:
Example text for critical
layout guidelines.

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Title: PiRA-RTC-HAT-PCB.PrjPcb

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POWER, RTC, RPI

CHARGER INPUTS

Wireless charger

Solar panel

CON1 microUSB
VBUS
GND
P3 Header 2
GND
D5 SE30AFG-M3/6A
D7 SE30AFG-M3/6A
D6 BZT52C6V2
R4 3k9
R12 10k
D2 3V
R30 10R
R16 10k
T1 MMBT3904
R13 470R
R1 470R
D1
R2 10R
NP

CHARGER

U1 BQ24296RGET
VBUS PMID REGN BTST SW SW
VBUS PGND
PSEL PGND
PG SYS
STAT SYS
SCL BAT
SDA BAT
INT OTG CE ILIM TS QON PAD
SCL SDA
C1 10uF /16V
C2 4u7/16V
C3 47n
L1 1.5uH
C4 10uF /16V
C5 10uF /16V
GND
VBAT
R6 5k6
R5 10k
P4 Header 2
R7 220R
R14 0R
R15 33k
GND

BATTERY CONNECTOR

VBAT
F1 3A
D4 RS1J-E3/61T..
P1 Header 2
GND

BOOST CONVERTER

ENABLE_5V
P2 Header 2
D3 1N4148W-7-F.
R34 1M2
C6 10uF /16V
C7 22u
C8 22u
C15 1uF
R9 470k
L2 1.5uH
U2 TPS630701RNMT
VIN VIN EN VSEL
VOUT VOUT FB2 FB
PS/S PG VAUX GND
L1 PGND L2
R10 10k
C12 100nF
R3 0R
R8 50k NP
C9 22u
C10 22u
C11 10uF /16V
+5V
GND

CHARGER (section labels)
CPU_SELF_EN_5V
U5
Q1 Q2
DMG6602SVT
VBAT
TIMER_EN_5V
ENABLE_5V
R23 47k
CHG EN VBUS
R24 0R
R38 100k
U6
Q1 Q2
DMG6602SVT
RTC_VCC
RTC_EN_5V
R25 47k

MOSFET OUT
VBAT J4 +5V
R17 100k
T2 SI7635DP-T1-GE3
R27 100R
GPIO_FET
R18 100R
T3 2N7002,215
R19 100k
FET_OUT
P7 Header 8
3.3V FET_OUT
TXD
RXD
GPIO_BCM5 +5V
GPIO_BCM6

BATTERY VOLTAGE
DESIGN NOTE:
The battery voltage is measured only when RPi has power, no current leakage.
ENABLE_5V
R26 470k
R29 470k
C13 3.3V
100nF
U4 MCP3021
VDD SCL
VSS
AIN SDA
SCL
SDA

Lora RFM95
U7
GND DIO2
MISO DIO1
MOSI DIO0
SCK 3V3
NSS DIO4
RESET DIO3
DIO5 GND
GND ANT
R35 10k LORA_DIO2_BCM7
R36 10k LORA_DIO1_BCM1
R37 10k LORA_DIO0_BCM12
3.3V
ANTENA
MISO MOSI SCK SPI_CSS LORA_RST

J1 Socket
ANTENA
CON2 CON3

LAYOUT NOTE:
One uFL connector is on TOP and second on BOTTOM

RPI CONNECTOR
3.3V P5 +5V
SDA
SCL
RST_RTC
TXD
RXD
TIMER_EN_5V R32 470k CPU_SELF_EN_5V
TIMER_DONE
RTC_EN_5V R33 470k GPIO_FET
R39 10k R40 10k
MOSI
MISO GPIO_BCM25
SCK
SPI_CSS
LORA_DIO2_BCM7
LORA_DIO1_BCM1
GPIO_BCM5
GPIO_BCM6
LORA_RST
LORA_DIO0_BCM12
Header 20X2

RTC
U3 DS3231M
33KHZ SCL
VCC SDA
INT/SQW VBAT
RST GND
N.C. N.C.
N.C. N.C.
N.C. N.C.
N.C. N.C.
VBAT
J3
+5V
RST_RTC R28 0R
R22 10k
C14 100nF
RTC_VCC
RTC_EN_5V
R20 10k R21 10k
3.3V
P9 Header 2
SCL SDA

TIMER
DESIGN NOTE:
2h timer
VBAT J2 VBAT
U8 TPL5110
VDD EN/ONE_SHOT
GND DRV
DELAY/M_DRV DONE
R31 169k
TIMER_EN_5V
TIMER_DONE
R11 10k
GND

DESIGN NOTE:
Jumper to select ONE_SHOT mode of the TPL5110
HIGH - works as timer
LOW - the TPL5110 turns on the MOSFET one time for the programmed time interval. The next power on of the MOSFET is enabled by the manual power ON.

I2C/DISPLAY
P6 Header 4
SDA
SCL
3.3V

SENSOR
3.3V P8 Header 3
GPIO_BCM25
GND

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65.00

30.00

65.00

30.00

J1

P5 R20 R21 R28 R37 R36 R35   R38 R23 R40 C13   C10   C9   C5   C4   R15   P4

CON3   R24   R32   U4   C11   R3   R8   U1   R6 R7   R5

P9   C12   R2 R14 R13

GND SCL SDA   R32   U2   C15 R9 R10   L1   CHG

3V3   P6   U6 R31   U5 R29   L2   C6 D2   R4   T1   C1

R18   R11   C8   C3   R1

T2 R33   V3   T3   T2 U8   D4 C7   P2   R16 R12   D1

R19   R27 R17   D3   R34   C2   R30

R22 J3   R25   R39   C14   J4   P8   P3   P1   SOLAR D5

P7   CON1

IO6 IO5 5V GND RX TX 3V3 OUT 3V3 IO25 GND   + BAT -   -   +

PiRA Zero

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v0.3

No.

CERN OHL

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U7

F1