SmartParks Elephant LoRa

Lora module for elephant tracker

CONTENTS:

Version Revision:

V1   - 12.06.2019.

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational
design notes.

DESIGN NOTE:
Example text for critical
design notes.

LAYOUT NOTE:
Example text for critical
layout guidelines.

IRNAS	www.irnas.eu	
SmartParks Elephant LoRa		
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LORA MODULE

EEPROM WITH EUI

EXPANSION CONNECTOR

DESIGN NOTE:
DIO1, DIO2 are GPIO, configurable for multiple functions ; DIO2 can connect to TXEN, without connecting to IO of MCU, for controlling RF switch TX, Please see more in SX126x datasheet, can be floated when free.

DESIGN NOTE:
E22(433M22S) uses DIO3 internally to power 32MHz TCXO.

DESIGN NOTE:
On module uFL connector is used for antenna.

DESIGN NOTE:
In this schematic the single band topologie (ISM 868) is implemented.
There is a option for dual band matching sircuit without changing the PCB. For further information please see the antena datasheet.

U2 — CMWX1ZZABZ

GND, TCXO_VCC, TCXO_OUT, PH0-OSC_IN, PH1-OSC_OUT, BOOT0
PA14/SWCLK, PA13/SWDIO, PB5/LPTIM1_IN1, PB6/LPTIM1_ETR, PB7/LPTIM1_IN2, PB2/LPTIM1_OUT

GND 54
GND 55
GND 56
GND 57

1 PA12/USB_DP
2 PA11/USB_DM
3 GND
4 VDD_USB
5 VDD_MCU
6 VDD_RF
7 GND
8 DBG_SX1276_DIO2
9 DBG_SX1276_DIO3
10 SX1276_DIO4
11 DBG_SX1276_DIO5
12 DBG_SX1276_DIO0

36 PB9/I2C1_SDA — I2C1_SDA
35 PB8/I2C1_SCL — I2C1_SCL
34 MCU_nRST — RESET
33 PA0/WKUP1 — LED
32 VREF+
31 STSAFE_nRST
30 DBG_CRF2
29 DBG_CRF3
28 DBG_CRF1
27 GND
26 ANT — LORA_ANT
25 GND

DBG_SX1276_DIO0, PB15/SPI2_MOSI, PB14/SPI2_MISO, PB13/SPI2_SCK, PB12/SPI2_NSS, PA10/USART1_RX, PA9/USART1_TX, PA8/MCO, PA5/ADC5/DAC2, PA4/ADC4/DAC1, PA3/ADC3, PA2/ADC2

SPI2_MOSI, SPI2_MISO, SPI2_NSS, USART1_RX, USART1_TX, LORA_RST, LORA_BUSY, BAT_AN, MCU_IO1, UART2_TX

U1 — E22-900M22S

9 VCC
21 ANT
15 NRST — LORA_RST
19 NSS — SPI2_NSS
18 SCK — SPI2_SCK
17 MOSI — SPI2_MOSI
16 MISO — SPI2_MISO
1 GND
2 GND
3 GND
4 GND
5 GND
10 GND
11 GND
12 GND
22 GND
20 GND
6 RXEN — RXEN
7 TXEN
14 BUSY — LORA_BUSY
13 DIO2 — DIO2
DIO1

U3 — 24AA02E48T-I/OT

1 SCL — I2C1_SCL
3 SDA — I2C1_SDA
5 NC
4 VCC — VMCU
2 VSS

U4 — MCP1810T

7 VIN
8 SHDN
2 OUT
6 FB
GND GND

A1 — SR42I010-R

2/1 FEED B_SEL
7, 6, 5, 3, 4

CON1

1 VMCU
2 SWDIO
3 RESET
4 SWCLK
5
6 UART2_TX

P1

VCC_EXT
1
2
3
4 MCU_IO1
5 USART1_RTS
6 USART1_CTS
7 USART1_RX
8 USART1_TX
9
10
11 M1
12 M2

P2 — Header 4

1 VMCU
2 I2C1_SCL
3 I2C1_SDA
4

P3

MP2
MP1
2 VBAT
1

J1 Selector
3 VMCU
1 VBAT
2

Components:
R1 10k, R4 10k, R6 4k7, R7 4k7, R8 75k, R9 100R, R10 100R, R11 100k, R12 100k, R2 0R, R3 0R, R5 0R
C1 100nF, C2 1uF, C3 100nF, C4 10uF, C5 1uF, C6 100nF, C7 1uF, C8 2.2uF 6V3, C9 100nF, C10 10nF, C11 2.2uF, C12 2.2uF
L1 NC, L2 NC, L3 4.3nH
T1 2N7002ET1G
D1 RED
S1

Signals: BAT_MON_EN, BOOT0, SWCLK, SWDIO, DIO2, RXEN, USART1_CTS, USART1_RTS, TXEN, VMCU, VBAT, GND, NC, LORA_RST, BAT_AN