Group 10
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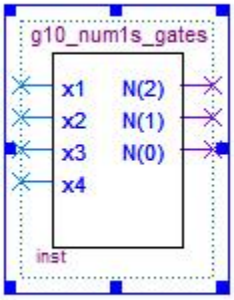
ECSE 323 – Digital Systems Design
Lab 1 Report - G10_num1s

Description of circuit function

This circuit takes in a 4 bit input vector denoted as x1x2x3x4 (with x1 being the MSB and x4 the LSB) and outputs a 3 bit vector representing the number of 1's in the input in binary (N(0) being the LSB and N(2) the MSB). Therefore, a 1001 input would give 010 as an output and a 1000 would output 001. Overall, there are 16 possible inputs and 5 possible outputs (0, 1, 2, 3, and 4 possible '1's in the input). As it is, it is possible for different inputs to give the same output. In order to get the output, different inputs were grouped together. For example, N(0) would equal '1' only if the input contained either 1 or 3 '1's. N(1) would be '1' if the input contained 2 '1's. Finally, N(2) would equal '1' if the input contained 4 '1's. This information was used in a Karnaugh map in order to find the minimal sum-of-products equation for each of the 3 output bits.

Symbol diagram



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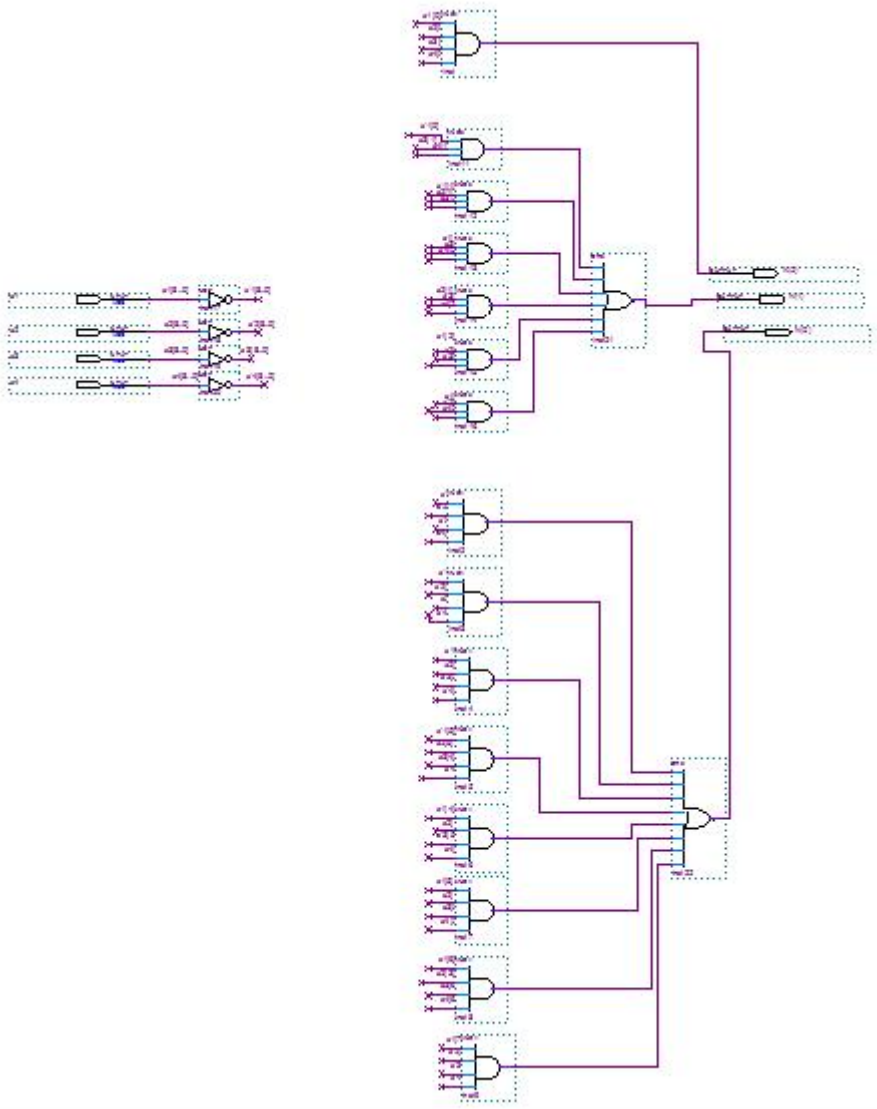
Gate level diagram



Circuit testing

The num1s circuit was tested by creating a VHDL file describing the logic function of the circuit and then a testbench file in Quartus II. The testbench file was modified to test all 16 possible inputs using a for loop and then it was imported to Modelsim where it was compiled. The compiled file in the ‘work’ folder would then be imported to the simulation page. Pressing on the wave function and dragging the inputs and the outpus to the wave page, displayed the below simulation plot, when the ‘run’ button was pressed.

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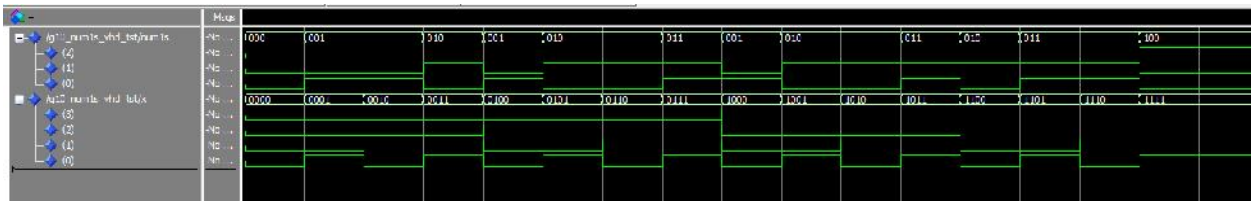

How do we know that the circuit worked?

We knew that the circuit was working correctly because there were no red lines under any numbers in the simulation, we double checked that each input corresponded to the right output, and the simulation displayed all the 16 possible inputs.