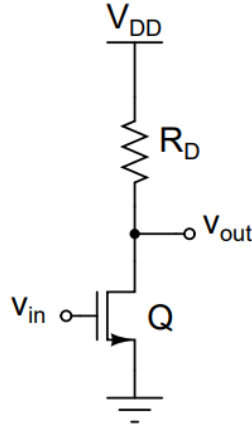


Solution of Tutorial Sheet No. 5

- Design a following circuit (specify the required values of V_{DD} , R_D and W/L) such that high and low output voltages equal to $V_{OH} = 2V$ and $V_{OL} = 0.1V$, respectively, are obtained, and so that the current drain from the supply in the low-output state is $20\mu A$. The transistor has $V_t = 0.5V$ and $\mu_n C_{ox} = 100\mu A/V^2$.



ANSWER:

$$\begin{aligned}
 V_{DD} &= V_{OH} = \boxed{2.0V} \\
 i_D &= \frac{V_{DD} - V_{OL}}{R_D} \rightarrow R_D = \frac{2.0V - 0.1V}{20\mu A} = \boxed{95k\Omega} \\
 i_D &= 20\mu A = \frac{1}{2}(\mu_n C_{ox})(W/L)(2(v_{GS} - V_t)v_{DS} - v_{DS}^2) \\
 \frac{W}{L} &= \frac{20\mu A}{\frac{1}{2}(100\mu A/V^2)(2(2V - 0.5V)(0.1V) - (0.1V)^2)} \simeq \boxed{1.38/1}
 \end{aligned}$$

- Design a CMOS inverter for the following specifications: $k_n = 0.2mA/V^2$, $V_M = 1.47V$, $V_{tn} = |V_{tp}| = 0.6V$, $V_{DD} = 3.3V$. Consider $\mu_n = 2.5\mu_p$

pMOS	nMOS
$W/L = ?$	$W/L = ?$

Solution: For given parameters, $k_p = 0.1mA/V^2$. Using k_n and k_p values, the values of W/L for each transistor can be calculated.

3. Consider a CMOS inverter circuit with the following parameters:

$$\begin{aligned} V_{DD} &= 3.3 \text{ V} \\ V_{T0,n} &= 0.6 \text{ V} \\ V_{T0,p} &= -0.7 \text{ V} \\ k_n &= 200 \mu\text{A/V}^2 \\ k_p &= 80 \mu\text{A/V}^2 \end{aligned}$$

Calculate the noise margins for the circuit.

Solution:

First, the output low voltage V_{OL} and the output high voltage V_{OH} are found, using (5.54) and (5.55), as $V_{OL} = 0$ and $V_{OH} = 5 \text{ V}$. To calculate V_{IL} in terms of the output voltage, we use (5.62).

$$\begin{aligned} V_{IL} &= \frac{2 V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R} \\ &= \frac{2 V_{out} - 0.7 - 3.3 + 1.5}{1 + 2.5} = 0.57 V_{out} - 0.71 \end{aligned}$$

Now substitute this expression into the KCL equation (5.59).

$$2.5(0.57 V_{out} - 0.71 - 0.6)^2 = 2(0.57 V_{out} - 0.71 - 3.3 + 0.7)(V_{out} - 3.3) - (V_{out} - 3.3)^2$$

This expression yields a second-order polynomial in V_{out} , as follows:

$$0.66 V_{out}^2 + 0.05 V_{out} - 6.65 = 0$$

Only one root of this quadratic equation corresponds to a physically correct solution for V_{out} (i.e., $V_{out} > 0$).

$$V_{out} = 3.14 \text{ V}$$

From this value, we can calculate the critical voltage V_{IL} as:

$$V_{IL} = 0.57 \cdot 3.14 - 0.71 = \underline{\underline{1.08 \text{ V}}}$$

To calculate V_{IH} in terms of the output voltage, use (5.67):

$$\begin{aligned} V_{IH} &= \frac{V_{DD} + V_{T0,p} + k_R \cdot (2 V_{out} + V_{T0,n})}{1 + k_R} \\ &= \frac{3.3 - 0.7 + 2.5(2 V_{out} + 0.6)}{1 + 2.5} = 1.43 V_{out} + 1.17 \end{aligned}$$

Next, substitute this expression into the KCL equation (5.64) to obtain a second-order polynomial in V_{out} .

$$2.5[2(1.43 V_{out} + 1.17 - 0.6) V_{out} - V_{out}^2] = (1.43 V_{out} - 1.43)^2$$

$$2.61 V_{out}^2 + 6.94 V_{out} - 2.04 = 0$$

Again, only one root of this quadratic equation corresponds to the physically correct solution for V_{out} at this operating point, i.e., when $V_{in} = V_{IH}$.

$$V_{out} = 0.27 \text{ V}$$

From this value, we can calculate the critical voltage V_{IH} as:

$$V_{IH} = 1.43 \cdot 0.27 + 1.17 = \underline{\underline{1.55 \text{ V}}}$$

Finally, we find the noise margins for low voltage levels and for high voltage levels using (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 1.08 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 1.75 \text{ V}$$