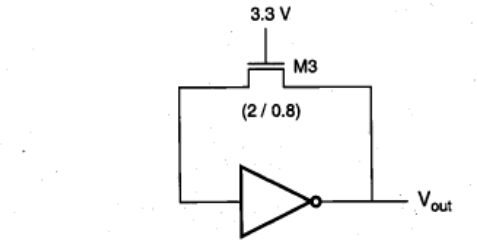
MOS Circuit Design UEC750

Tutorial Sheet No. 5

1. Consider the CMOS inverter shown below:



Derive an expression for Vout.

2. Consider a CMOS inverter, with the following device parameters:

nMOS	$V_{T0,n} = 0.6$ V	$\mu_n C_{ox} = 60\ \mu A/V^2$
pMOS	$V_{T0,p} = -0.8$ V	$\mu_p C_{ox} = 20\ \mu A/V^2$
Also:	$V_{DD} = 3$ V	
	$\lambda = 0$	

Determine the (W/L) ratios of the nMOS and the pMOS transistor such that the switching threshold is V_{th} = 1.5 V.

3. Design a CMOS inverter for the following specifications: k_n =0.2mA/V^2, V_M = 1.47V, Vtn=|Vtp|=0.6V, VDD=3.3V. Consider $\mu_n=2.5\mu_p$

pMOS	nMOS
W/L = ?	W/L = ?

4. Consider a CMOS inverter circuit with the following parameters:

$V_{DD} = 3.3$ V
$V_{T0,n} = 0.6$ V
$V_{T0,p} = -0.7$ V
$k_n = 200\ \mu A/V^2$
$k_p = 80\ \mu A/V^2$

Calculate the noise margins for the circuit.