for optimal "stacking" of sc-graphs into processormemory to ensure the subsequent efficiency of message transmission between processor elements

- Since the configuration of *logical communication channels* changes during the processing of sc-constructions, it is also advisable to talk about the development of algorithms for repositioning ("defragmentation") of the sc-construction already recorded in the processor-memory in order to ensure the subsequent efficiency of message transmission. Such reallocation can be performed, for example, according to a schedule during a period when the processor-memory is not used for solving other problems.
- In addition, if there is a hardware capability, *the physical communication channels* can also be reswitched in order to approximate their configuration to the configuration of *logical communication channels*.

Let us consider an example of the optimal variant of writing the simplest *five-element sc-construction* into the proposed processor-memory within the fine-grained architecture of *associative semantic computers*.

In Figure 2, the record of some *five-element sc-construction* in the SCg-code is shown.

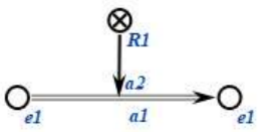

Figure 2. SCg-text. Example of a *five-element sc-construction*

In Figure 3, an incidence graph for the same *five-element sc-construction* is shown, which allows reducing the sc-construction to a classical graph with two types of connections. For clarity, the syntactic types of the corresponding sc-elements are not shown in the Figure.

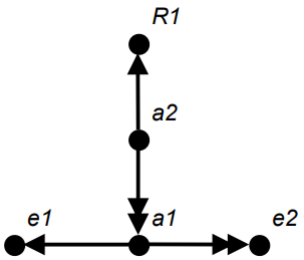

Figure 3. Incidence graph for a *five-element sc-construction*

In Figure 4, one of the possible optimal options for recording the resulting incidence graph into processormemory is shown. Dotted lines show *physical communication channels* between processor elements, solid lines show *physical communication channels* corresponding to *logical communication channels*. Note that it is advisable to record element R1 in the *processor element* adjacent to the *processor element* storing element e1 or element e2, as shown in the Figure. Due to this, the processor elements storing the specified sc-elements are directly connected by a *physical communication channel*, which simplifies communication in the case of sending messages via *physical communication channels* without taking into account *logical communication channels*.

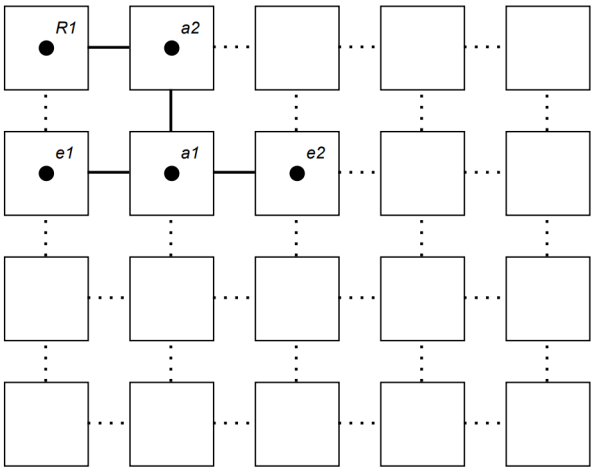

Figure 4. Example of stacking an sc-construction into a processormemory

VI. Conclusion

In the article, the disadvantages of the currently dominant von Neumann architecture of computer systems as a basis for building-up intelligent computer systems of a new generation are considered, the analysis of modern approaches to the development of hardware architectures that eliminate some of these disadvantages is carried out, the need for the development of fundamentally new hardware architectures representing a hardware implementation of ostis-platforms – *associative semantic computers* – is demonstrated.

The general principles underlying *associative semantic computers* are proposed, three possible variants of the architecture of such computers are considered, their advantages and disadvantages are represented.

Further development of the approaches proposed in the work requires solving a number of problems, both technical and organizational ones:

- development of a wave language for recording microprograms, that are exchanged between processor elements and run by these processor elements;
- development of a language for writing programs for controlling the exchange of micro-programs and managing the queue of micro-programs;
- organization of active participation of specialists in the field of microelectronics in clarifying the principles of implementation of processor elements and

processor-memory in general, clarifying the element base and lower-level architectural features of *associative semantic computers*;
- development of algorithms for optimizing the ways of recording sc-constructions to processor-memory and repositioning already recorded sc-constructions in order to ensure the subsequent efficiency of message transmission between processor elements;
- clarification of the typology of information processes in the processor-memory, their features, and the corresponding typology of labels;
- clarification of the principles of implementing multiagent knowledge processing within the processormemory, in particular, the development of principles for implementing event-based information processing in such memory.

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