Problem 1.

For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

1. What is the cache block size (in words)?

$2^{5-2} = 8$ words

2. How many entries does the cache have?

$2^5 = 32$ entries

3. Ratio

$\frac{22+3+256}{256} \approx 1.09$

4.

4

5.

4/12=0.33

ADDR	INDEX	TAG	Replace	Hit
0	00000=0	0		
4	00000=0	0		Y
16	00000=0	0		Y
132	00100=4	0		
232	00111=7	0		
160	00101=5	0		
1024	00000=0	1	Y	
30	00000=0	0	Y	
140	00100=4	0		Y
3100	00000=0	3	Y	
180	00101=5	0		Y
2180	00100=4	2	Y	

6.

INDEX	Tag	Data
0	3	3072-3103
4	2	2176-2207
5	0	160-191
7	0	224-255

We only list the non-empty cache blocks.

Problem 2.

1.
   - offset: 2-0
   - index: 4-3
   - tag: 31-5
2.

Addr	Bin	Index	Tag	Block	H | M
3	00000011	00=0	0	0	M
180	10110100	10=2	5	0	M
43	00101011	01=1	1	0	M
2	00000010	00=0	0	0	H
191	10111111	11=3	5	0	M
88	01011000	11=3	2	1	M
190	10111110	11=3	5	0	H
14	00001110	01=1	0	1	M
181	10110101	10=2	5	0	H

	block0	block1	block2
set-0	mem[0-7]		
set-1	mem[40-47]	mem[8-15]	
set-2	mem[176-183]		
set-3	mem[184-191]	mem[88-95]	

3.
   - offset: 1-0
   - index: None
   - tag: 31-2
4.

Addr	Bin	Tag	H | M
3	00000011	0	M
180	10110100	45	M
43	00101011	10	M
2	00000010	0	H
191	10111111	47	M
88	01011000	22	M
190	10111110	47	H
14	00001110	3	M
181	10110101	45	H

block0	block1	block2	block3	block4	block5	block6	block7
m[0-3]	m[180-183]	m[40-43]	m[188-191]	m[88-91]	m[12-15]		

5.

Base CPI, No Memory Stalls	1.5
Processor Speed	2 GHz
Main Memory Access Time	100 ns
First Level Cache Miss-Rate pre Instruction	7%
Second Level Cache, Direct-Mapped Speed	12 cycles
Global Miss Rate with second level cache, direct-mapped	3.5%
second level cache, eight-way set associative speed	28 cycles
global miss rate with second level cache, eight-way set associative	1.5%

1) only a first level cache

clock cycle time: $0.5ns$

main memory access CPI = 200

Finally CPI = $1.5 + 7\% * 200 = 15.5$

2) a second level direct-mapped cache

0.93 × 1.5 + 0.035 × 13.5 + 0.035 × 213.5 = 9.34

3) a second level eight-way set associative cache

0.93 × 1.5 + 0.055 × 29.5 + 0.015 × 229.5 = 0.93*1.5+1.6225+3.4425=6.46

Problem3

1. 9-bit
2. 0x375 = 0011 0111 0101

	p1	p2		p3				p4					res
	0	0	1	1	0	1	1	1	0	1	0	1	
p1	x		x		x		x		x		x		0
p2		x	x			x	x			x	x		0
p3				x	x	x	x					x	0
p4								x	x	x	x	x	1

correct data is 0x365

Problem4

1.
   - offset: 11-0
   - VPN: 31-12
2.

VA	VPN	hit state
4669	1	page fault
2227	0	hit in PT
13916	3	hit in TLB
34587	8	page fault
12608	3	hit in TLB
TLB:		
Vaild	Tag(recent)	PPN
1	0	5
1	8	14
1	3	6
1	1	13
Page table		
Valid	PPN or Disk	
1	5	
1	13	
0	disk	
1	6	
1	9	
1	11	
0	disk	
1	4	
1	14	
0	disk	
1	3	
1	12	
