Fabrication of CMOS Integrated Circuits

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References

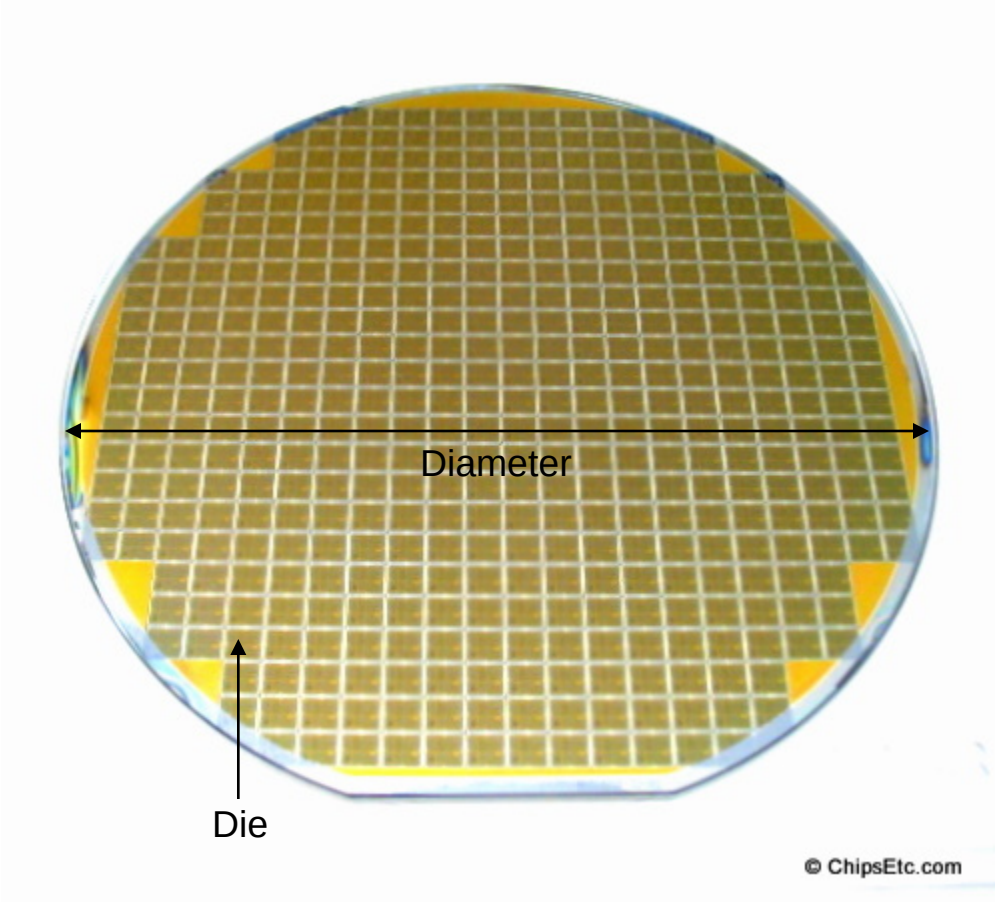
- John P. Uyemura, “Introduction to VLSI Circuits and Systems,” 2002.
  - Chapter 4

Goal

- Understand the fabrication (manufacturing) process for CMOS integrated circuits (ICs)

Silicon Wafer and Yield

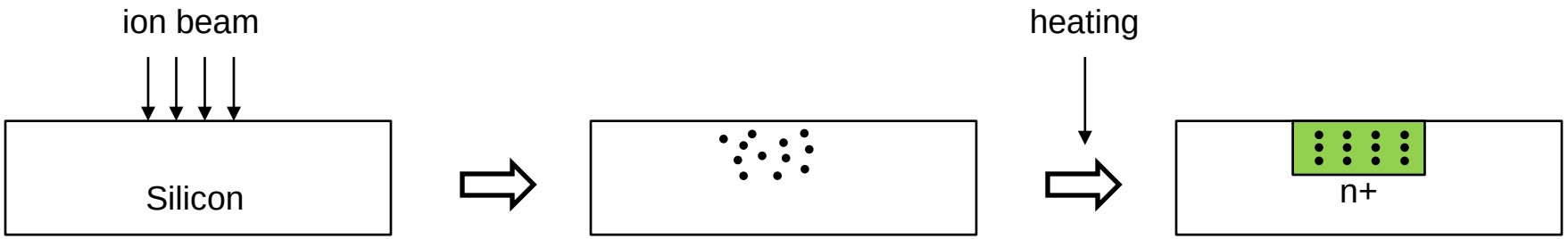
- Yield
  - $Y = \frac{N_G}{N_T} \times 100\%$
    - N_G: # good dies
    - N_T: # total dies
      - $N_T = \pi \frac{(d-d_e)^2}{4A_{die}}$
  - $Y = e^{-\sqrt{DA}}$
    - A: die area
    - D: defect density
  - $Y = \left(1 - \frac{A_{die}D}{c}\right)^c$
  - $Y = \frac{1}{\left(1+\frac{A_{die}D}{c}\right)^2}$
    - c: a constant for clustered defects



Source: http://www.chipsetc.com/uploads/1/2/4/4/1244189/1780324_orig.jpg

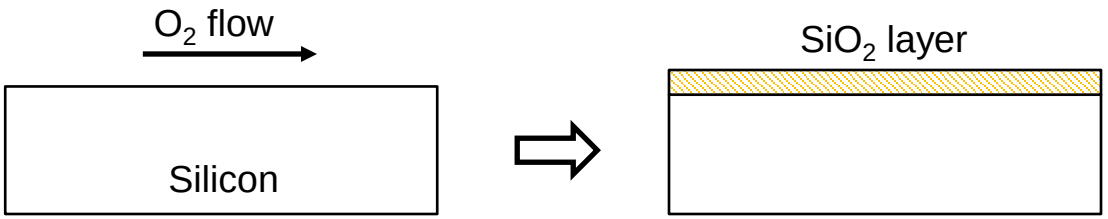
Material Growth and Deposition

- Doped silicon layers
  - Ion implantation
  - Annealing

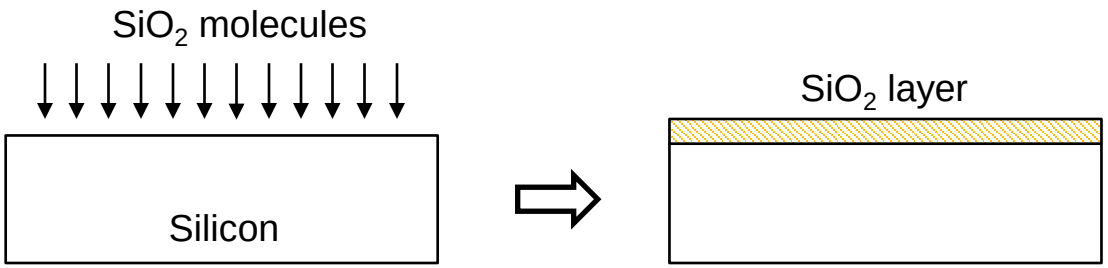


Material Growth and Deposition

- Silicon Dioxide (insulator)
  - Thermal oxide

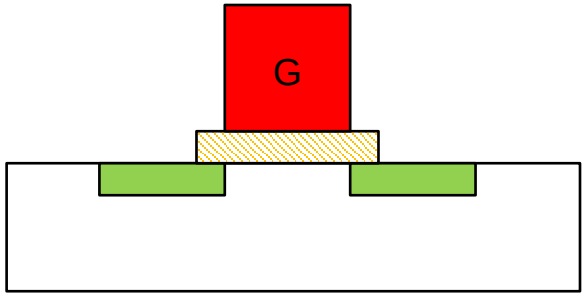


  - Chemical vapor deposition (CVD) oxide

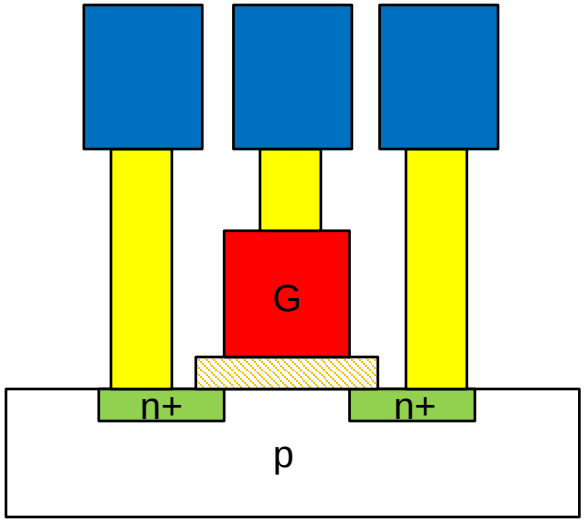


Material Growth and Deposition

- Polycrystal Silicon
  - Used to fabricate Gate
  - Deposition



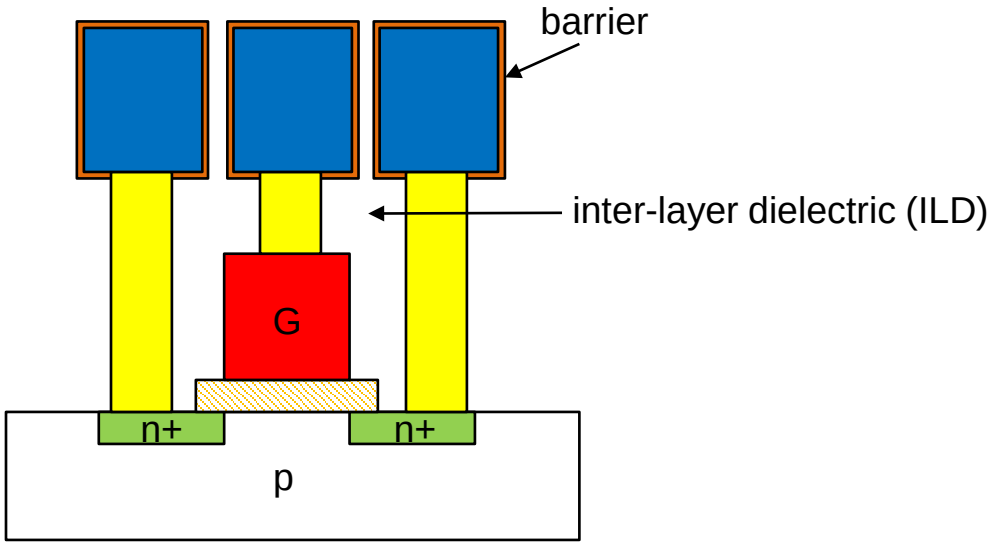
- Metal
  - Deposition



Material Growth and Deposition

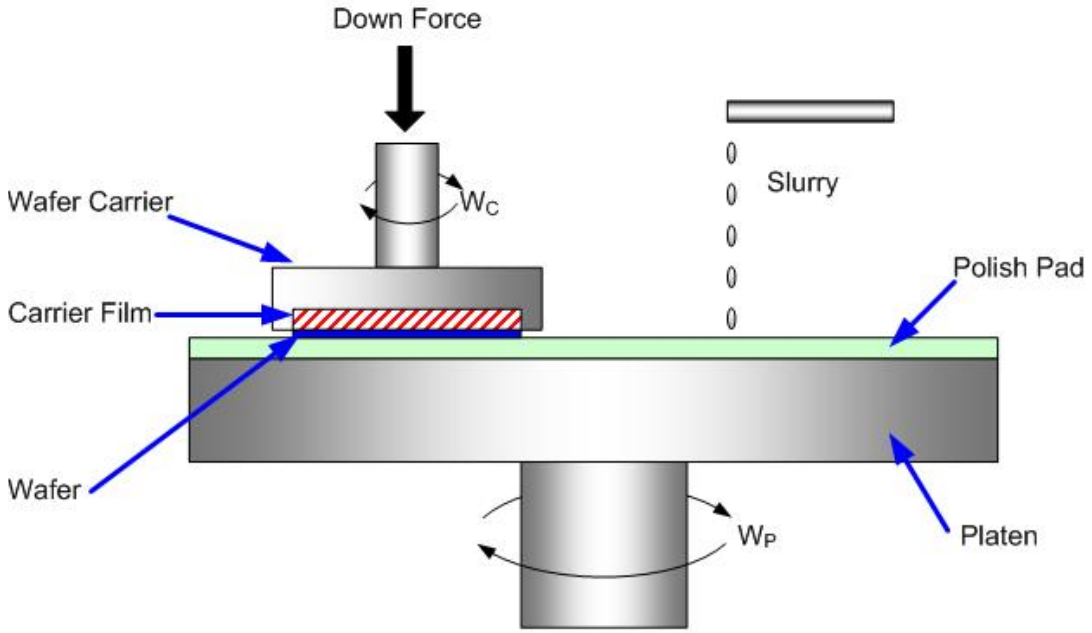
- Silicon Nitride
  - Barrier on the topmost layer

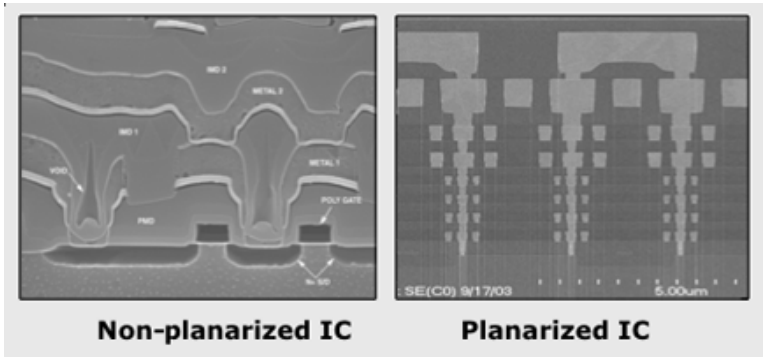
- Barrier is also used for preventing copper from diffusing into adjacent layers.



Material Growth and Deposition

- Chemical-Mechanical Polishing (CMP)
  - also called Chemical-Mechanical Planarization
  - After depositing each layer, CMP is applied to planarize the surface.

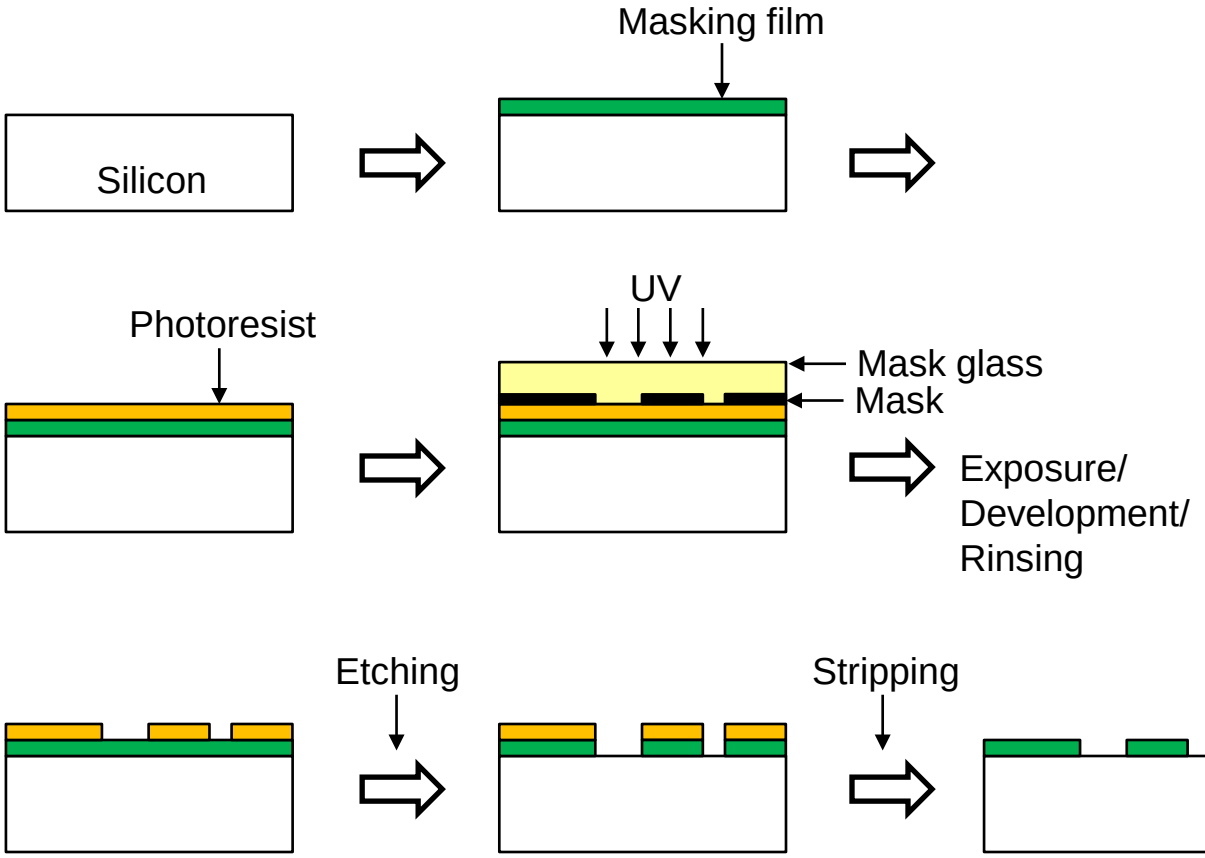


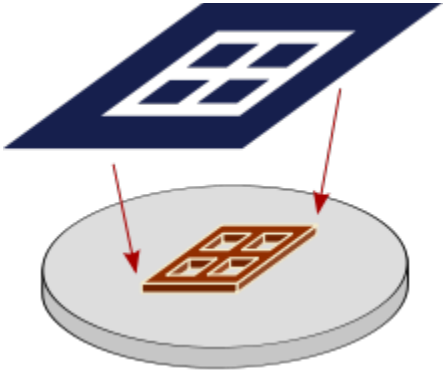


Source: http://www.ntu.edu.sg/home/mdlbutler/Research/cmp%20polisher.jpg
Source: http://linx-consulting.com/images/planarized_IC.gif

Lithography (Photolithography)

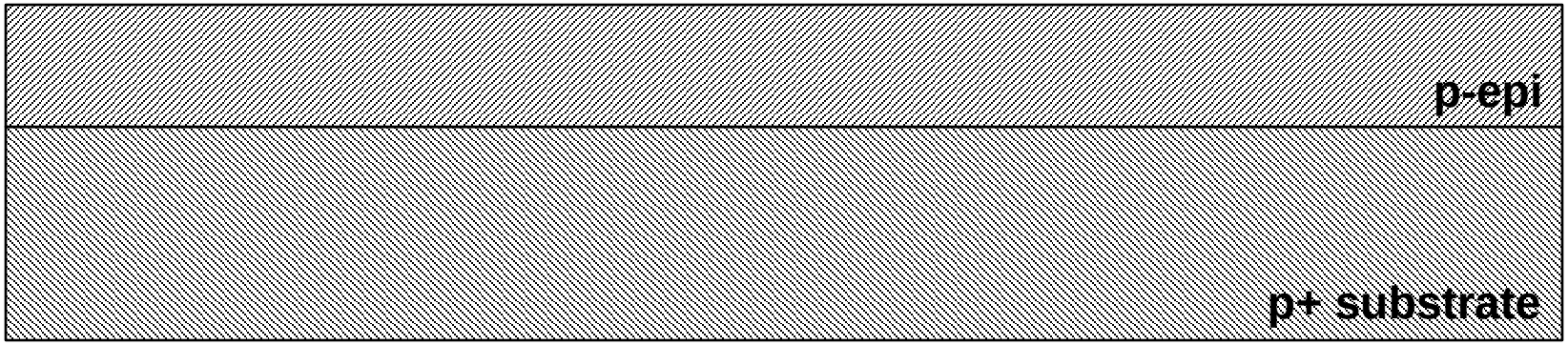
- Reticle (mask)



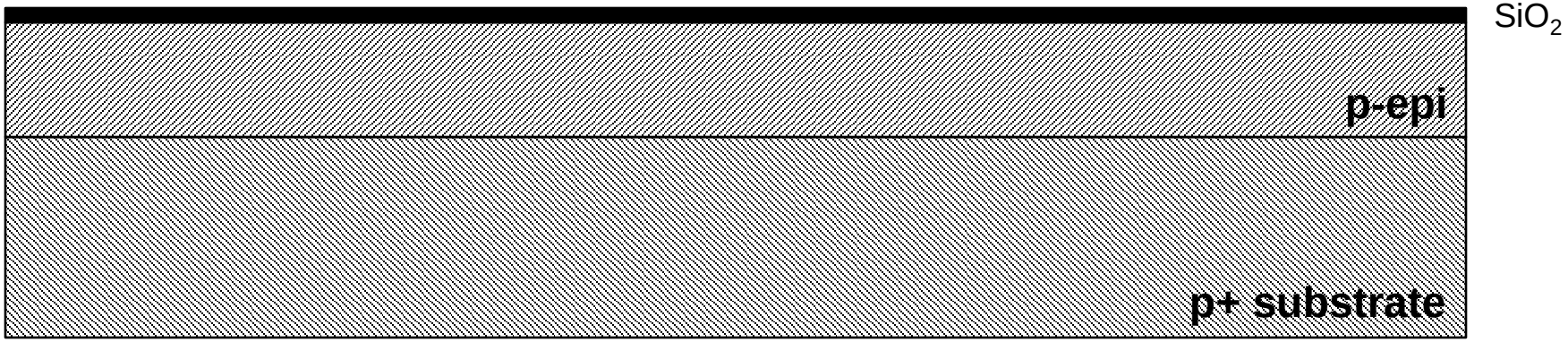


Source: https://upload.wikimedia.org/wikipedia/commons/thumb/5/5e/Mask_illustration.svg/220px-Mask_illustration.svg.png

CMOS Fabrication Process

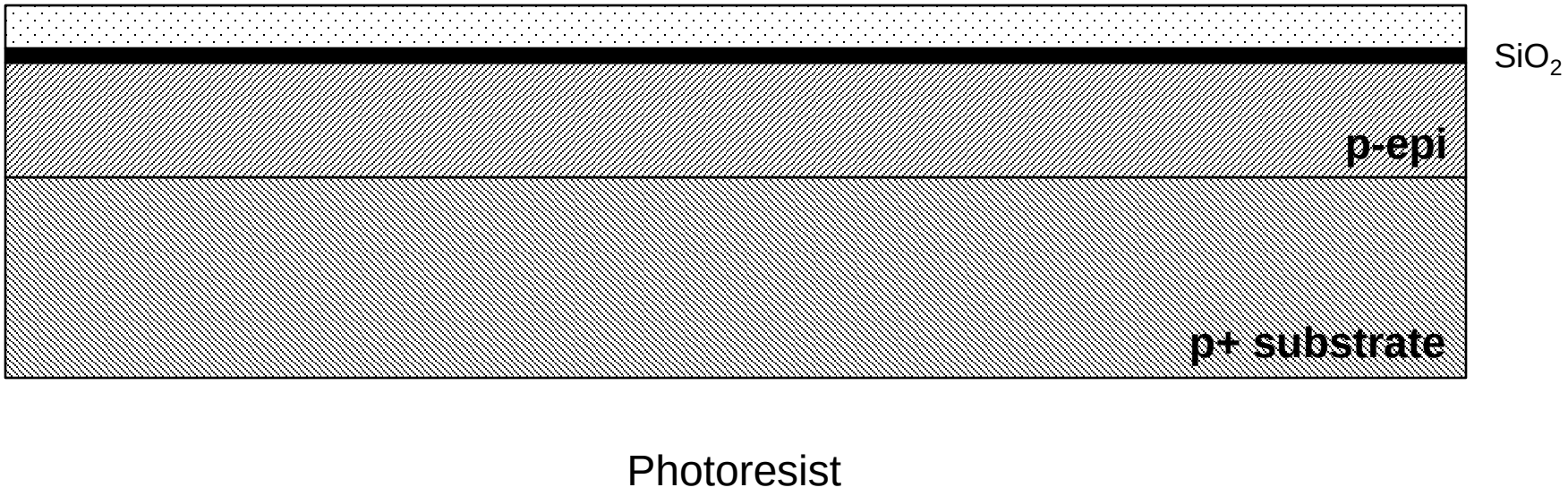


CMOS Fabrication Process

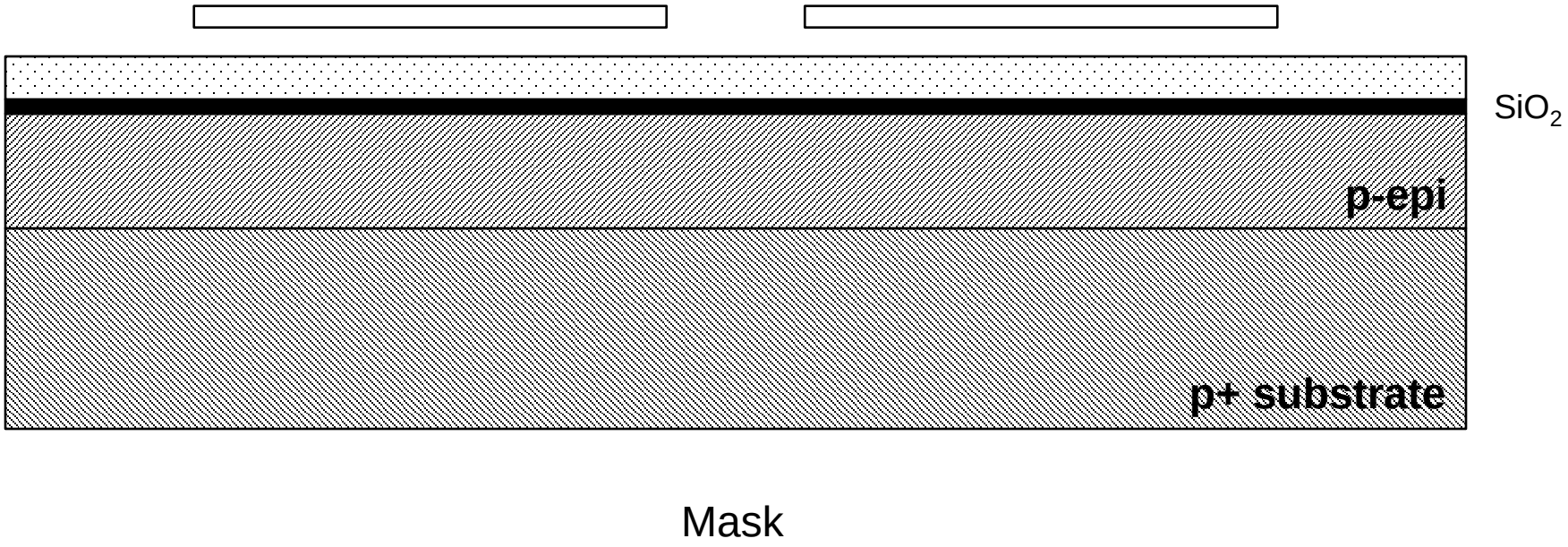


Gate-oxide deposition

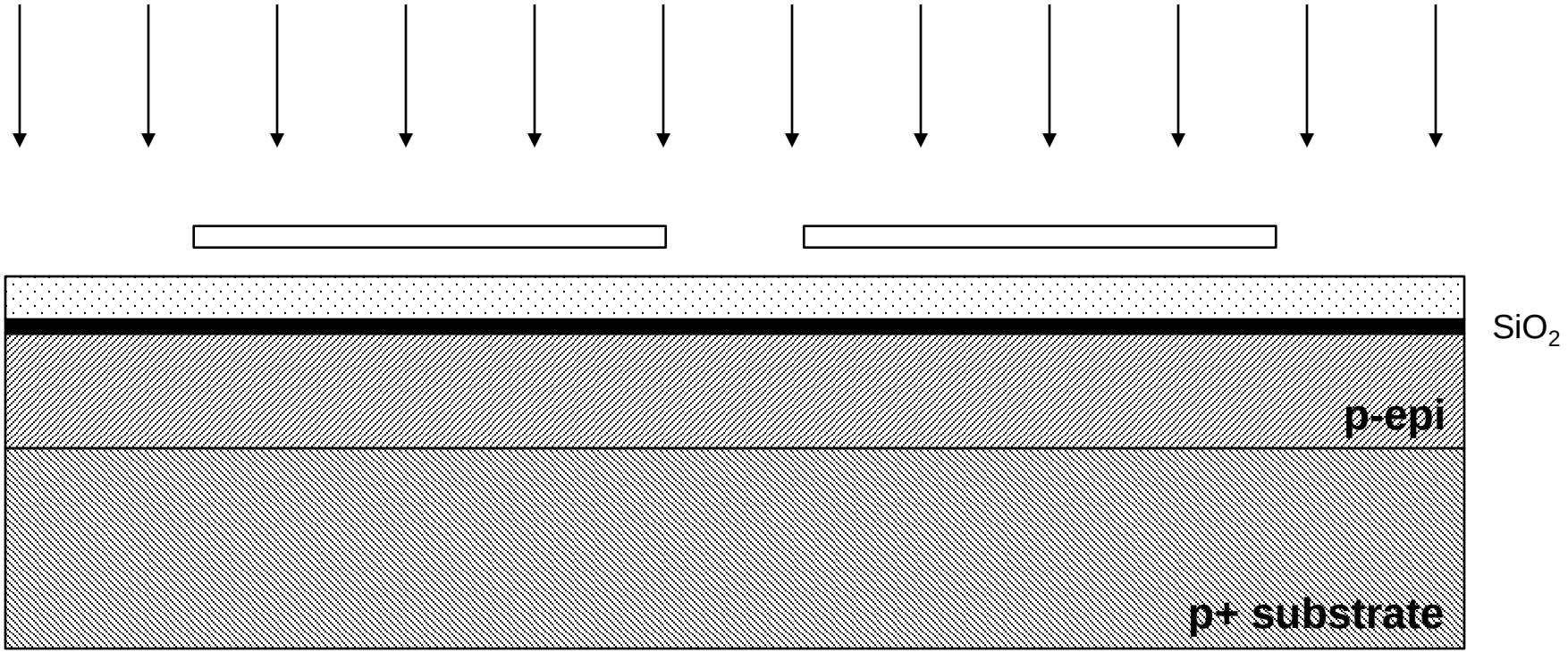
CMOS Fabrication Process



CMOS Fabrication Process

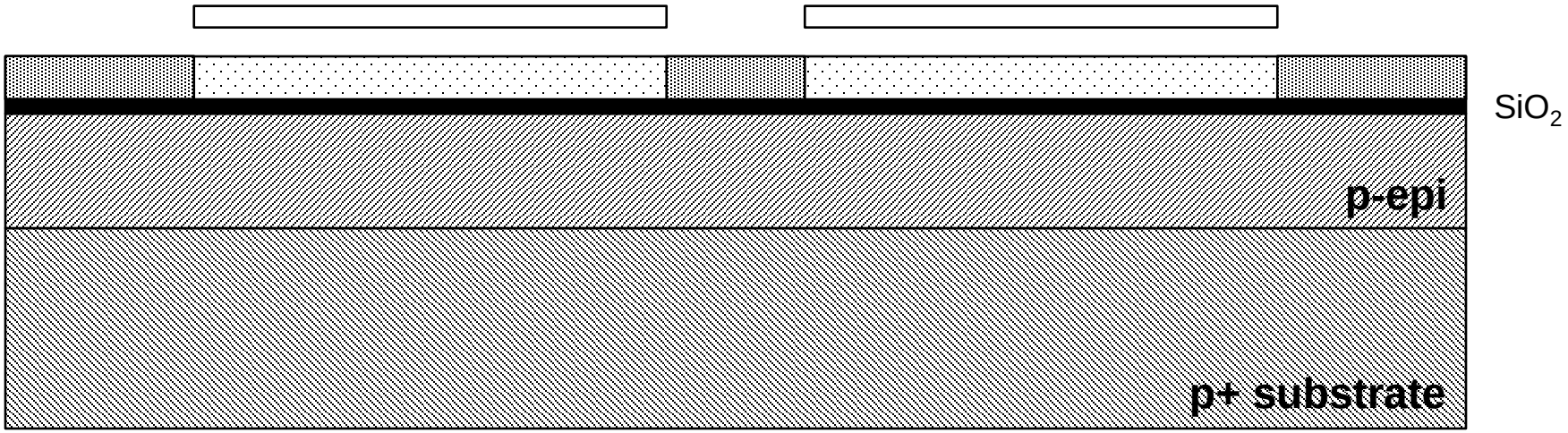


CMOS Fabrication Process



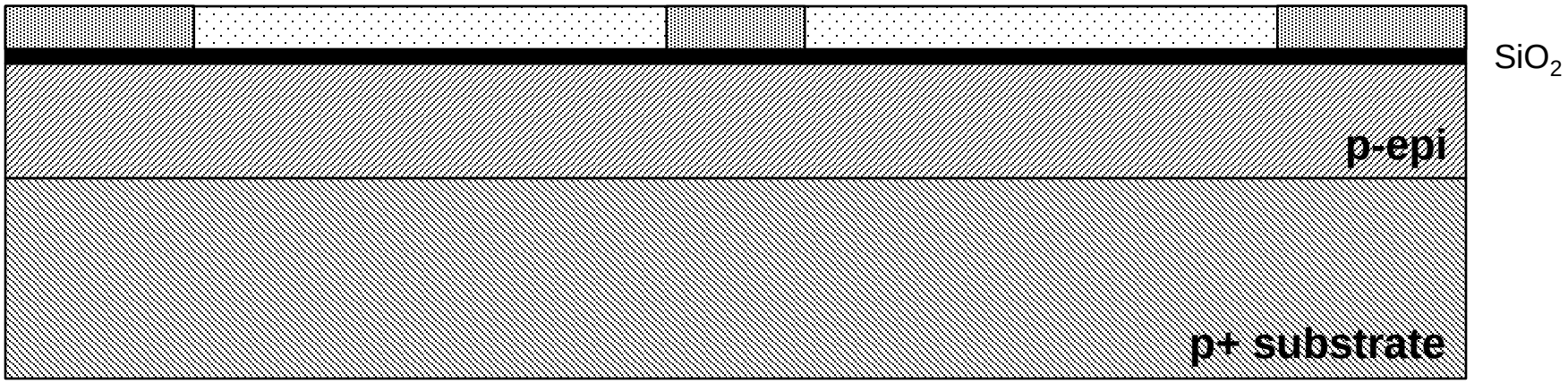
Expose (photolithography)

CMOS Fabrication Process



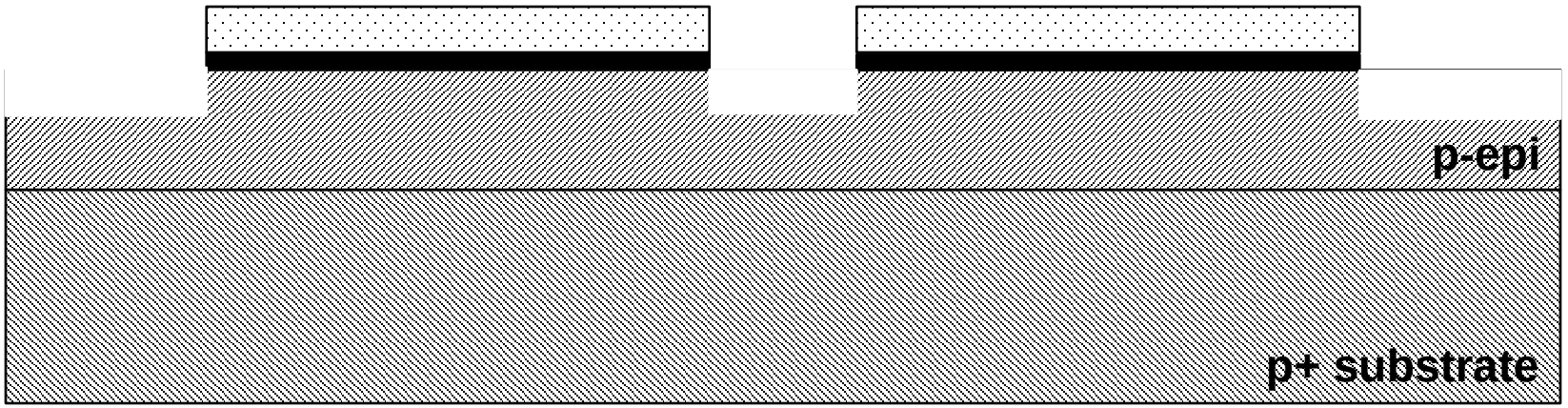
After photolithography

CMOS Fabrication Process



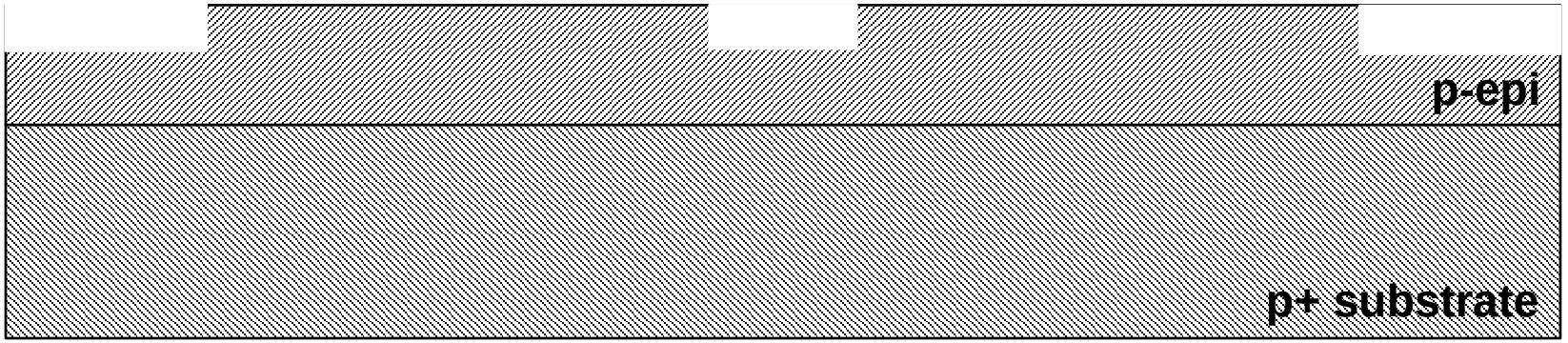
Remove mask

CMOS Fabrication Process



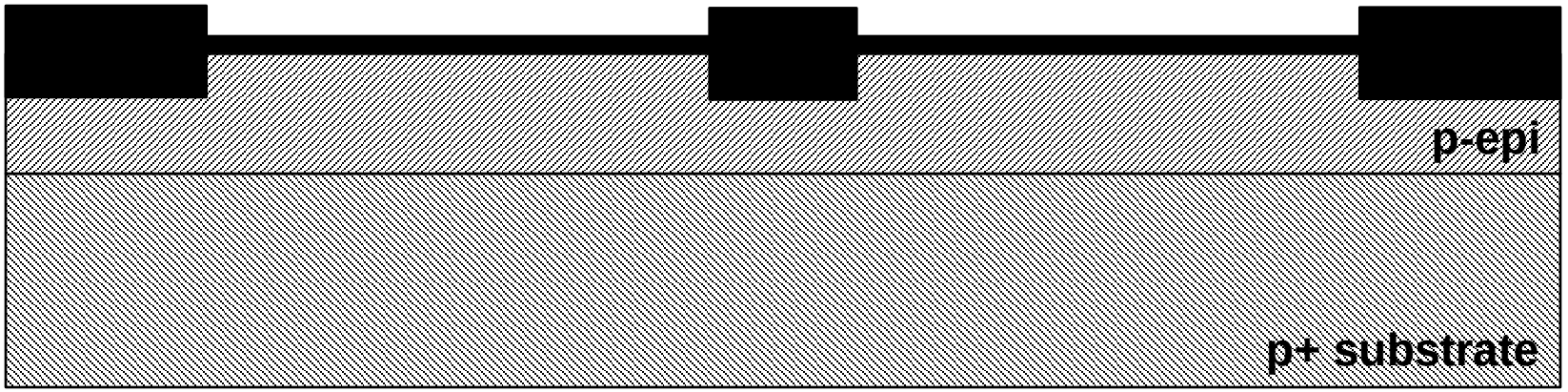
Etching

CMOS Fabrication Process



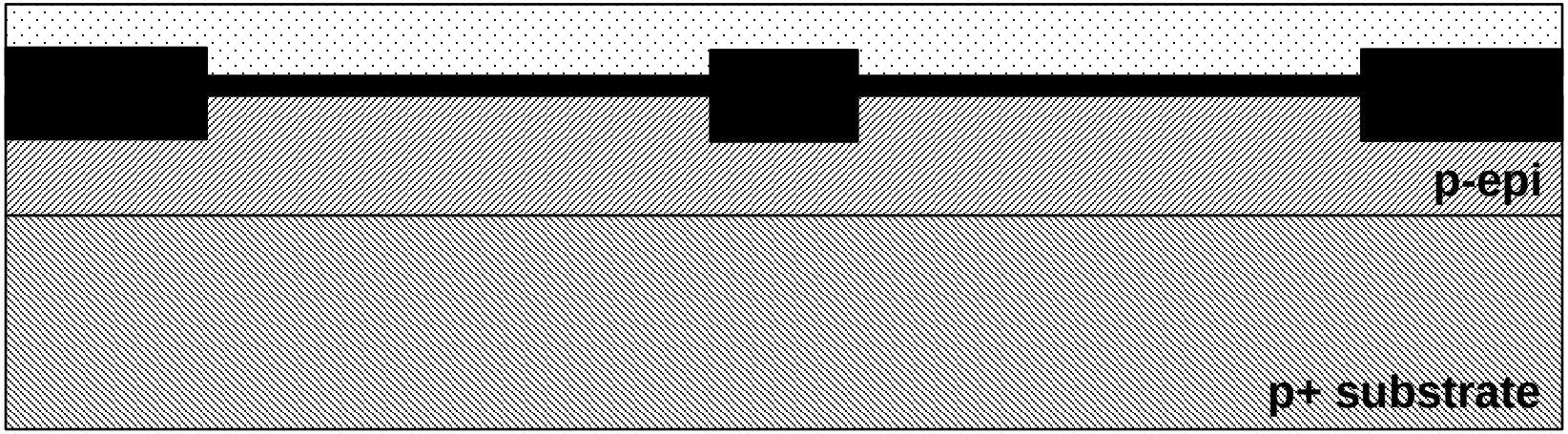
Etching

CMOS Fabrication Process



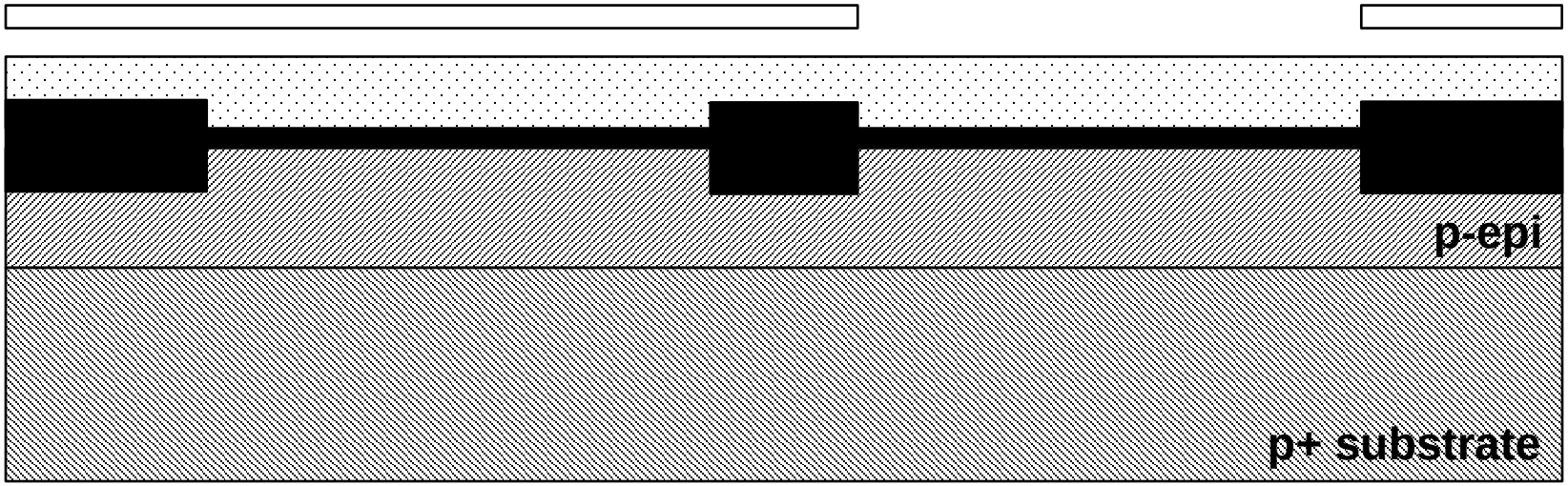
Oxide deposition

CMOS Fabrication Process



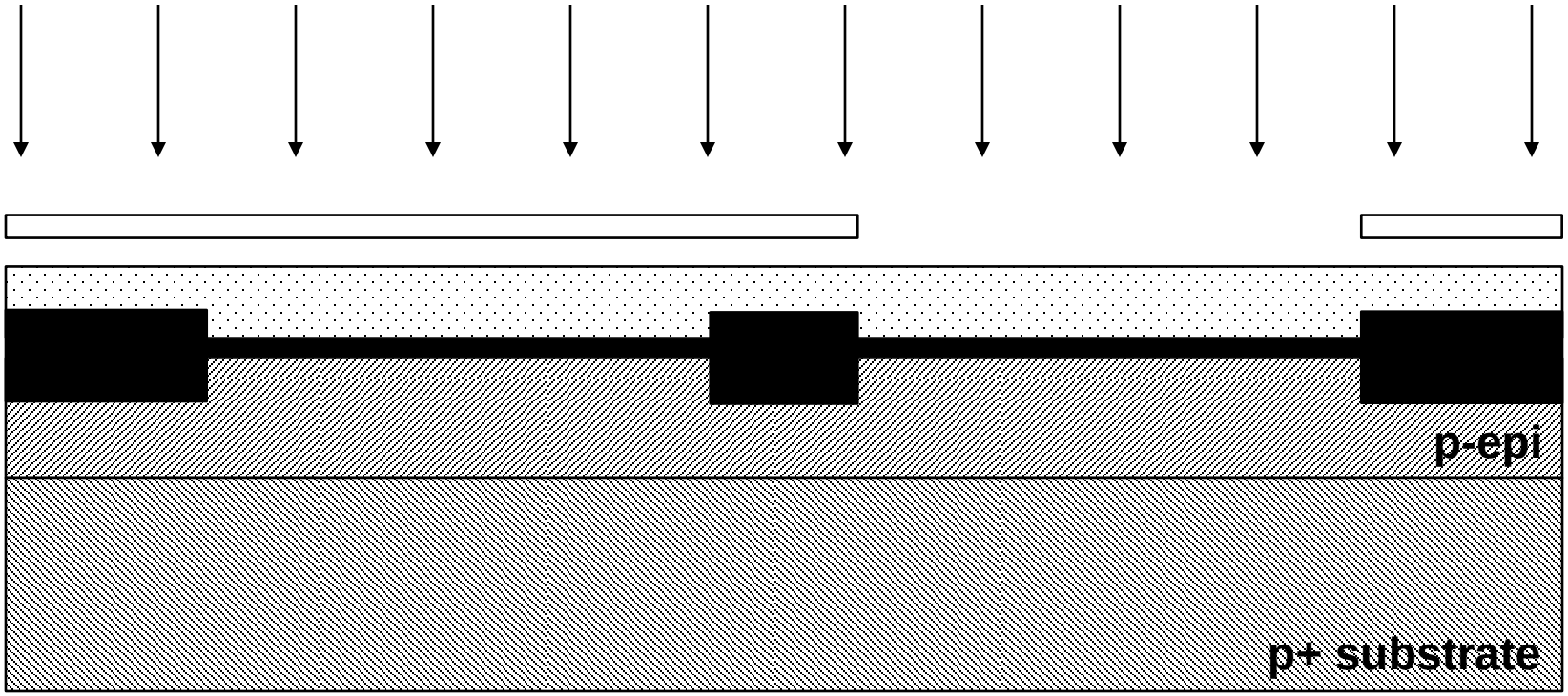
Photoresist

CMOS Fabrication Process



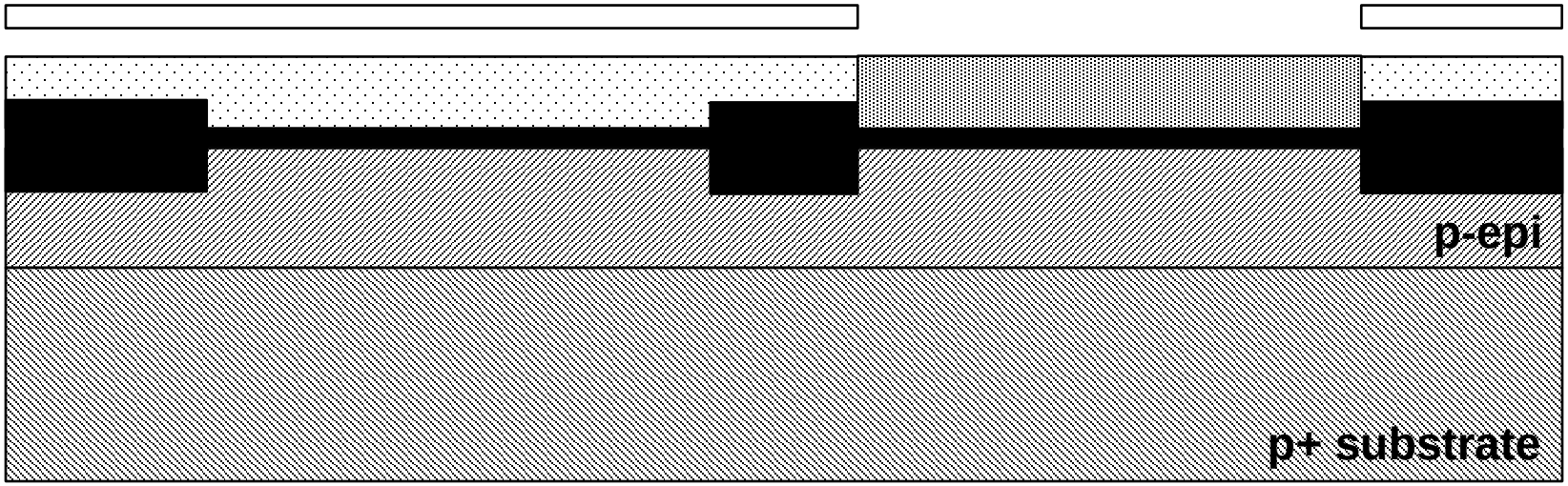
Mask

CMOS Fabrication Process



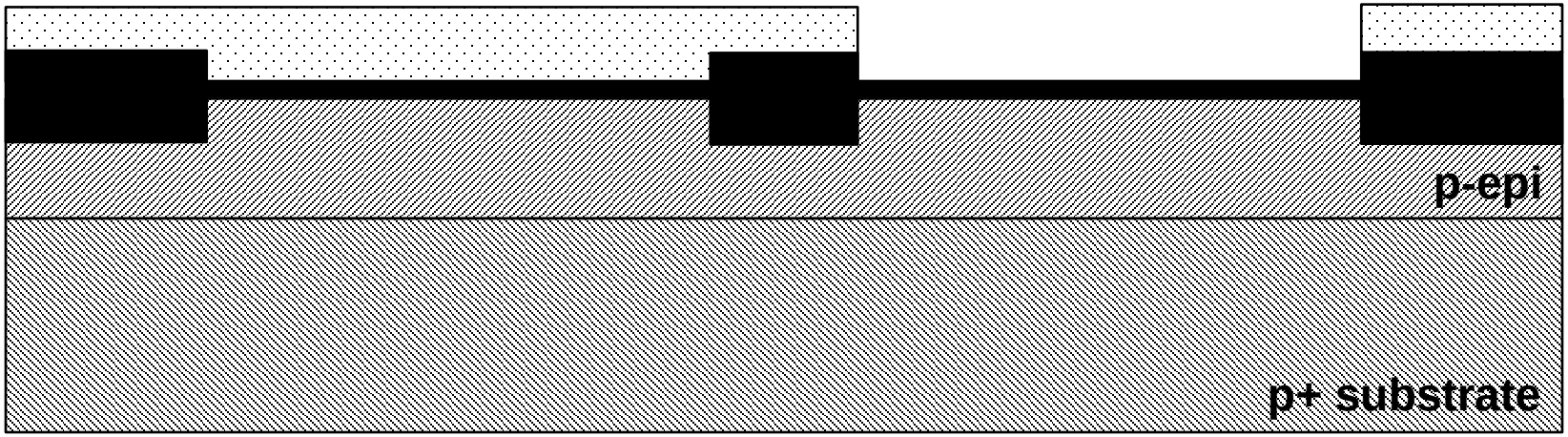
Photolithography

CMOS Fabrication Process



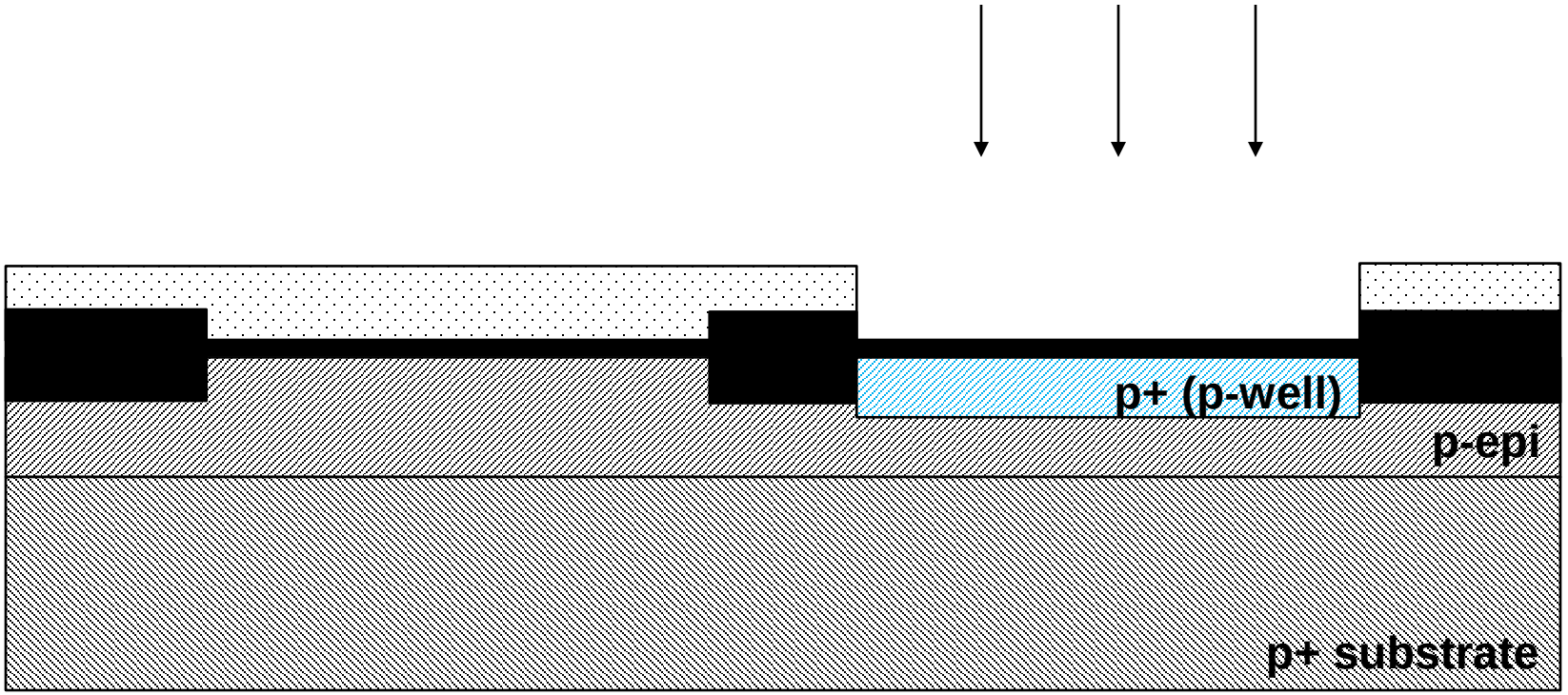
After photolithography

CMOS Fabrication Process



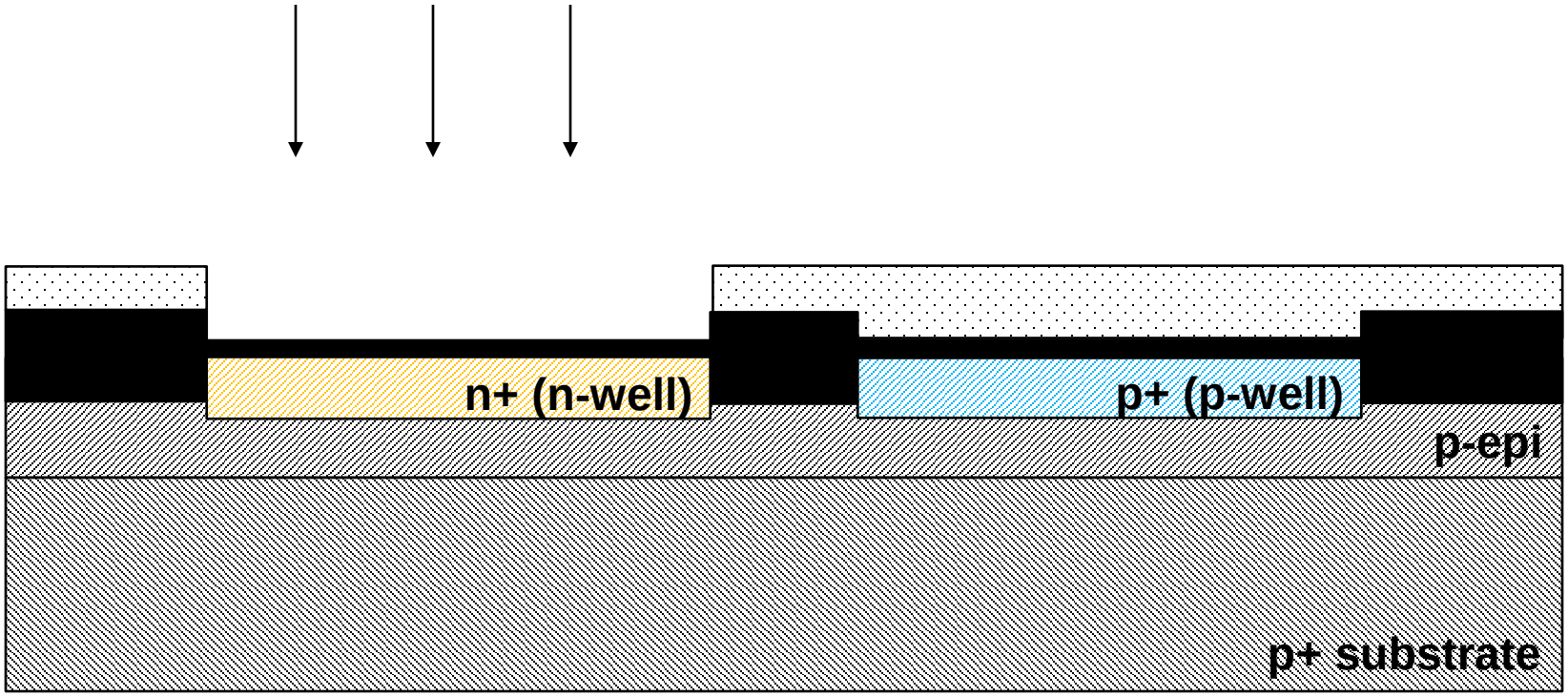
Etching

CMOS Fabrication Process



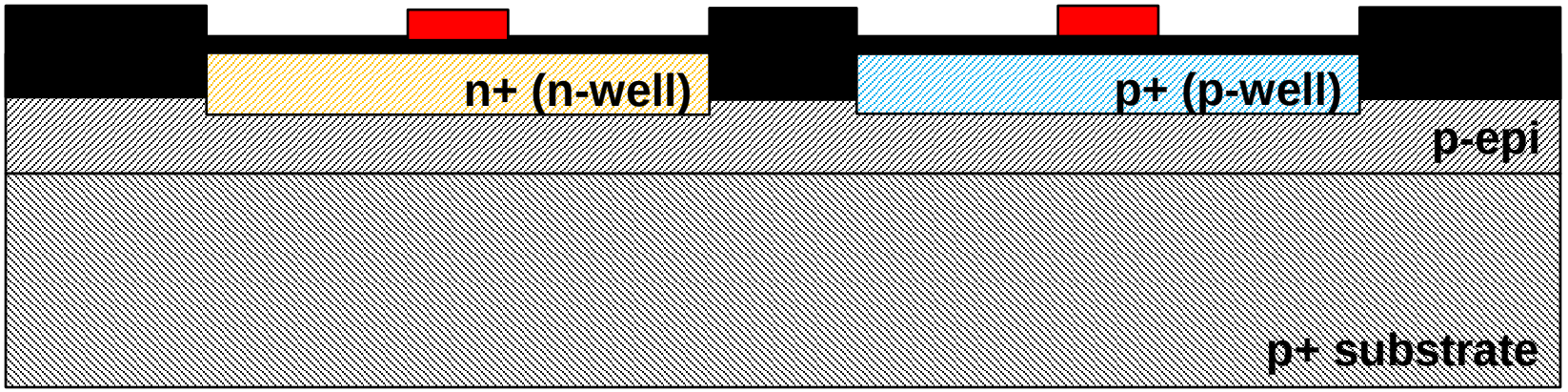
Doping

CMOS Fabrication Process



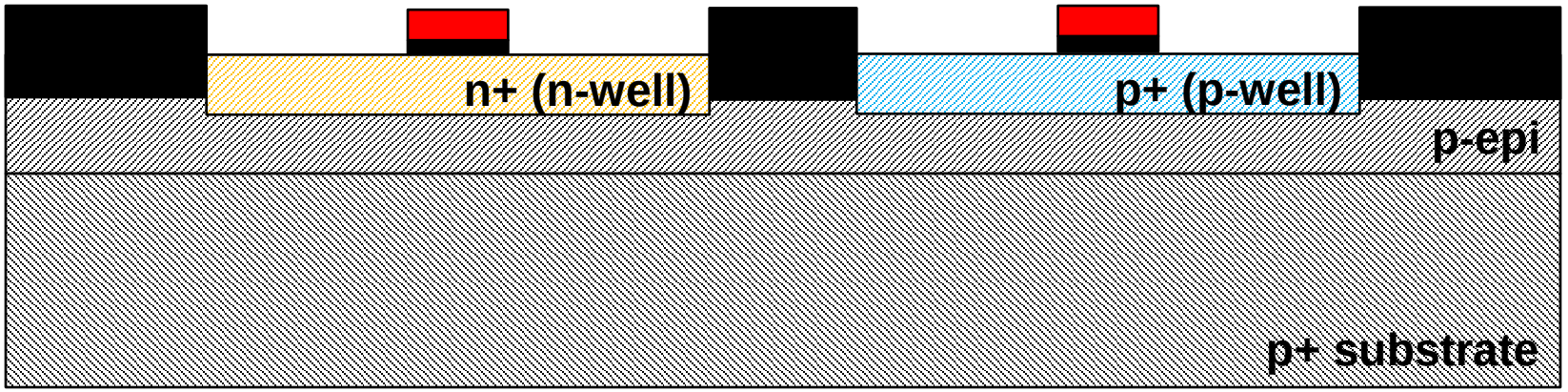
Doping

CMOS Fabrication Process



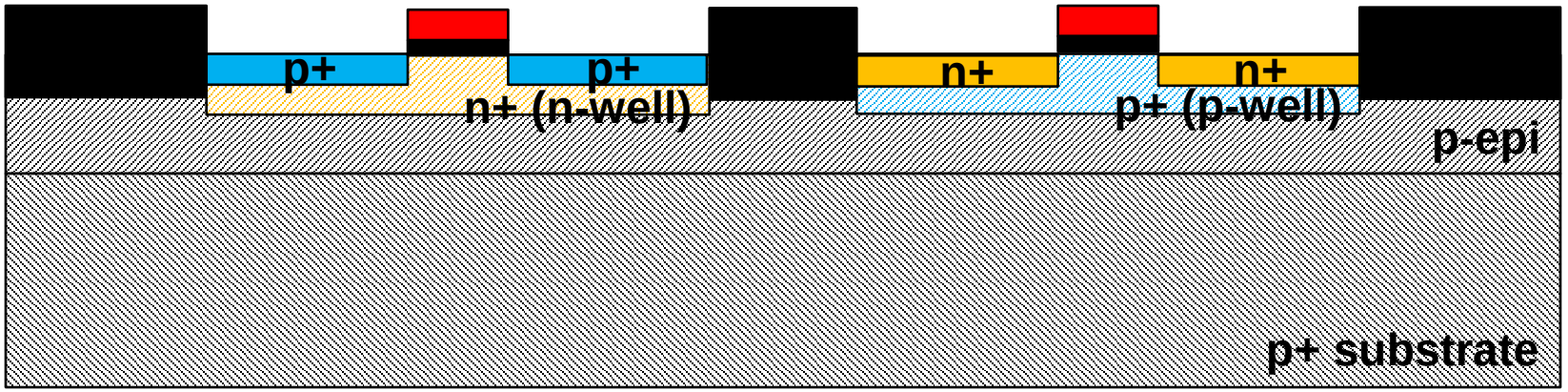
Poly

CMOS Fabrication Process



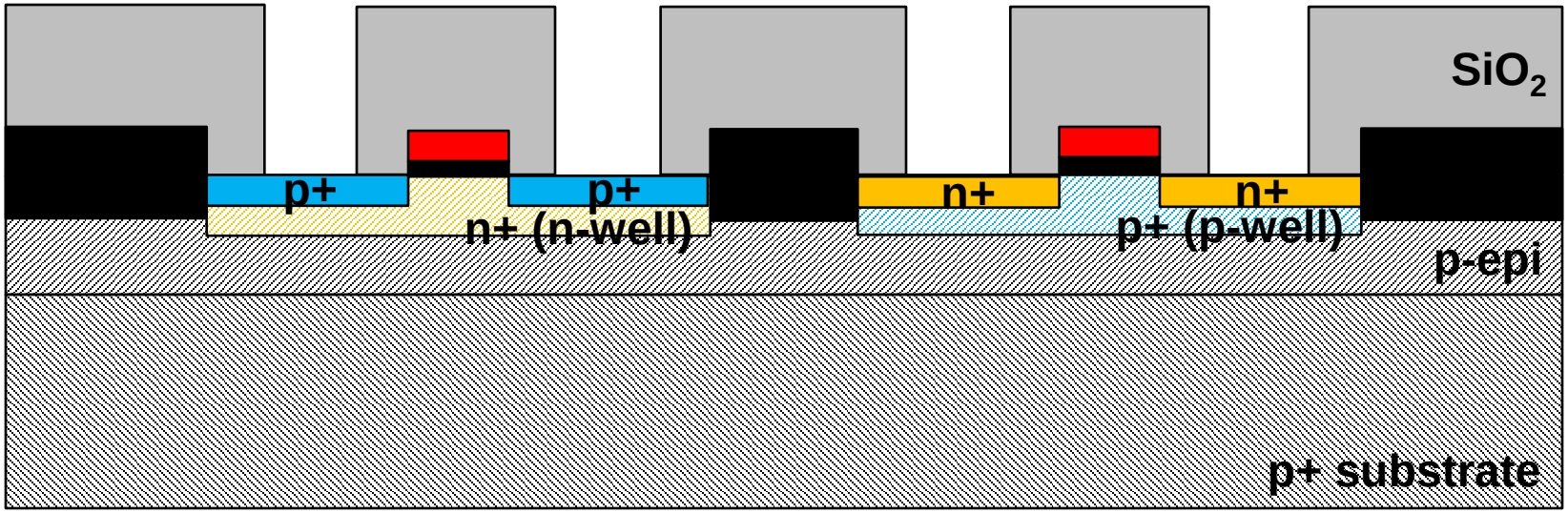
Etching

CMOS Fabrication Process



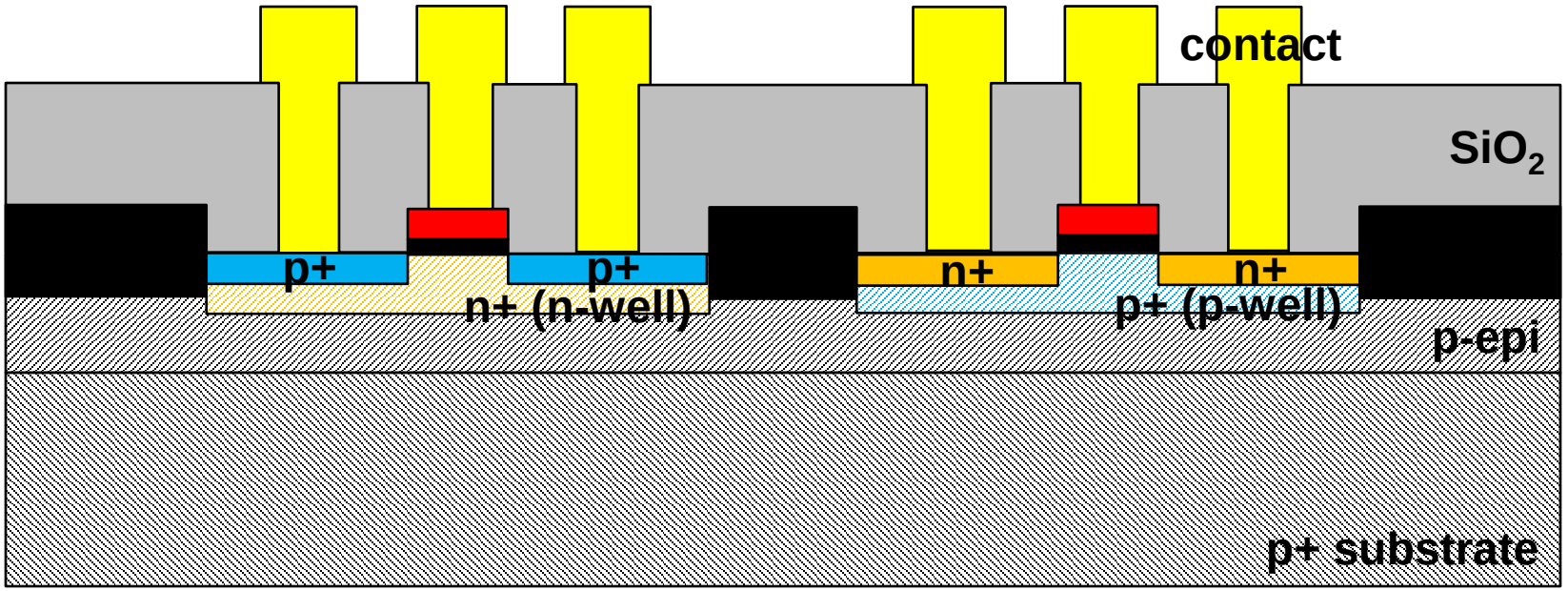
Doping

CMOS Fabrication Process



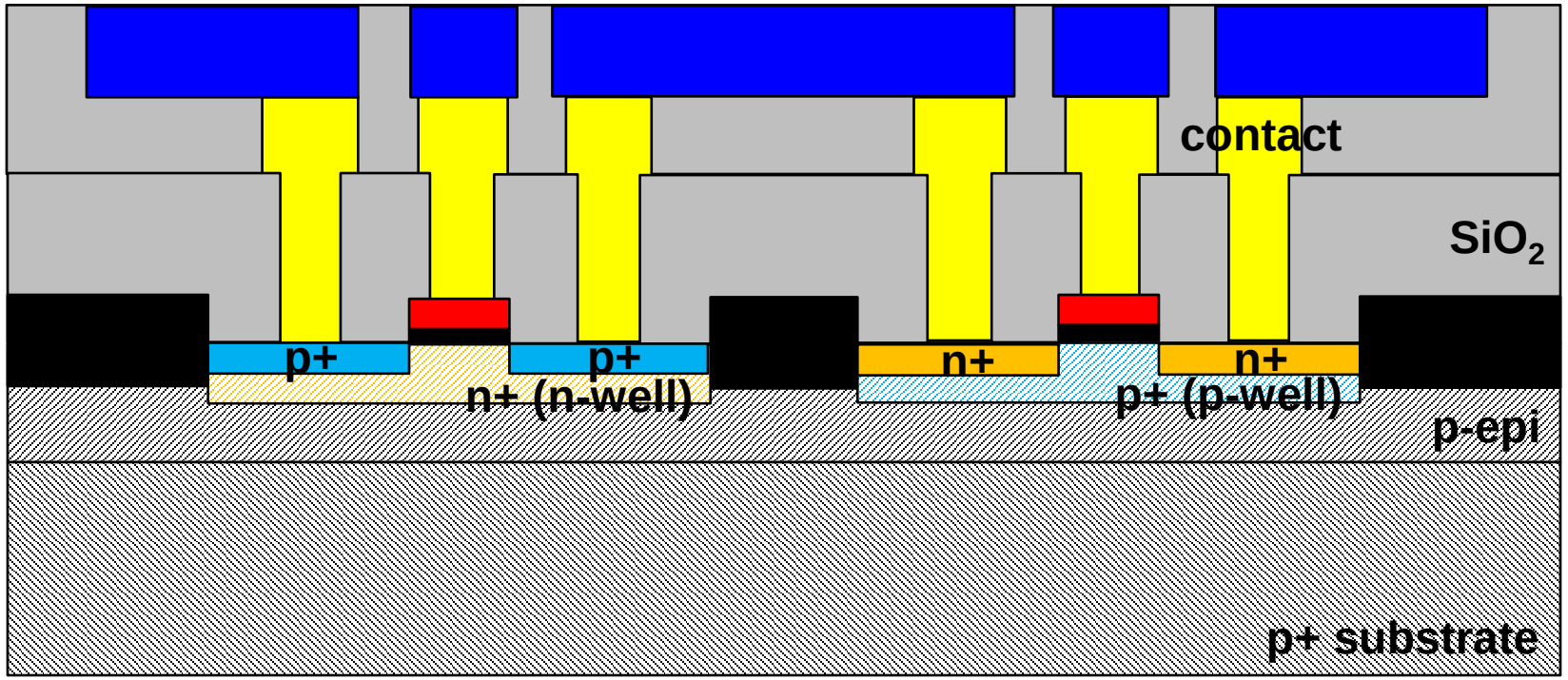
Oxide deposition

CMOS Fabrication Process



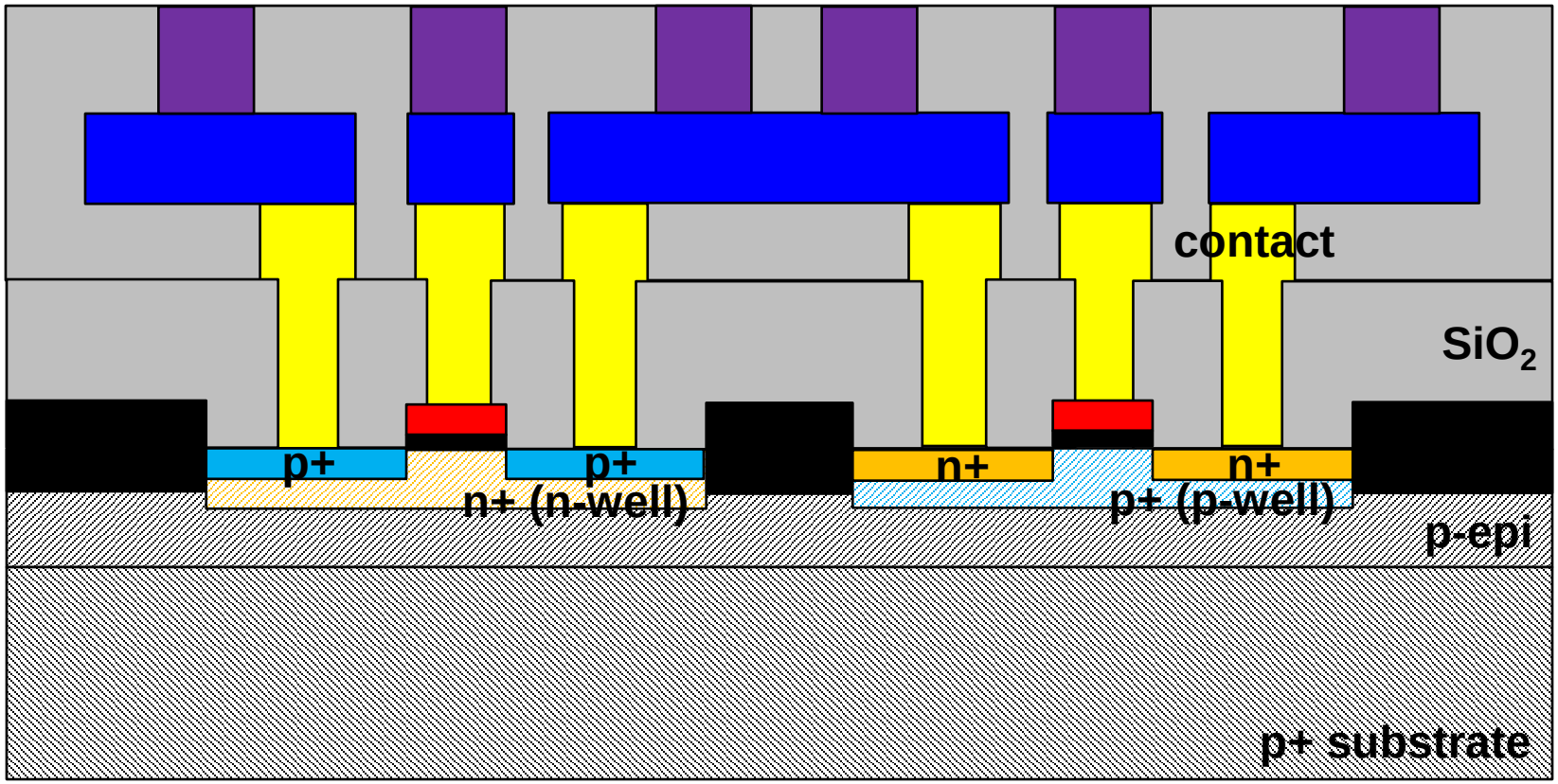
Contact

CMOS Fabrication Process



Metal 1

CMOS Fabrication Process



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