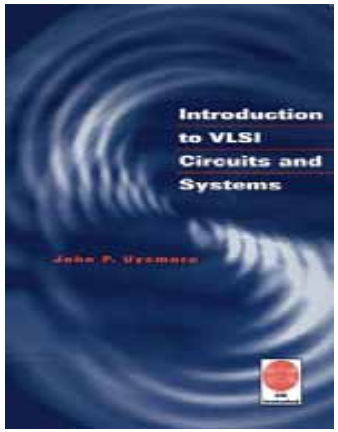
國立勤益科技大學
National Chin-Yi University of Technology

Introduction to VLSI Circuits and Systems
積體電路概論

Chapter 09

Advanced Techniques in CMOS Logic Circuits



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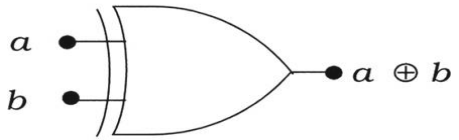
Fall 2007

Outline

- Mirror Circuits
- Pseudo-nMOS
- Tri-State Circuits
- Clocked CMOS
- Dynamic CMOS Logic Circuits
- Dual-Rail Logic Networks

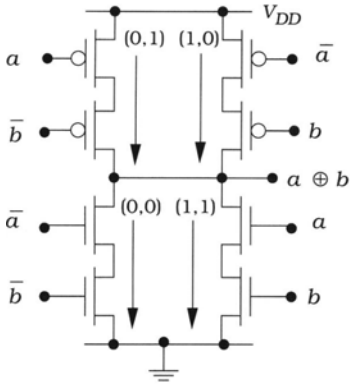
Mirror Circuits

- Mirror circuits are based on series-parallel logic gates, but are usually faster and have a more uniform layout
  - » Output 0's imply that an nFET chain is conducting to ground
  - » Output 1's means that a pFET group provides support from the power supply

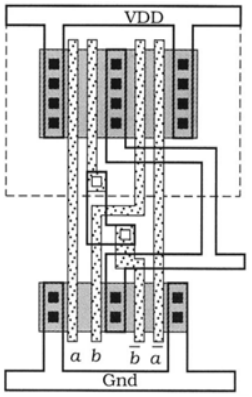


a	b	a ⊕ b	On devices
0	0	0	nFET
0	1	1	pFET
1	0	1	pFET
1	1	0	nFET

Figure 9.1 XOR function table



(a) Circuit



(b) Layout

Figure 9.2 XOR mirror circuit

XOR & XNOR

- The advantages of the mirror circuit are more *symmetric layouts* and *shorter rise and fall times*
- In Figure 9.3, transient calculations of XOR

$$\tau_x = C_{out}(2R_x) + C_x R_x \qquad (9.1)$$

where x is p or n

$$t_r \approx 2.2\tau_p \qquad (9.2)$$

$$t_f \approx 2.2\tau_n \qquad (9.3)$$

- In Figure 9.4, a example of XNOR

$$\overline{a \oplus b} = \overline{\bar{a} \cdot b + a \cdot \bar{b}} \qquad (9.4)$$

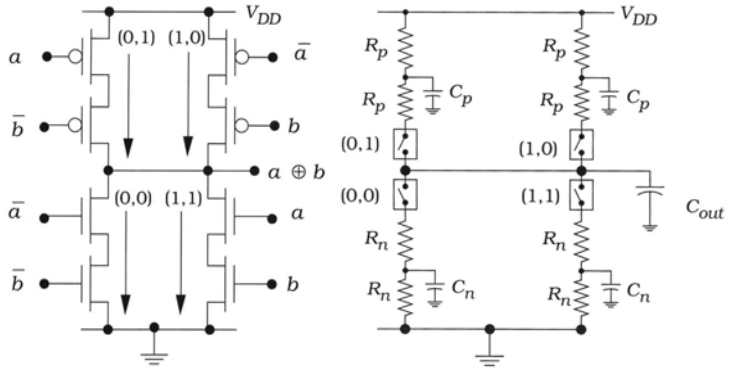
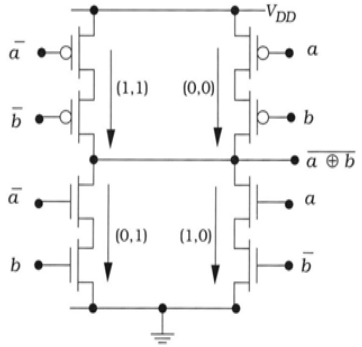


Figure 9.3 Switching mode for transient calculations (XOR)



a	b	$\overline{a \oplus b}$
0	0	1
0	1	0
1	0	0
1	1	1

Figure 9.4 Exclusive-NOR (XNOR) circuit

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Pseudo-nMOS

- Adding a single pFET to otherwise nFET-only circuit produces a logic family that is called pseudo-nMOS
  - » Less transistor than CMOS
  - » For N inputs, only requires (N+1) FETs
  - » Pull-up device: pFET is biased active since the grounded gate gives $V_{SGp} = V_{DD}$
  - » Pull-down device: nFET logic array acts as a large switch between the output f and ground
  - » However, since the pFET is always biased on, V_{OL} can never achieve the ideal value of 0 V
- A simple inverter using pseudo-nMOS as Figure 9.6

$$\frac{\beta_n}{2}\left[2(V_{DD}-V_{Tn})V_{OL}-V_{OL}^{\,2}\right]=\frac{\beta_p}{2}\left(V_{DD}-|V_{Tp}|\right)^2 \qquad (9.4)$$

$$V_{OL}=(V_{DD}-V_{Tn})-\sqrt{(V_{DD}-V_{Tn})^2-\frac{\beta_p}{\beta_n}\left(V_{DD}-|V_{Tp}|\right)^2} \qquad (9.5)$$

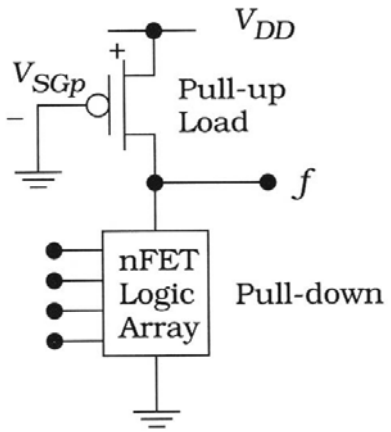


Figure 9.5 General structure of a pseudo-nMOS logic gate

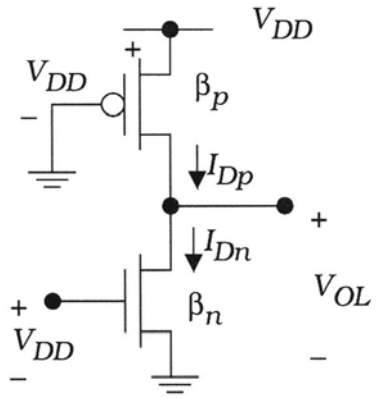
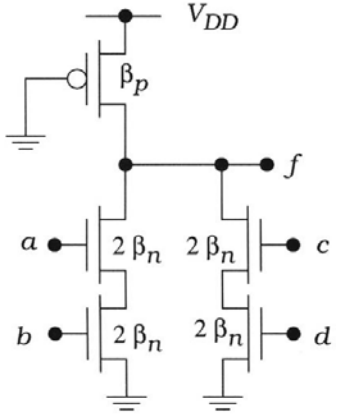


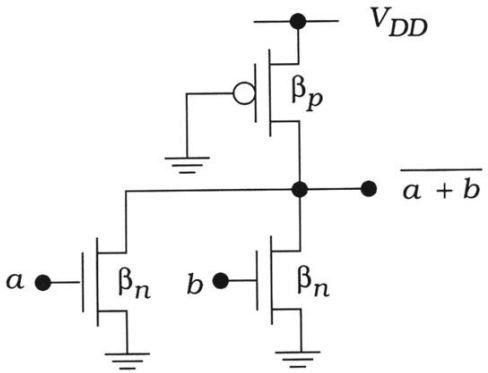
Figure 9.6 Pseudo-nMOS inverter

nFET Array in Pseudo-nMOS

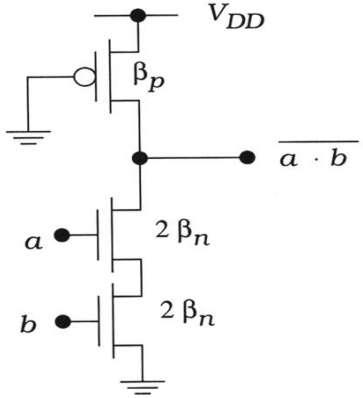
- The design of nFET array of pseudo-nMOS is the same as in standard CMOS
  - » Series and parallel logic FETs
  - » Smaller simpler layouts, and interconnect is much simpler
  - » However, the sizes need to be adjusted to insure proper electrical coupling to the next stage
  - » Resize in physical design



(a) General circuit

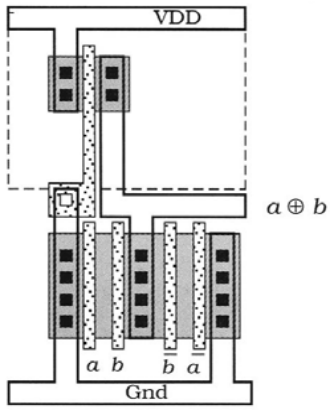


(a) NOR2



(b) NAND2

Figure 9.7 Pseudo-nMOS NOR and NAND gates



(b) Layout

Figure 9.8 AOI gate

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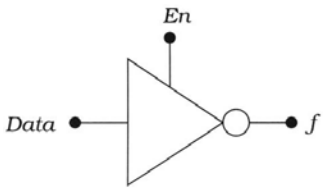
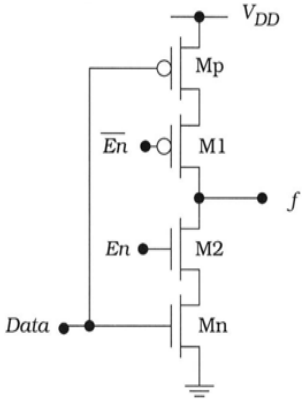
Tri-State Circuits

- A tri-state circuit produces the usual 0 and 1 voltages, but also has a third high impedance Z (or Hi-Z)
  - » Useful for isolating circuits from common bus lines
  - » In Hi-Z case, the output capacitance can hold a voltage even though n hardwire connection exists
- A non-inverting circuit (a buffer) can be obtained by adding a regular static inverter to the input



En	f
0	Z
1	$\overline{Data}$

(a) Symbol and operation



(b) CMOS circuit

Figure 9.9 Tri-state inverter

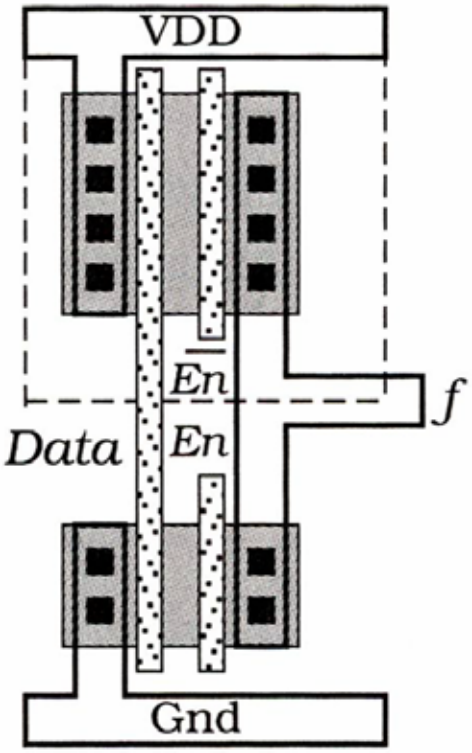


Figure 9.10 Tri-state layout

Outline

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Clock-CMOS (C^2MOS)

- *Static CMOS*: the output of a static logic gate is valid so long as the input value are valid and the circuit has stabilized
- However, logic delays are due to the "rippling" through the circuits
  - » Not reference to any specific time base
  - » So on, Clock CMOS, or C^2MOS is proposed
- C^2MOS concept: non-overlapping clock

$$\phi(t)\cdot\bar{\phi}(t)=0 \qquad (9.9)$$

$$\Rightarrow \bar{\phi}(t)=V_{DD}-\phi(t) \qquad (9.10)$$

  - » But in physical signal, the clocks may overlap slightly during a transition

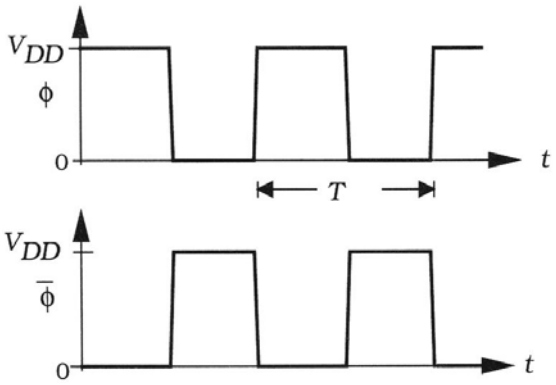


Figure 9.11 Clock signals

C²MOS Networks

- C2MOS is composed of a static logic circuit with tri-state output network (made up of FETs M1 and M2) that is controlled by ϕ and $\bar{\phi}$
  - When $\phi = 0$, both M1 and M2 are active, and become to a standard static logic gate
  - When $\phi = 1$, both M1 and M2 are cutoff, so the output is a Hi-Z state

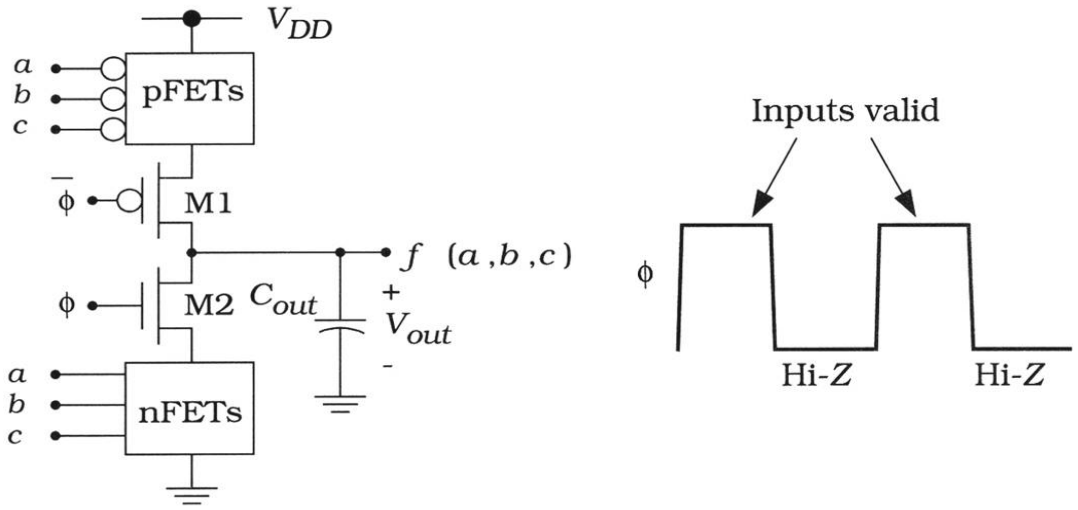
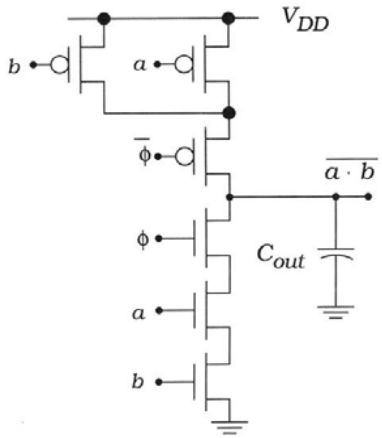
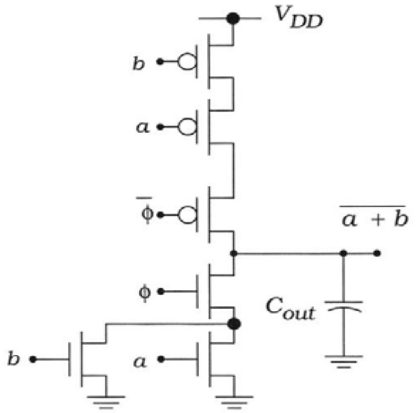


Figure 9.12 Structure of a C²MOS gate

Example of C²MOS

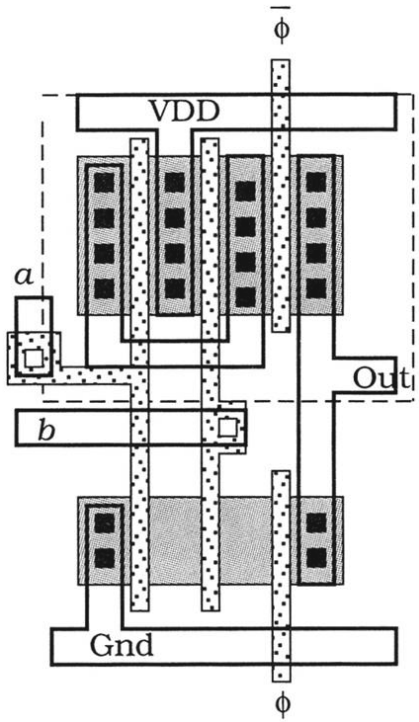


(a) NAND2

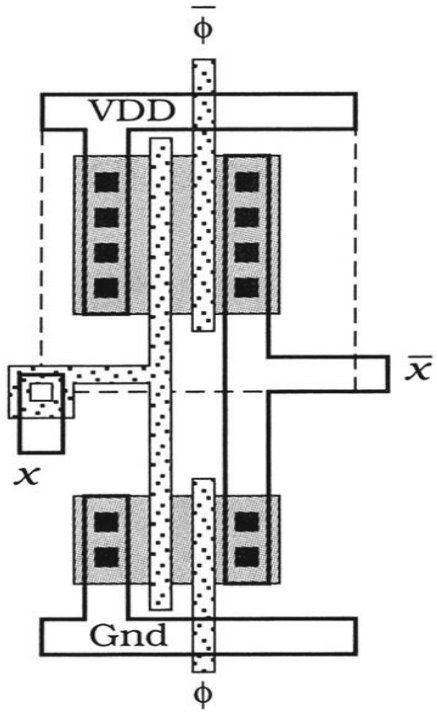


(b) NOR2

Figure 9.13 Example of C²MOS logic gate



(a) Inverter



(b) NAND2

Figure 9.14 Layout examples of C²MOS circuits

Leakage in C²MOS (1 / 2)

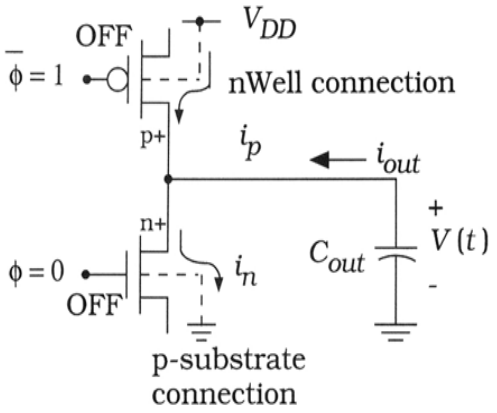
- *Charge leakage*: since the output node cannot hold the charge on V_{out} very long
  - » This places a lower limit on the allowable clock frequency
- If a voltage is applied to the drain or source, a small leakage current flows into, or out of, the device
  - » One reason is due to the required bulk connections
  - » The current off of the capacitor by i_{out}

$$i_{out} = i_n - i_p = -C_{out}\frac{dV}{dt} \quad (9.11)$$

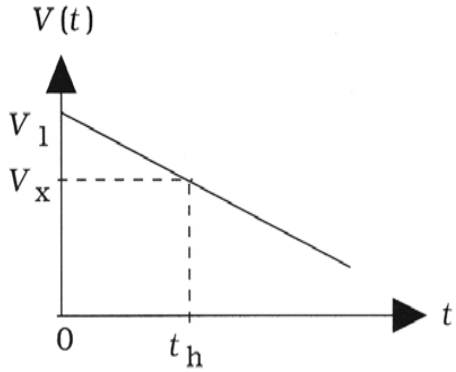
$$I_L = -C_{out}\frac{dV}{dt} \quad (9.12)$$

$$\int_{V_1}^{V(t)} dV = -\int_0^t \left(\frac{I_L}{C_{out}}\right) dt \quad (9.13)$$

$$V(t) = V_1 - \left(\frac{I_L}{C_{out}}\right) t \quad (9.14)$$



(a) Bulk leakage currents



(b) Logic 1 voltage decay

Figure 9.15 Charge leakage problem

Leakage in C²MOS (2 / 2)

$$V(t_h) = V_1 - \left(\frac{I_L}{C_{out}}\right) t_h = V_x \qquad (9.15)$$

$$t_h = \left(\frac{C_{out}}{I_L}\right)(V_1 - V_x) \qquad (9.16)$$

$$t_h = \left(\frac{50\times10^{-15}}{10^{-13}}\right)(1) = 0.5 \quad \text{sec} \qquad (9.17)$$

$$V(t) = \left(\frac{I_L}{C_{out}}\right) t \qquad (9.18)$$

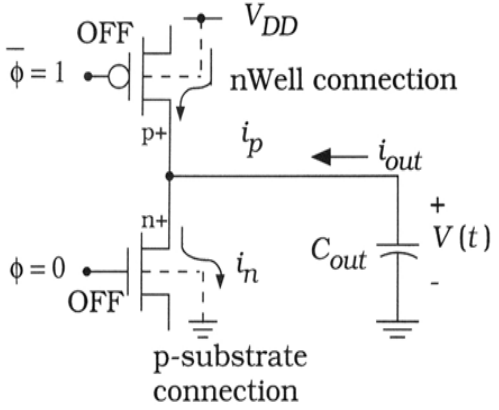
$$I = I_{D0}\left(\frac{W}{L}\right) e^{-(V_{GS}-V_T)/(nV_{th})} \qquad (9.19)$$

$$t_h = \left(\frac{50\times15^{-15}}{10^{-9}}\right)(1) = 50 \quad \mu\text{sec} \qquad (9.20)$$

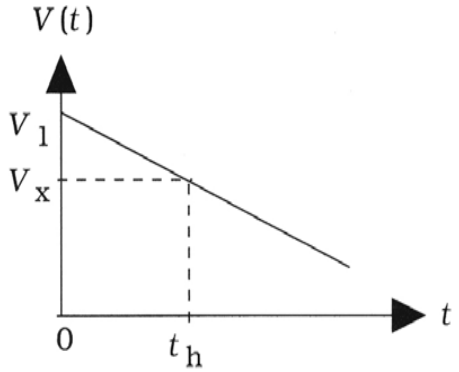
$$t_h = \left(\frac{50\times15^{-15}}{10^{-7}}\right)(1) = 0.5 \quad \mu\text{sec} \qquad (9.21)$$

$$I_L(V) = -C_{out}(V)\frac{dV}{dt} \qquad (9.22)$$

$$\int_0^t dt = \int_{V_x}^{V(t)} \frac{C_{out}(V)}{I_L(V)} dV = t \qquad (9.23)$$



(a) Bulk leakage currents



(b) Logic 1 voltage decay

Figure 9.15 Charge leakage problem

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Dynamic CMOS Logic Circuits (1 / 2)

- A dynamic logic gate uses clocking and charge storage properties of MOSFETs to implement logic operations
  - » Provide a *synchronized* data flow
  - » Result is valid only for a short period of time
  - » Less transistors, and may be faster than static cascades
- Based on the circuit in Figure 9.17
  - » The clock ϕ drives a complementary pair of transistors M_n and M_p
  - » An nFET array between the output node and ground to perform the logic function
  - » When $\phi = 0$, it is called *precharge phase*
  - » When $\phi = 1$, it is called *evaluation phase*

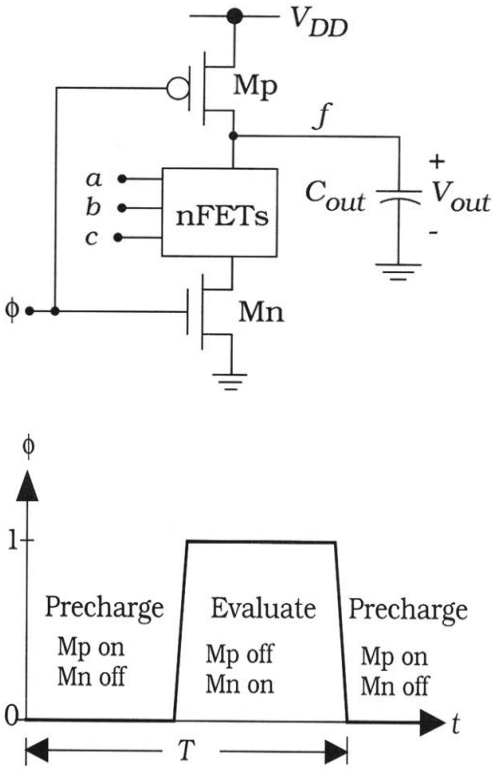


Figure 9.17 Basic dynamic logic gate

Dynamic CMOS Logic Circuits (2/2)

- A dynamic NAND3 is shown in Figure 9.18

$$f = \overline{a \cdot b \cdot c} \qquad (9.24)$$

- When $f = 1$, *charge leakage* reduces the voltages held on the output node

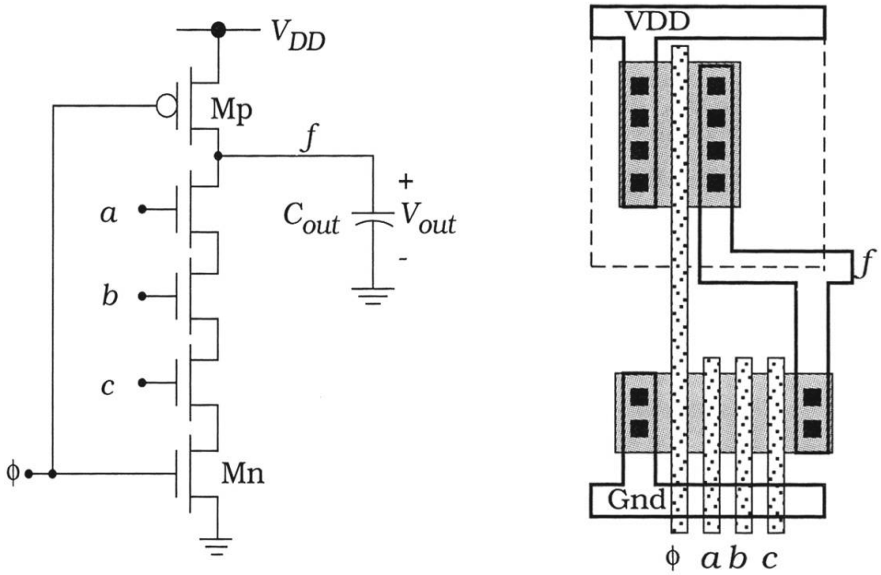


Figure 9.18 Dynamic logic gate example

Charge Sharing Problem

- The origin of the charge sharing problem is the parasitic node capacitance C_1 and C_2 between FETs
  - When clock $\phi \rightarrow 1$, and the capacitor voltage V_1 and V_2 are both 0 V at this time, the total charge is

$$Q = C_{out} V_{DD} \qquad (9.25)$$

  - The worst-case charge sharing condition is when the inputs are at (a, b, c) = (1, 1, 0)

$$V_{out} = V_2 = V_1 = V_f \qquad (9.26)$$ (When the current flow ceases)

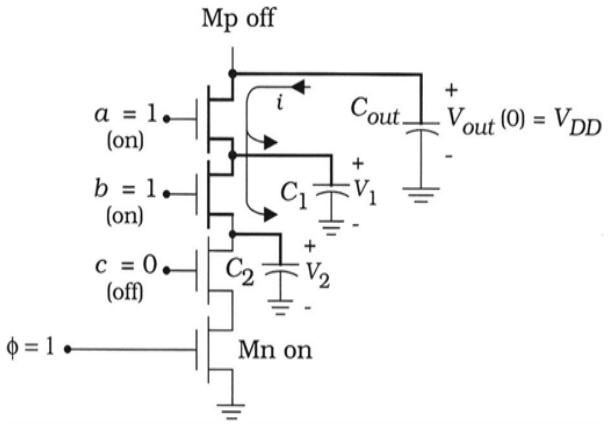


Figure 9.19 Charge sharing circuit

  - The principle of conservation of charge

$$\Rightarrow Q = C_{out} V_f + C_1 V_f + C_2 V_f = (C_{out} + C_1 + C_2) V_f \qquad (9.27)$$

$$\Rightarrow Q = (C_{out} + C_1 + C_2) V_f = C_{out} V_{DD} \qquad (9.28)$$

$$\Rightarrow V_f = \left(\frac{C_{out}}{C_{out} + C_1 + C_2} \right) V_{DD} \qquad (9.29)$$

$$\left(\frac{C_{out}}{C_{out} + C_1 + C_2} \right) < 1 \qquad (9.30)$$

$$V_f < V_{DD} \qquad (9.31)$$

$$C_{out} >> C_1 + C_2 \qquad (9.32)$$

Domino Logic (1/2)

- Domino logic is a CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit
  - » Non-inverting
  - » Cascade operation
  - » "Domino chain reaction" that must start at the first stage and then propagate stage by stage to the output

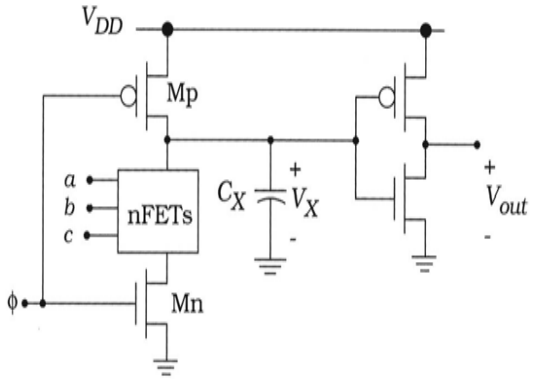
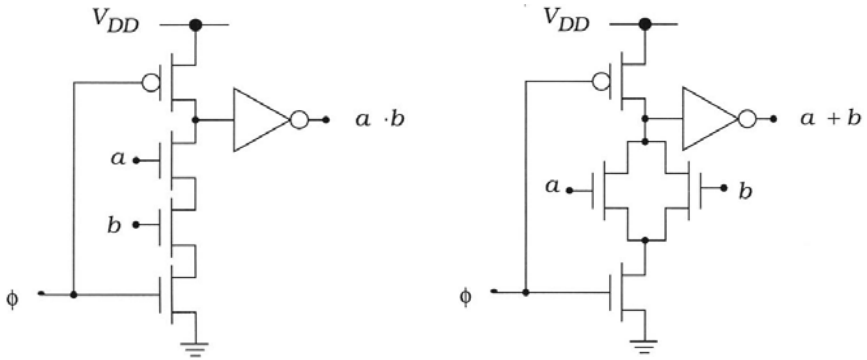


Figure 9.20 Domino logic stage



(a) AND gate (b) OR gate

Figure 9.21 Non-inverting domino logic gates

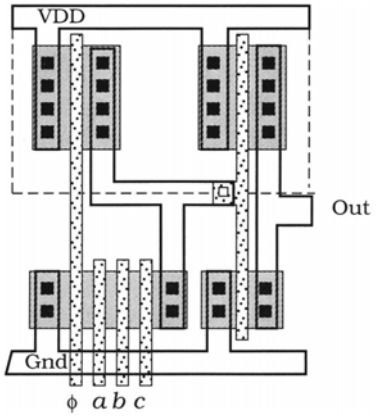


Figure 9.22 Layout for domino AND gate

Domino Logic (2/2)

- Note that the operation indicates that domino gates are only useful in cascades

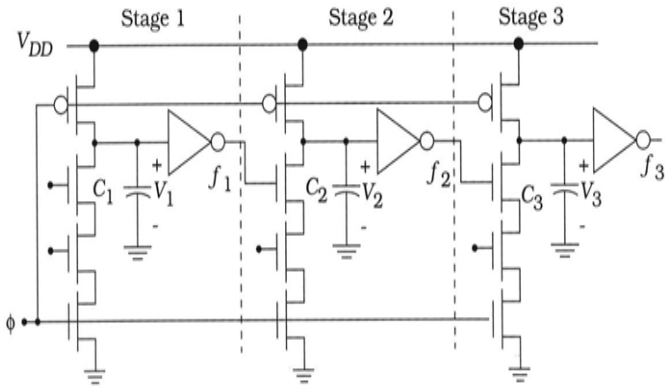
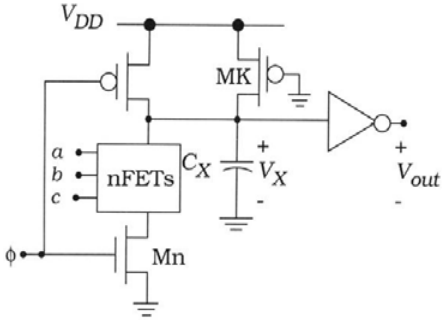
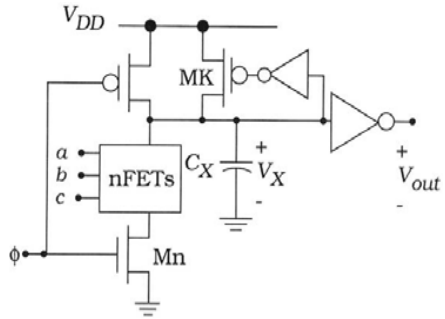


Figure 9.23 A domino cascade

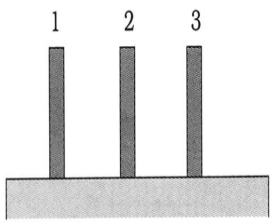


(a) Single-FET charge keeper

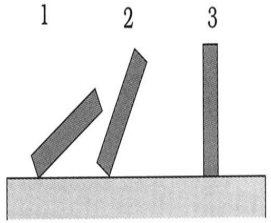


(b) Feedback controlled keeper

Figure 9.25 Charge-keeper circuits



(a) Percharge



(b) Evaluate

Figure 9.24 Visualization of the domino effect

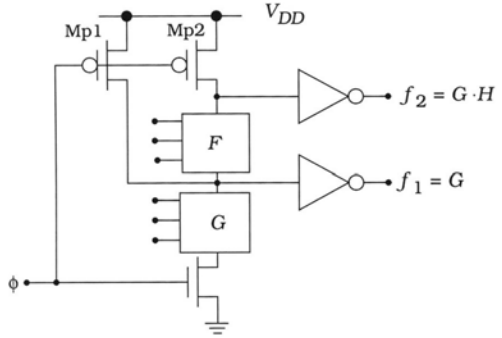


Figure 9.26 Structure of a MODL circuit

$$f_1 = G$$
$$f_2 = F \cdot G \qquad (9.33)$$

Outline

- Mirror Circuits
- Pseudo-nMOS
- Tri-State Circuits
- Clocked CMOS
- Dynamic CMOS Logic Circuits
- Dual-Rail Logic Networks

Dual-Rail Logic Networks

- *Single-rail logic*: the value of a variable is either a 0 or a 1 only
- *Dual-rail logic*: both the variable x and its complement $\bar{x}$ are used to form the difference

$$f_x = (x - \bar{x}) \qquad (9.35)$$

$$\frac{df_x}{dt} = \left(\frac{dx}{dt} - \frac{d\bar{x}}{dt} \right) \qquad (9.36)$$

$$\frac{d\bar{x}}{dt} \approx -\left| \frac{dx}{dt} \right| \qquad (9.37)$$

$$\frac{df_x}{dt} \approx 2\left| \frac{dx}{dt} \right| \qquad (9.38)$$

Differential Cascode Voltage Switch Logic, DCVS (1/2)

- DCVS or differential CVSL (CVSL) provides for dual-rail logic gates, and the out results f and $\overline{f}$ are held until the inputs induce a change

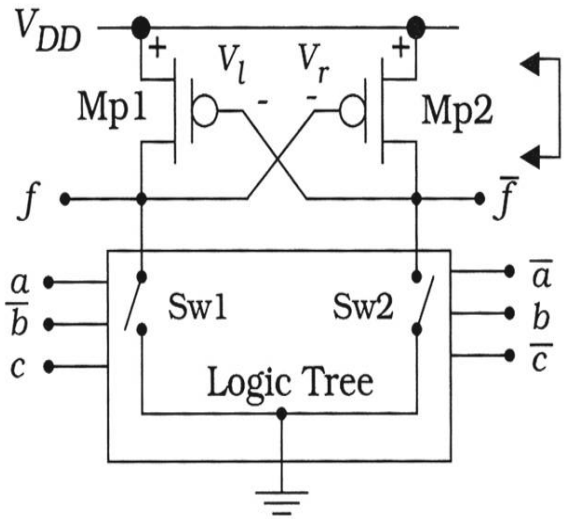
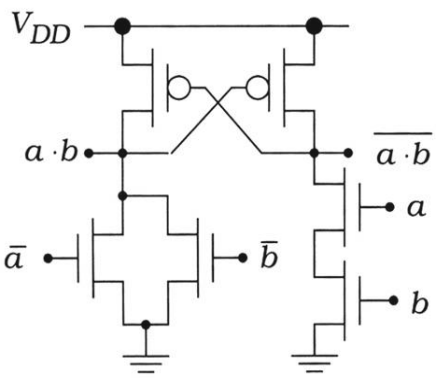
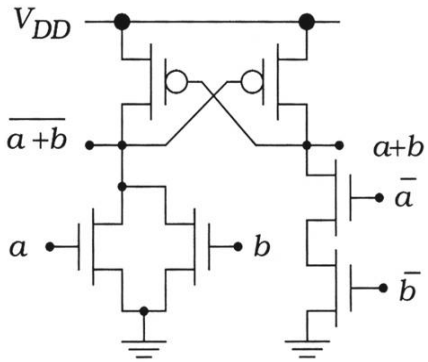


Figure 9.27 Structure of a CVSL logic gate



(a) AND / NAND



(b) OR / NOR

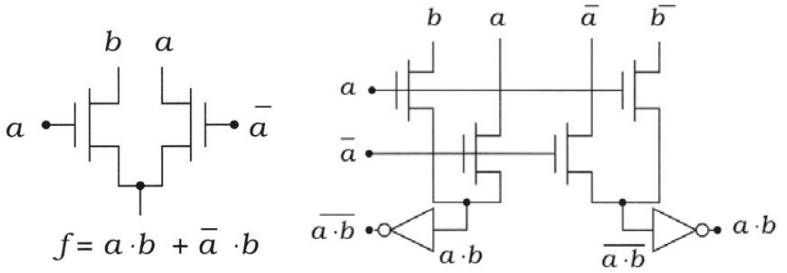
Figure 9.28 CVSL gate example

Complementary Pass-Transistor Logic

- Complementary Pass-Transistor (CPL): an dual-rail tech. that is based on nFET logic equations

$$f = a \cdot b + \bar{a} \cdot a \qquad (9.41)$$

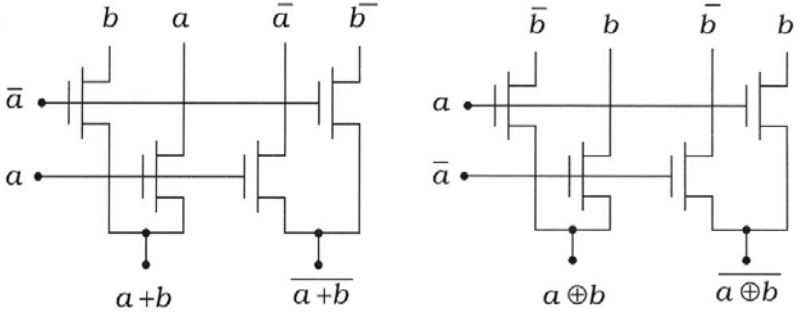
$$\Rightarrow a \cdot \bar{b} + \bar{a} = \bar{a} + \bar{b} = \overline{a \cdot b} \qquad (9.42)$$



(a) AND gate (b) AND / NAND array

Figure 9.32 CPL AND / NAND circuit

- CPL has several 2-input gates that can be created by using the same transistor topology with different input sequences
  - » Less layout area
  - » However, threshold will be loss and the fact that an input variable may have to drive more than one FET terminal



(a) OR / NOR (b) XOR / XNOR

Figure 9.33 2-input CPL arrays