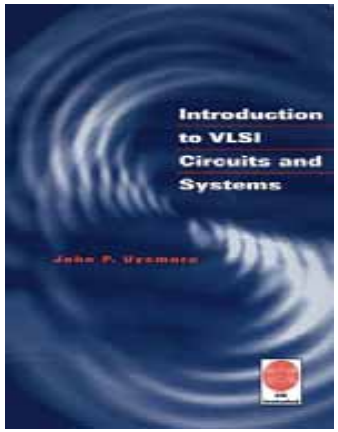
國立勤益科技大學
National Chin-Yi University of Technology

Introduction to VLSI Circuits and Systems
積體電路概論

Chapter 5

Elements of Physical Design



賴秉樑
Dept. of Electronic Engineering
National Chin-Yi University of Technology
Fall 2007

Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- FET Sizing and the Unit Transistor
- Physical Design of Logic Gates
- Design Hierarchies

Physical Design

- What is physical design?
  - To translating logic circuits into *silicon*
  - Switch speed is critical
    - The electrical characteristics of a logic gate depend on the aspect ratios of the transistors (In Chapter 6, we will discuss it)
    - In other words, this is due to both the current flow levels and the parasitic resistance and capacitance (In Chapter 3)
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - VDD and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

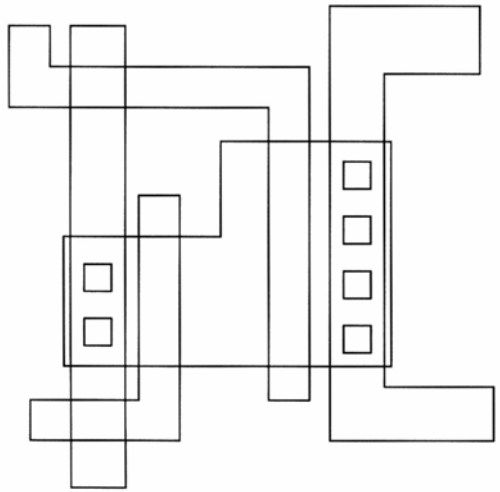
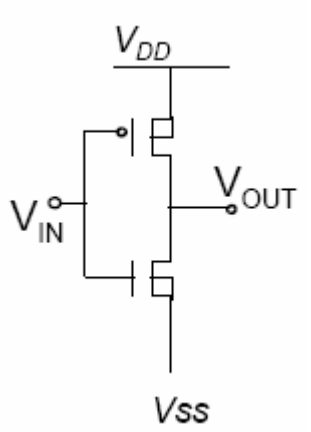
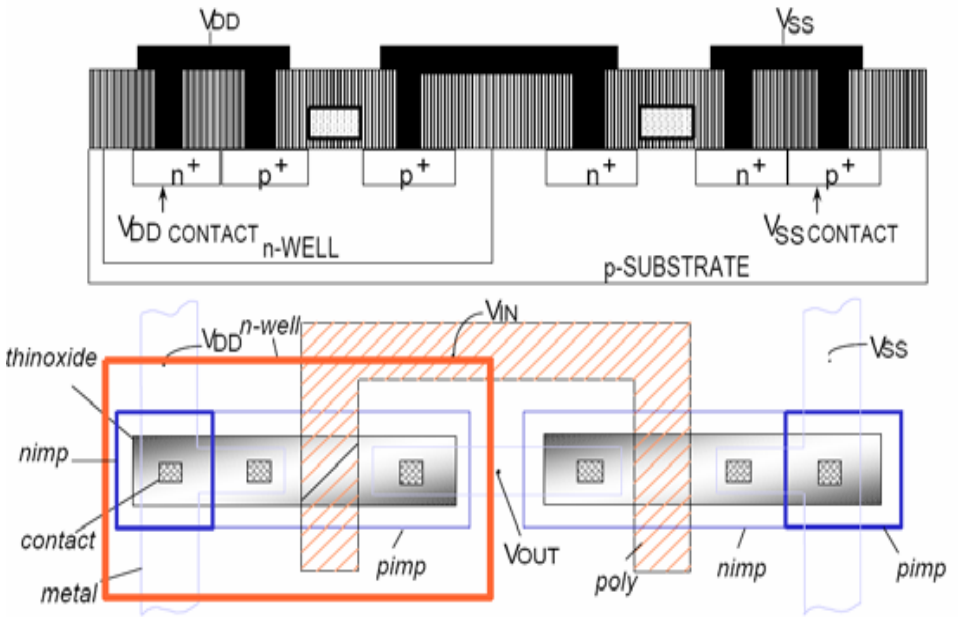


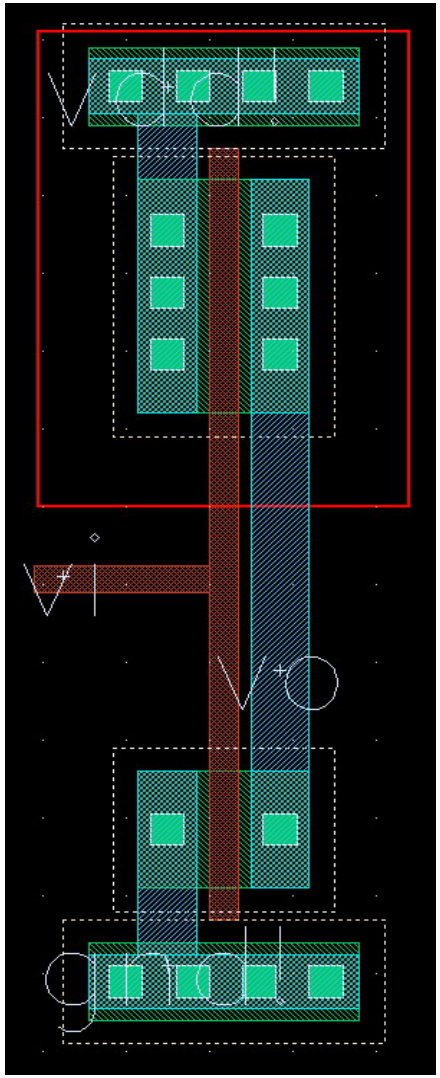
Figure 5.1 Polygons in physical design

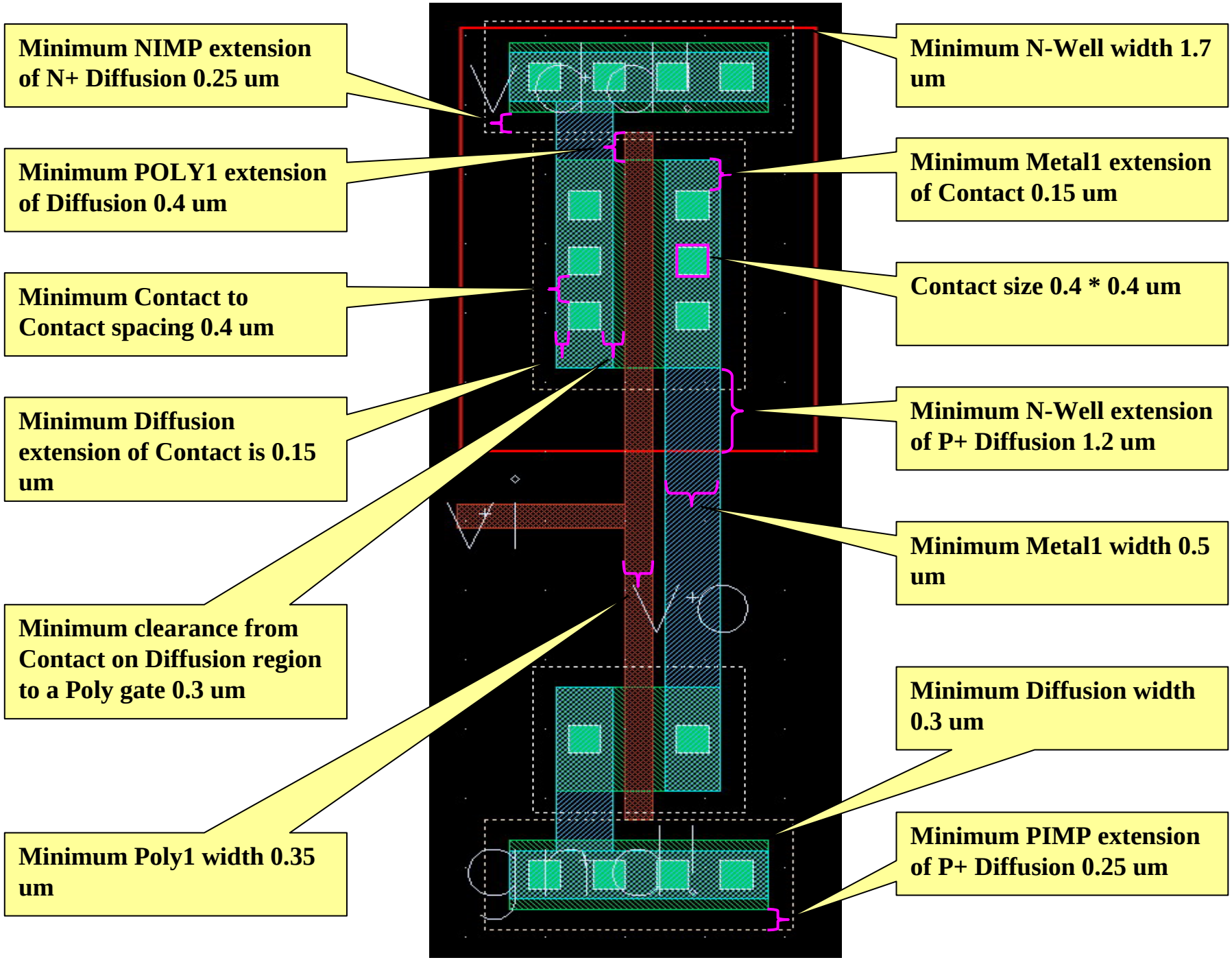
Example: N-Well COMS Inverter



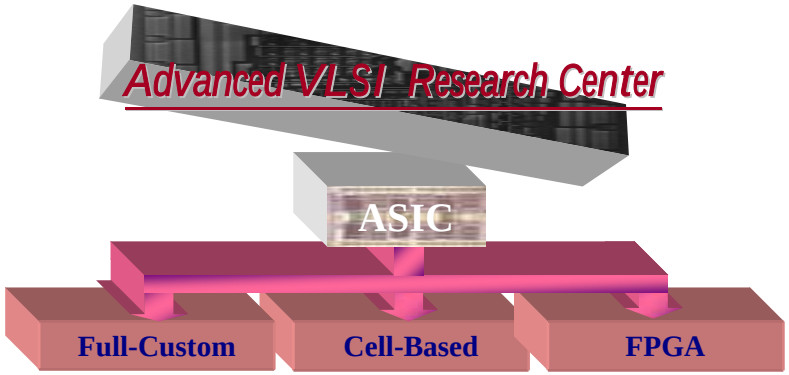


The cross-section view and layout
of a CMOS(n-well) inverter




Minimum NIMP extension of N+ Diffusion 0.25 um
Minimum POLY1 extension of Diffusion 0.4 um
Minimum Contact to Contact spacing 0.4 um
Minimum Diffusion extension of Contact is 0.15 um
Minimum clearance from Contact on Diffusion region to a Poly gate 0.3 um
Minimum Poly1 width 0.35 um
Minimum N-Well width 1.7 um
Minimum Metal1 extension of Contact 0.15 um
Contact size 0.4 * 0.4 um
Minimum N-Well extension of P+ Diffusion 1.2 um
Minimum Metal1 width 0.5 um
Minimum Diffusion width 0.3 um
Minimum PIMP extension of P+ Diffusion 0.25 um

ASIC Design Flow



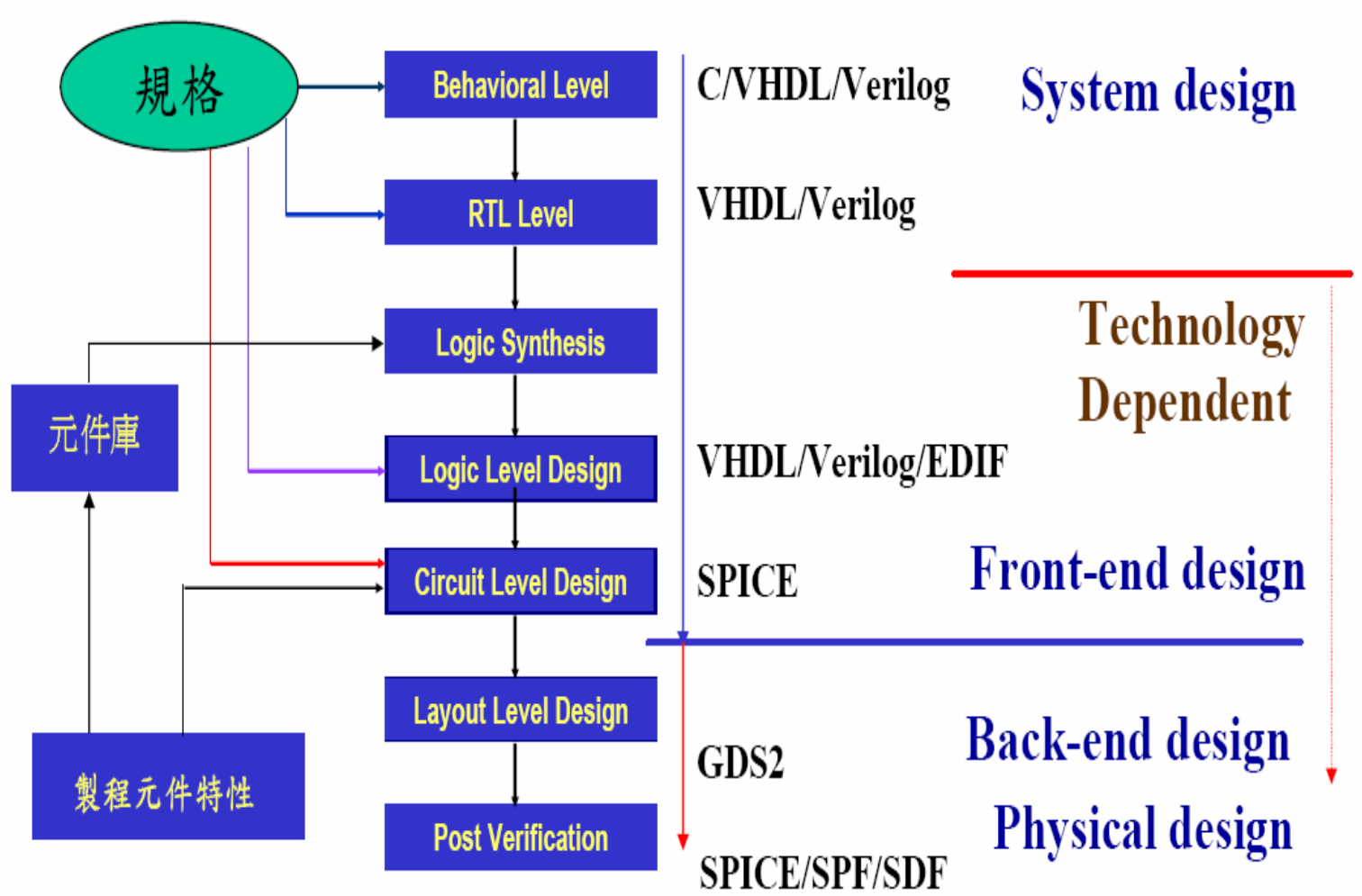
Full Custom Design Flow

Circuit-Level Design
Composer
Pre-Layout Circuit-Sim
Hspice
Spice Model
SBTSPICE
Physical Layout
Virtuoso
Physical Verification & RC Extraction
Dracula
Post-Layout Sim
Hspice
Spice Model & RC
SBTSPICE
Tape Out

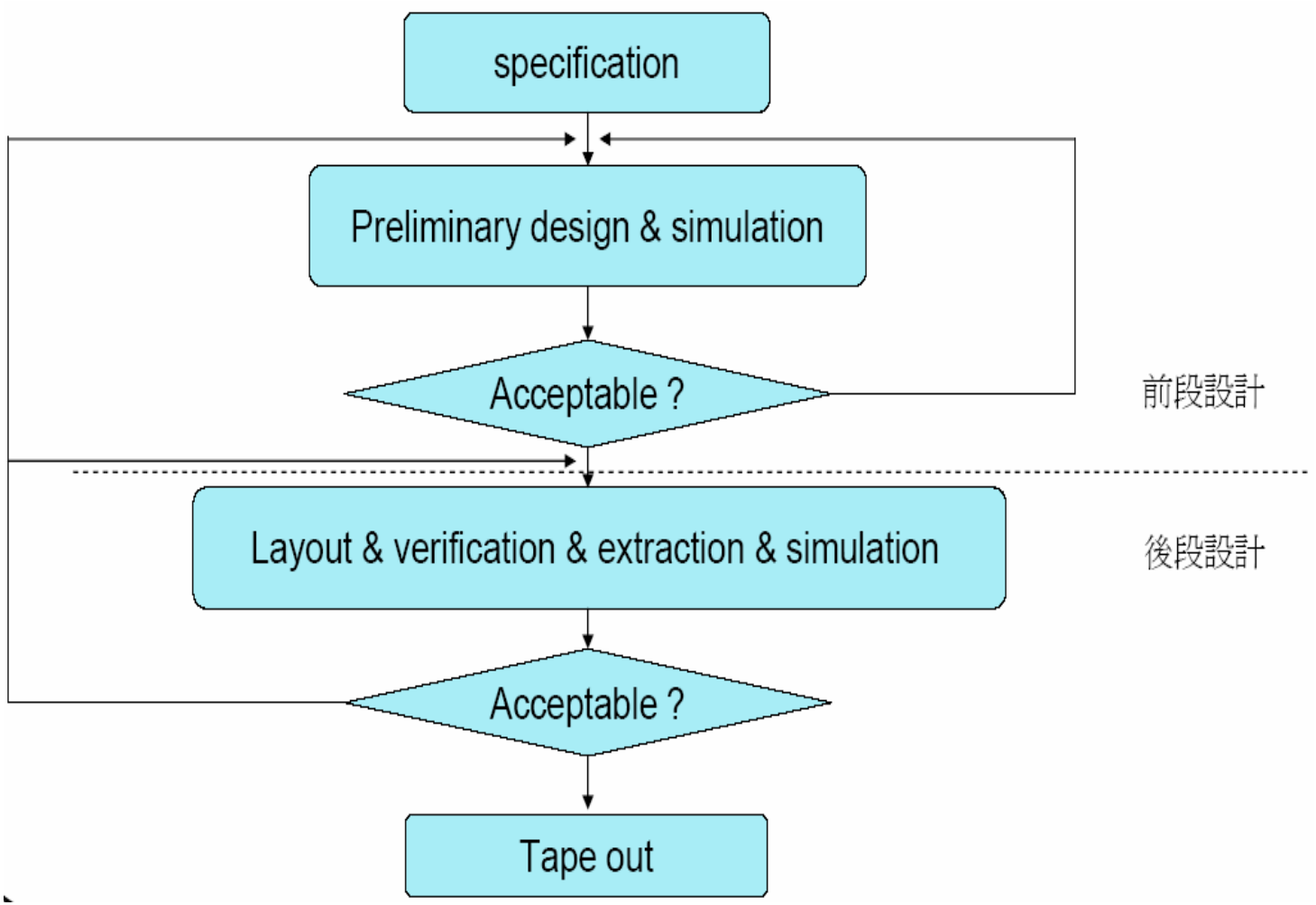
Cell Based Design Flow

Specification
System-Level Design & Sim
SPW
Matlab
BONeS
Behavior Synthesis
Visual Architect
MathWork RTW
RTL-Level Sim
Verilog-XL
Synopsys VCS
RTL Synthesis
Cell Library
Ambit
Design-Compiler
Gate-Level Sim
Cell Library Model
Synopsys VCS
Verilog-XL
Physical Verification
Apollo/Hercules
Silicon Ensemble Ultra / Dracula
RC Extraction
Star-RC
Dracula
Post-Layout Sim
TimeMill
Star-time
Star-sim
Tape Out

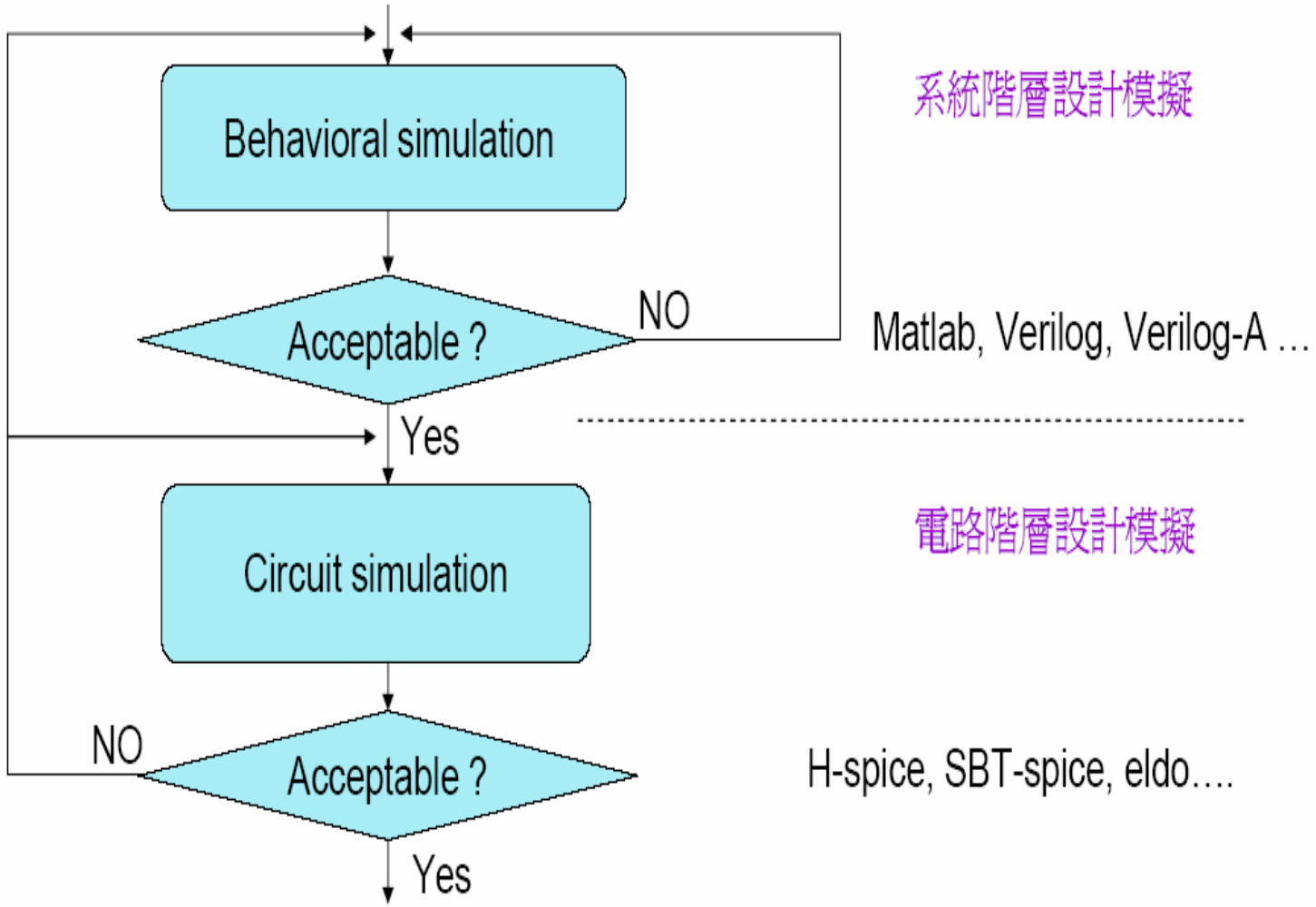
Design of VLSI Flowing



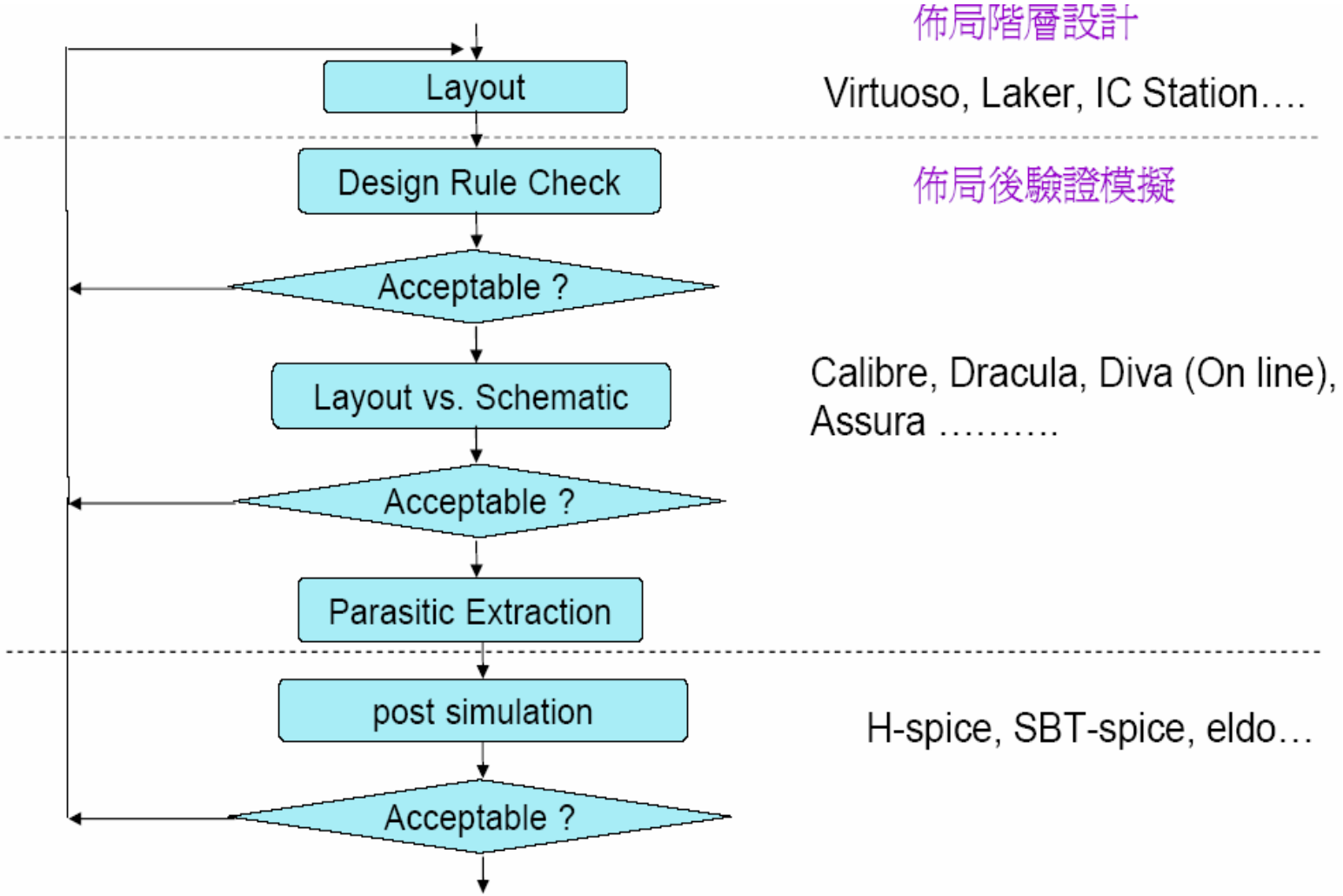
Full-custom IC Design Flow



Preliminary Design & Simulation



Layout & Verification & Extraction & Simulation



雛型IC設計步驟

- 規格定義: 需求時脈頻率，輸出入時序、功能對應...
- 製程選擇: (0.25/0.18, logic, mixed-mode, Embed) CMOS, BiCMOS,GaAs
- 架構選擇: Dynamic/Static logic, Parallel/Serial/Pipelined ...
- 電路設計: 模組分割，需求定義，電路方塊設計與連接
- 電路模擬: 功能模擬，時序驗證...
- 佈局設計: Auto Placement & Route(APR), HandCraft, Using Hard IP
- 佈局驗證: DRC/ERC, LVS, ...
- 佈局後模擬: LPE, Delay Calculation , Back annotation
- 可靠性分析: Electron-migration, ESD, Substrate coupling ...

Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- FET Sizing and the Unit Transistor
- Physical Design of Logic Gates
- Design Hierarchies

Basic Structure of nWell

- nWell technology
  1. Start with p-type substrate
  2. nWell
  3. Active
  4. Poly
  5. pSelect
  6. nSelect
  7. Active contact
  8. Poly contact
  9. Metal1
  10. Via
  11. Metal2
  12. Overglass

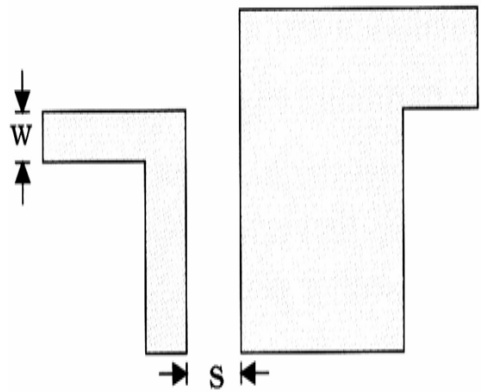


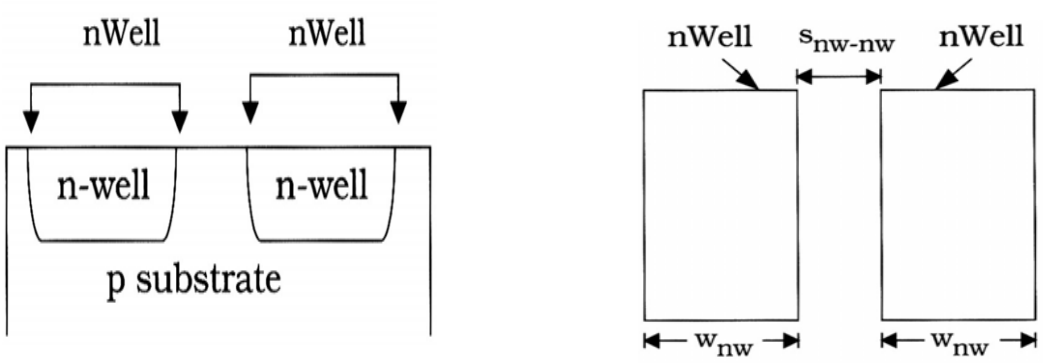
Figure 5.2 Minimum line width and space

- *Manhattan geometries*
  - » Where *all turns are multiples of 90°*
  - » If in an arbitrary manner, then must be sure what the structures are supported by the fabrication process

nWell

- An n-well is required at every location where a pFET is to be made
  - » n-well must be connected to the power supply V_{DD} when used for pFETs

W_{nw} = minimum width of an n-well mask feature
$S_{nw\text{-}nw}$ = minimum edge-to-edge spacing of adjacent n-wells



(a) Cross-section (b) Mask set

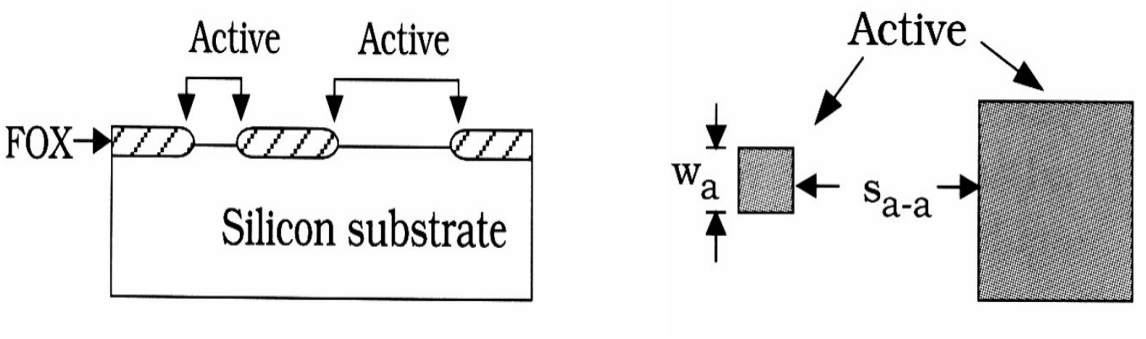
Figure 5.3 n-well structure and mask

Active Areas

- Silicon devices are built on active areas of the substrate

W_a = minimum width of an Active feature
$S_{a\text{-}a}$ = minimum edge-to-edge spacing of Active mask polygons

FOX = NOT (Active) (5.1)
FOX + Active = Surface (5.2)



(a) Cross-section (b) Active patterns

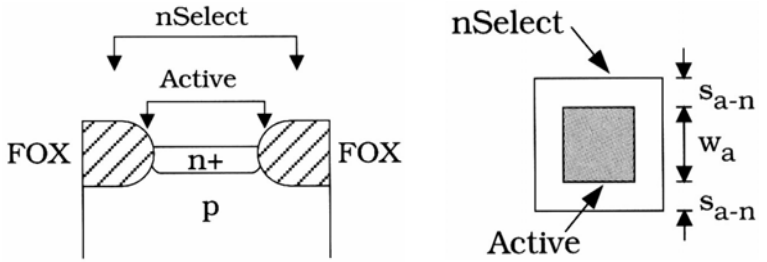
Figure 5.4 Active area definition

Doped Silicon Regions

- Thermal technique called *diffusion*
  - » Create n+ (ndiff, [砷, As] or [磷, p]) and p+ (pdiff, [硼, B]) regions

$$n+ = (nSelect) \cap (Active) \qquad (5.3)$$

W_a = minimum width of an Active area
$S_{a\text{-}n}$ = minimum Active-to-nSelect spacing

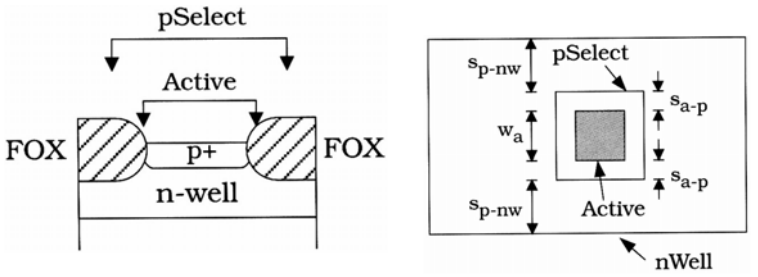


(a) Cross-section (b) Mask set

Figure 5.5 Design of a n+ regions

$$p+ = (pSelect) \cap (Active) \cap (nWell) \qquad (5.4)$$

W_a = minimum width of an Active area
$S_{a\text{-}p}$ = minimum Active-to-pSelect spacing
$S_{p\text{-}nw}$ = minimum pSelect-to-nSelect spacing



(a) Cross-section (b) Mask set

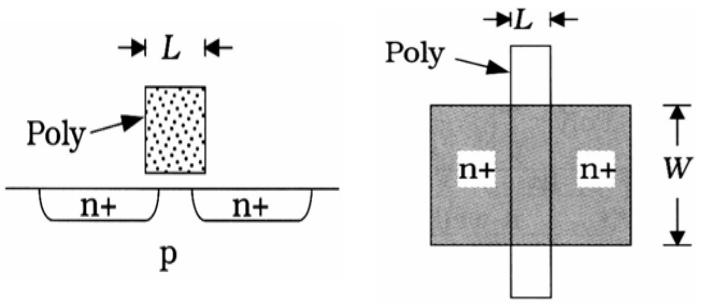
Figure 5.6 Design of a p+ regions

MOSFETs (1 / 2)

- Physically, the poly line is deposited before the ion implant, and acts to block dopants from entering the silicon
- nFETs

W_p = minimum poly width
$S_{p\text{-}p}$ = minimum poly-to-poly spacing
$L = W_p$ = minimum width (length) of a Poly line
d_{po} = minimum extension of Poly beyond Active

nFET = (nSelect)∩(Active)∩(Poly) (5.5)
n+ = (nSelect)∩(Active)∩(NOT [Poly]) (5.6)



(a) Cross-section (b) Layout view

Figure 5.7 nFET structure

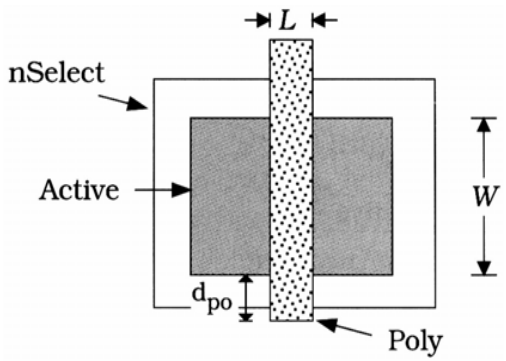
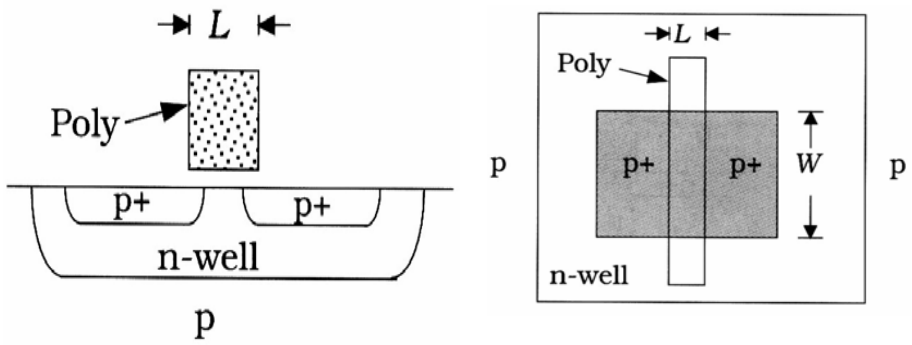


Figure 5.8 Masks for the nFET

MOSFETs (2 / 2)

- pFETs

$$\text{pFET} = (\text{pSelect}) \cap (\text{Active}) \cap (\text{Poly}) \cap (\text{nWell}) \quad (5.7)$$
$$\text{p+} = (\text{pSelect}) \cap (\text{Active}) \cap (\text{nWell}) \cap (\text{NOT [Poly]}) \quad (5.8)$$



(a) Cross-section (b) Layout view

Figure 5.9 pFET structure

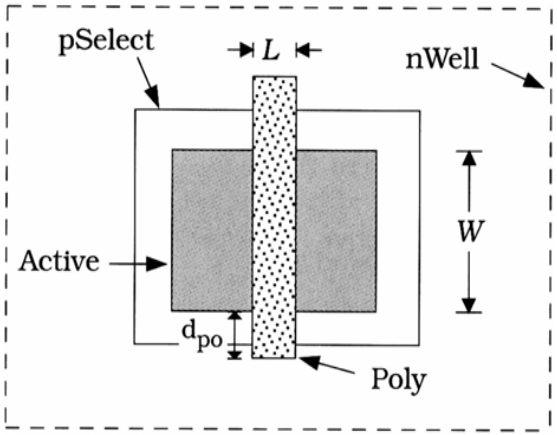


Figure 5.10 Masks for the pFET

Drawn and Effective in MOSFETs

- Draw and Effective Values in MOSFETs
  - » The critical dimensions of a MOSFET are the channel length *L* and the channel width *W*
- The physical length is small than L due to lateral doping during the implant annealing step
  - » L_{eff}: electrical or effective channel length
  - » L_o: overlap distance on both sides

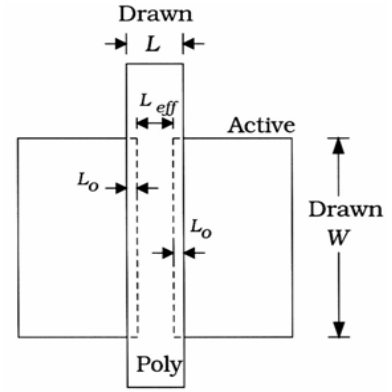
$$L_{eff} = L - 2L_o \qquad (5.9)$$

$$L_{eff} = L - \Delta L \qquad (5.10)$$

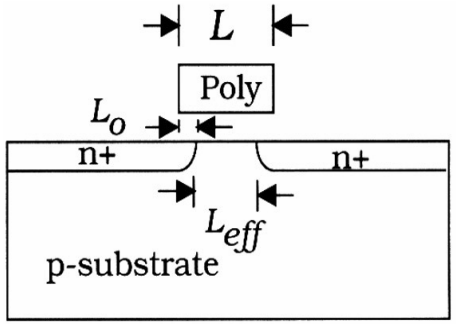
- The channel width is also small than the drawn value due to reduction of active area by the field oxide growth

$$W_{eff} = W - \Delta W \qquad (5.11)$$

$$\frac{W_{eff}}{L_{eff}} \qquad (5.12)$$



(a) Drawn Layout



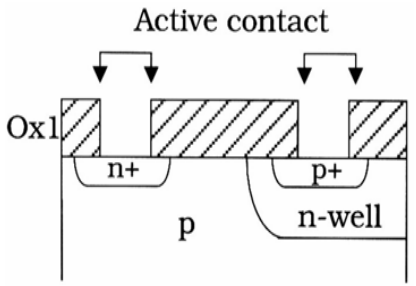
(b) Finished view

Figure 5.11 Drawn and effective dimensions of a MOSFET

Active Contacts

- An *active contact* is a cut in the Ox1 that allows the first layer of metal1 to contact an active n+ or p+ region

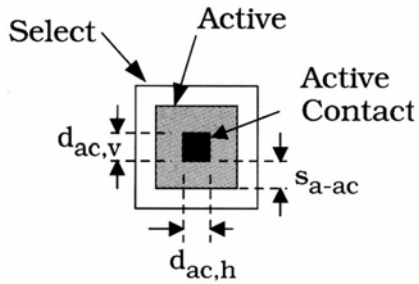
$S_{a\text{-}ac}$ = minimum spacing between Active and Active Contact
$d_{ac,\,v}$ = vertical size of the contact
$d_{ac,\,h}$ = horizontal size of the contact



(a) Cross-section

- A square contact is obtained if, *however*, it is not uncommon to have aspect rations other than 1:1

$$d_{ac,\,v} = d_{ac,\,h} = d_{ac} \qquad (5.13)$$



(b) General mask set

Figure 5.12 Active contact formation

Metal1 (1 / 3)

- Metal1 is used as interconnect for signals and power supply distribution

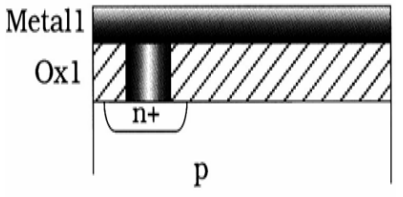
W_{m1} = minimum width of a Metal1 line
$S_{m1\text{-}ac}$ = minimum spacing from Metal1 to Active Contact

  - » Every contact is characterized by a resistance

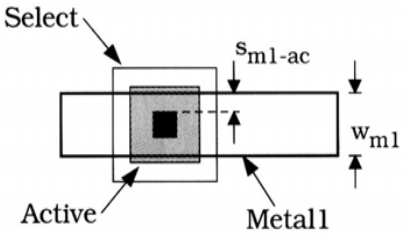
$$R_c = \text{contact resistance } \Omega$$

  - » Since the contacts are all in parallel, the effective resistance of the Metal1-Active connection with N contacts is reduced to

$$R_{c,\,eff} = \frac{1}{N} R_c \qquad (5.14)$$



(a) Cross-section



(b) General mask set

Figure 5.13 Metal1 line with Active Contact

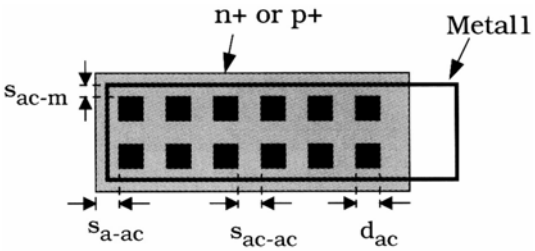
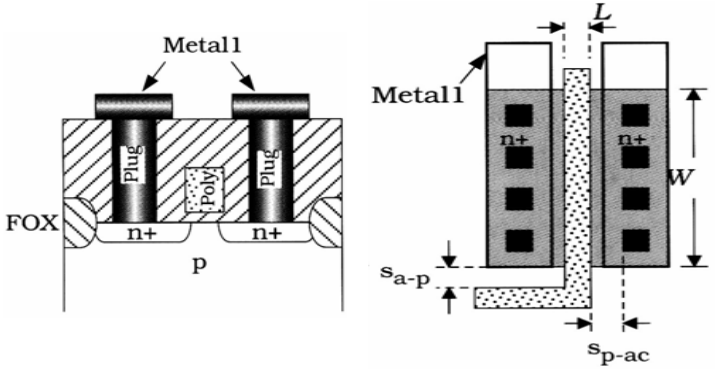


Figure 5.14 Multiple contacts

Metal1 (2 / 3)

- Metal1 allows access to the active regions of MOSFETs using the Active Contact oxide cut as Figure 5.15

$S_{p\text{-}ac}$ = minimum spacing from Poly to Active Contact
$S_{a\text{-}p}$ = minimum spacing from Active to Poly

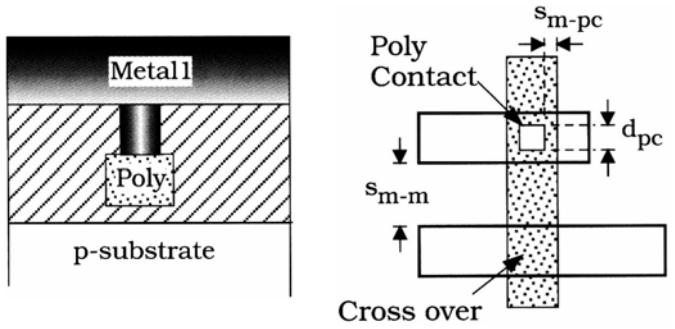


(a) Cross-section (b) Layout

Figure 5.15 Drain and source FET terminals using Metal1

- A Poly Contact mask is used to allow electrical connections between Metal1 and the polysilicon gate as Figure 5.16

$S_{p\text{-}p}$ = minimum Poly-to-Poly spacing



(a) Cross-section (b) Layout

Figure 5.16 Poly Contact

Metal1 (3 / 3)

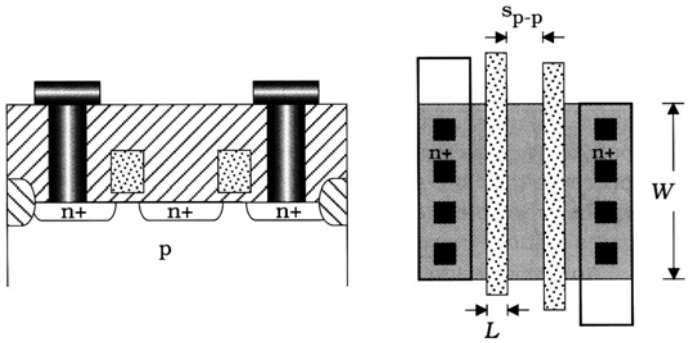
- Example: A pair of series-connected FETs sharing the central n+ region as Figure 5.17

$S_{p\text{-}p}$ = minimum Poly-to-Poly spacing

- Example: Parallel-connected FETs as Figure 5.18

$S_{g\text{-}g} = d_{ac} + 2\,S_{p\text{-}ac}$ (distance between the two gates)

- Example: allow for the size of the contact itself, plus two units of poly-active spacing as Figure 5.19
  - » Enforced twice $S_{p\text{-}a}$



(a) Cross-section (b) Layout

Figure 5.17 Series-connected FETs

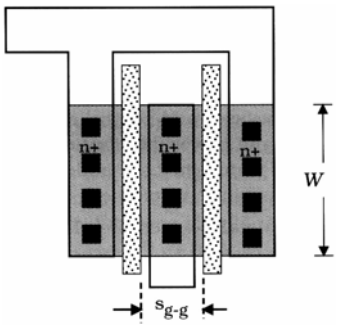


Figure 5.18 Parallel-connected nFETs

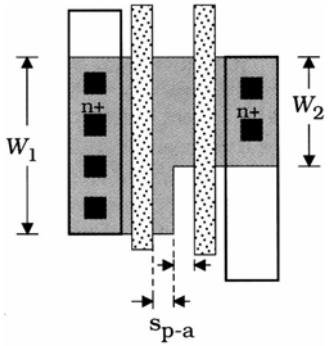
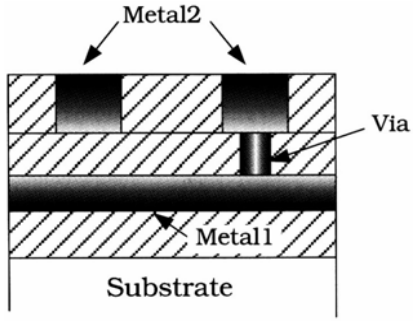


Figure 5.19 Different channel widths using the same active region

Vias and Higher Level Metals

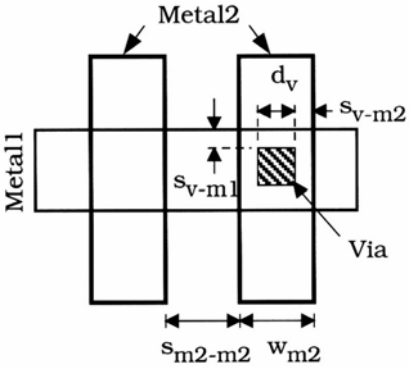
- Model CMOS processes add several additional layers of metal that can be used for signal and power distribution

Metal1 → Metal2 → Metal3 → Metal4



(a) Cross-section

d_v = dimension of a Via (may be different for vertical direction)
w_{m2} = minimum width of Metal2 feature
$s_{m2\text{-}m2}$ = minimum spacing between adjacent Metal2 features
$s_{v\text{-}m1}$ = minimum spacing between Via and Metal1 edges
$S_{v\text{-}m2}$ = minimum spacing between Via and Metal2 edges



(b) Layout

Figure 5.20 Metal1-Metal2 connection using a Via mask

Latch-up Prevention

- *Latch-up*: is a condition that can occur in a circuit fabricated in a bulk CMOS technology
  - The key to understanding latch-up is noting that the bulk technology gives a **4-layers pnpn** structure between the power supply VDD and ground
  - If VDD reaches the **breakover voltage** V_{BO}, the blocking is overwhelmed by internal electric fields

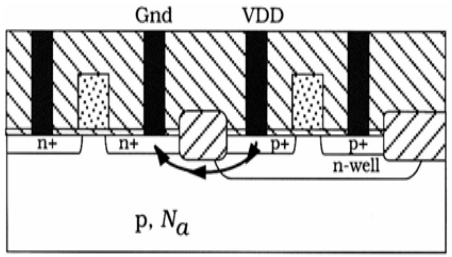
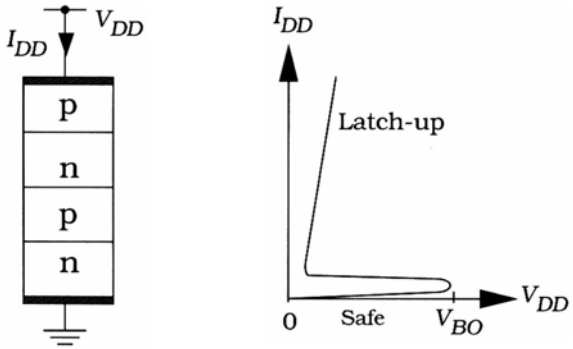


Figure 5.21 Latch-up current flow path

- Latch-up avoiding method
  - to steer the current out of the "bad" path
    - Include and n-Well contact every time a pFET is connected to the power supply VDD, and
    - Include a p-substrate contact every time and nFET is connected to a ground rail
  - Silicon-on-insulator, SOI
  - Twintub: using two separate wells for FETs, an n-well for pFETs and a p-well for nFETs



(a) Structure (b) Behavior

Figure 5.22 Characteristics of 4-layer pnpn device

Layout Editors

- Several and critical items
  - n+ is formed whenever Active is surrounded by nSelect; this is also called ndiff.
  - p+ is formed whenever Active is surrounded by pSelect; this is also called pdiff.
  - A nFET is formed whenever Poly cuts an n+ region into two separate segments.
  - A pFET is formed whenever Poly cuts an p+ region into two separate segments.
  - No electrical current path exists between conducting layer (n+, p+, Poly, Metal, etc.) unless a contact cut (Active Contact, Poly Contact, or Via) is provided.
- Basic features of layout
  - Polygon of the specific object
  - Grid size
  - Undefined order for these shape
  - Design rules must be obeyed
  - Only the outline is important

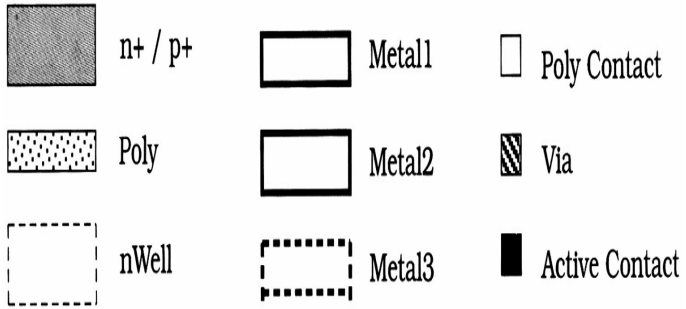
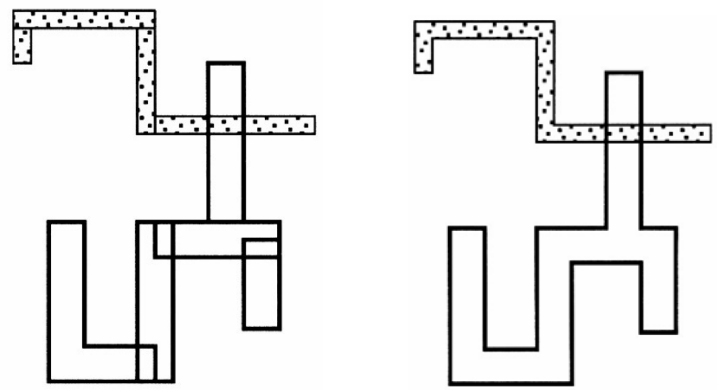


Figure 5.24 Layer key for layout drawings in this book



(a) Structure (b) Behavior

Figure 5.25 Drawing complex polygons using rectangles

Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- FET Sizing and the Unit Transistor
- Physical Design of Logic Gates
- Design Hierarchies

Cell-based Concept

- Cell-based: once a set are defined, they may be used to create more complex networks
- A function using unit gate of Figure 5.26

$$f = \overline{a} \cdot b \qquad (5.16)$$

$$\Rightarrow 2X_{NOT} + X_{NAND} \qquad (5.17)$$

- In this case, a new complex cell F1 will become to the new unit component, and this block without decomposing it into the primitive cells

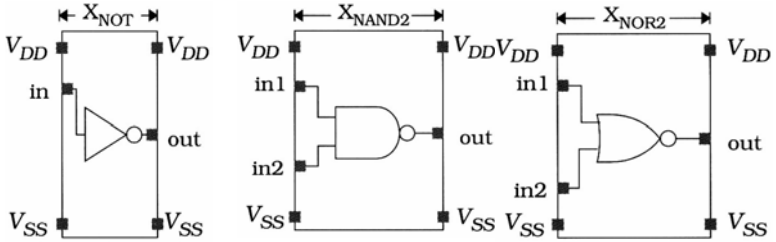
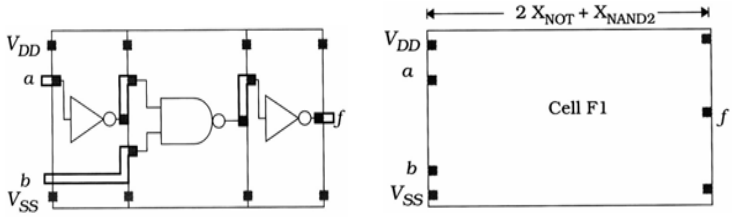


Figure 5.26 Logic gates as basic cells



(a) Primitive (b) New complex cell

Figure 5.27 Creation of a new cell using basic units

Cell-based: VDD & VSS Placement

- Power supply lines placement
  - Both are shown on the Metal1

$D_{m1\text{-}m1}$ = Edge-to-Edge distance between VDD and VSS

  - Pitch

$P_{m1\text{-}m1}$ = Distance between the middle of the VDD and VSS lines

  - The two are related by, where WDD is the width of the power supply lines

$$P_{m1\text{-}m1} = D_{m1\text{-}m1} + W_{DD} \quad (5.18)$$

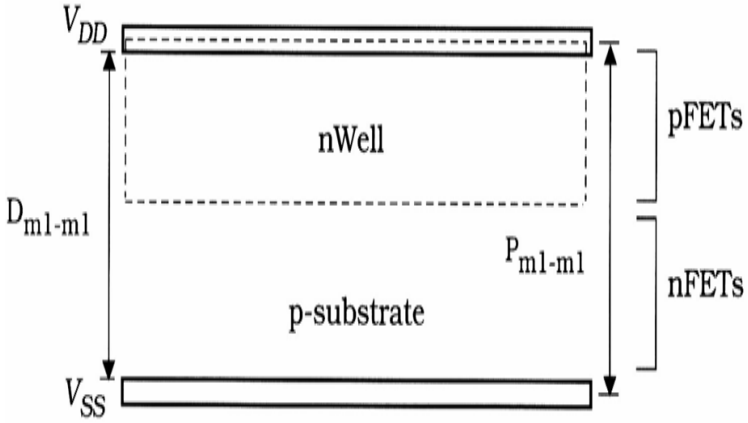


Figure 5.28 VDD and VSS power supply lines

Cell-based: FET Placement

- Two approaches to place FETs: *Horizontal* and *Vertical* direction

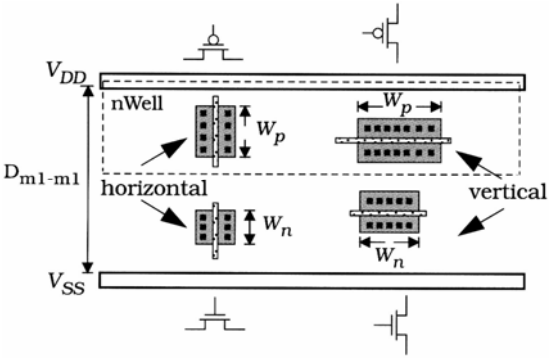
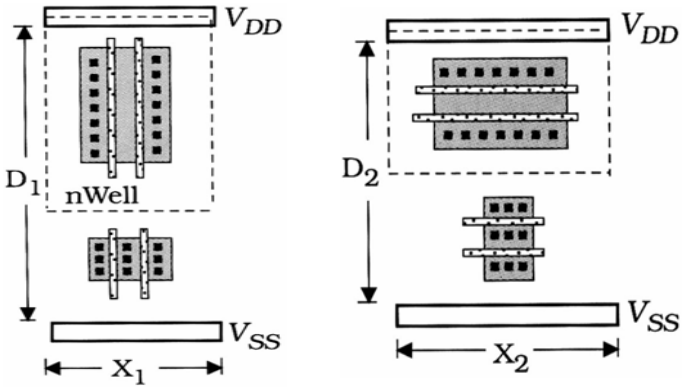
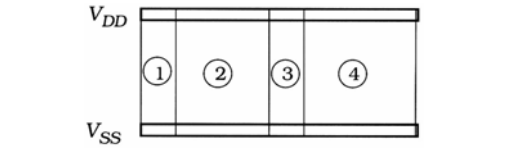


Figure 5.29 MOSFET orientation

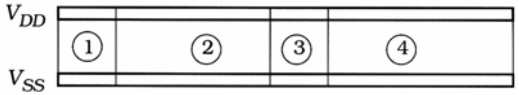


(a) Horizontal FETs (b) Vertical FETs

Figure 5.30 Effect of FET orientation on cell dimensions



(a) Large D



(b) Smaller D

Figure 5.31 Effect of tile shapes on large cells

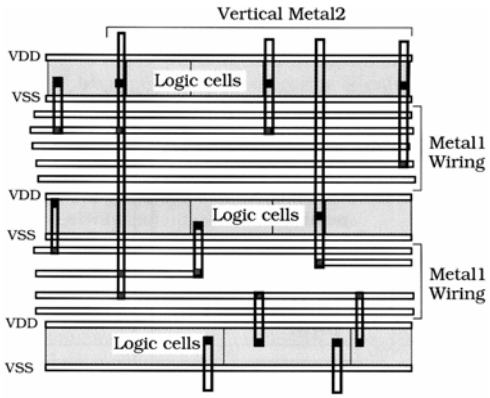


Figure 5.32 Wiring channels

Weinberger Image Placement

- A high-density technique is to alternate VDD and VSS power lines
  - » "Inverted logic cells" are defined to be flipped in relation to the rows of "Logic cells"
  - » High-density placement rate
- Major drawback: must use Metal2 or higher metal layer to achieve this approach

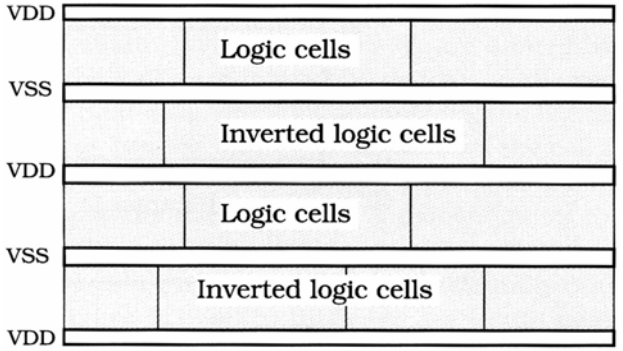


Figure 5.33 Weinberger image array

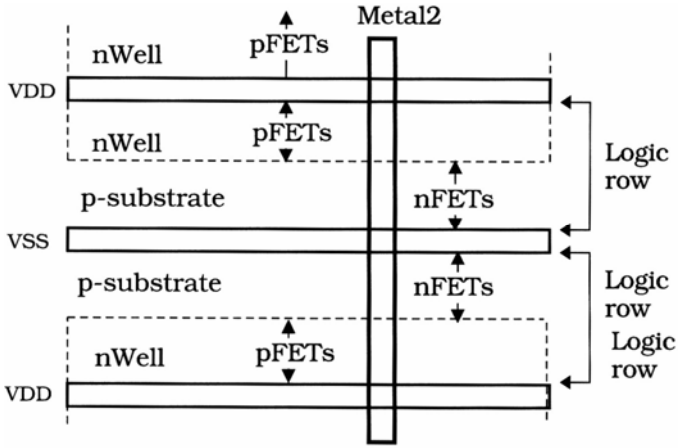


Figure 5.34 FET placement in a Weinberger array

Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- FET Sizing and the Unit Transistor
- Physical Design of Logic Gates
- Design Hierarchies

FET Sizing

- FET are specified by the aspect ratio (W/L)
  - Combine with the processing parameters to give the electrical characteristic of the transistor
  - Given the gate area by $A_G = LW$

$$C_G = C_{ox} WL \quad (5.19)$$

  - Since $I_D \approx I_S$

$$R_{chan} = R_{s,c}\left(\frac{L}{W}\right) \Rightarrow R_{chan} \propto \frac{1}{W} \quad (5.21, 5.22)$$

  - Since $\mu_n > \mu_p$

$$r = \frac{\mu_n}{\mu_p} \Rightarrow \frac{R_p}{R_n} = r \quad (5.24, 5.25) \quad (r = 2 \sim 3)$$

$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n \quad (5.26)$$

pFETs don't conduct as well as nFETs

$$C_{Gp} = rC_{Gn} \quad (5.27)$$

(Since C is proportional to W)

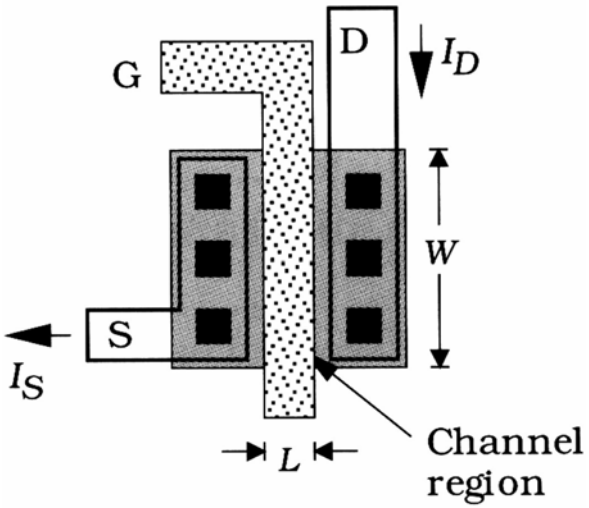


Figure 5.36 Basic geometry of a FET

Unit Transistors

- Unit transistor is the minimum-size MOSFET

$$\left(\frac{W}{L}\right)_{\min} = \frac{w_a}{w_b} \qquad (5.30) \qquad \text{(the aspect ratio)}$$

$$C_G = C_{ox} w_a w_p \qquad (5.31) \qquad \text{(gate capacitance)}$$

d_c = dimension of the contact
$s_{a\text{-}ac}$ = spacing between Active and Active Contact

  - » As Figure 5.38, the minimum width is now

$$W = d_c + 2s_{a\text{-}ac} \qquad (5.32)$$

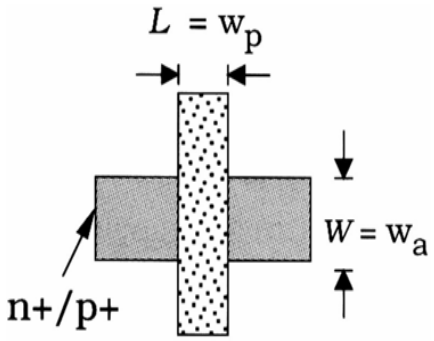
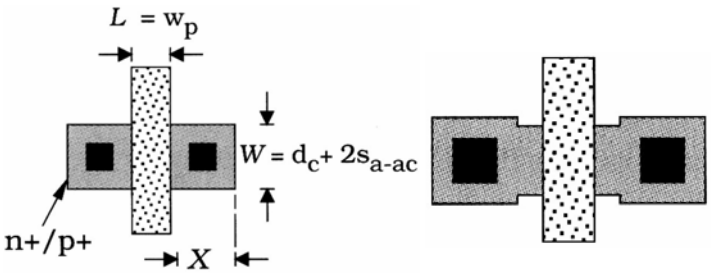


Figure 5.37 Geometry of a minimum-size FET



(a) Active contact (b) Small W_a

Figure 5.38 Minimum-size FETs with Active Contact features

Scaling Technology

- Once a unit FET has been selected, it's useful to allow it to be scaled in size
  - » Reference 1X → 2X → 4X
  - » However, Altering the size of the transistor changes its resistance and capacitance
- Denote R_{1X} and C_{1X} be the R and C of the 1X device

$$W_{SX} = SW_{1X} \quad (5.33) \quad (S\text{: Scaling factor})$$

$$W_{4X} = 4W_{1X} \quad (5.34) \quad (S = 4)$$

$$R_{SX} = \frac{R_{1X}}{S} \qquad C_{SX} = SC_{1X} \quad (5.35) \quad \text{(decided by FET size)}$$

$$R_{2X} = \frac{R_{1X}}{2} \qquad C_{2X} = 2C_{1X} \quad (5.36) \quad (S = 2)$$

$$2(R_{1X}/2) = R_{1X} \quad (5.37) \quad \text{(Figure 5.40)}$$

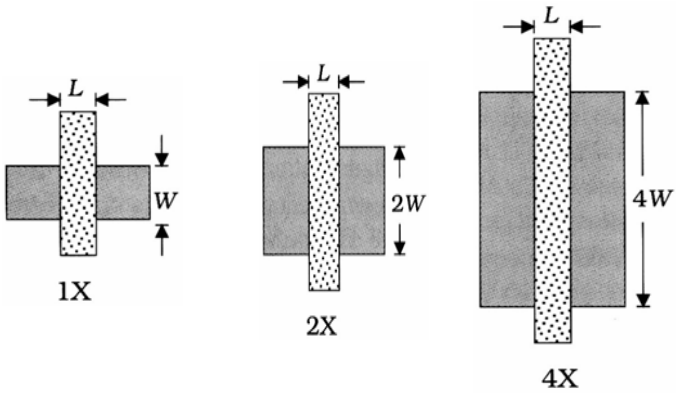


Figure 5.39 Scaling of the unit transistor

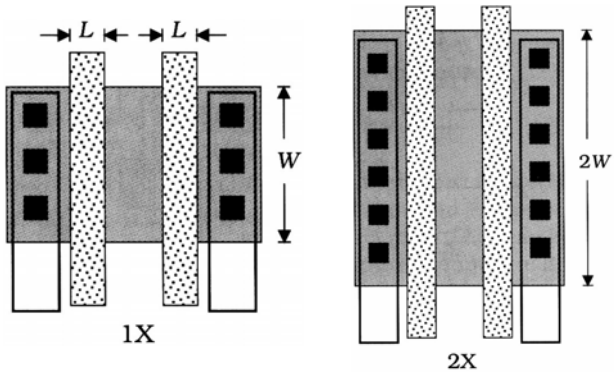
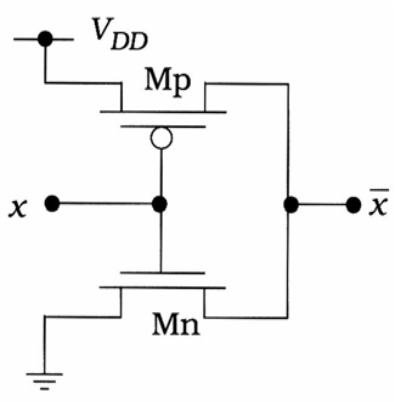


Figure 5.40 Scaling of series-connected FET chain

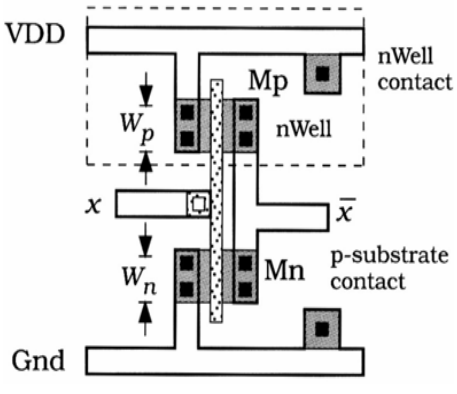
Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- FET Sizing and the Unit Transistor
- Physical Design of Logic Gates
- Design Hierarchies

The Not Cell

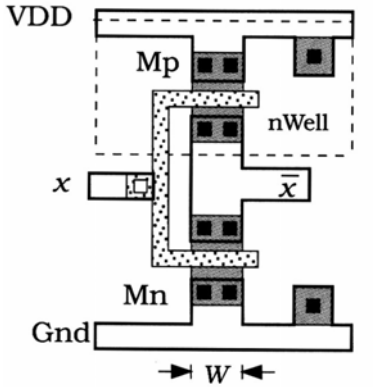


(a) Schematic

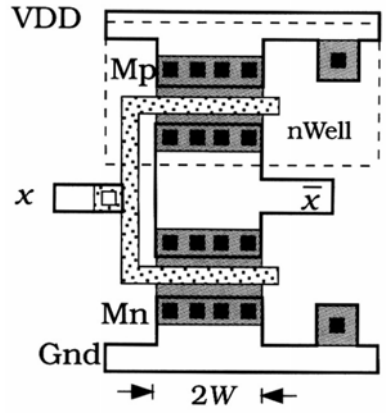


(b) Cell layout

Figure 5.42 NOT gate width horizontal FETs



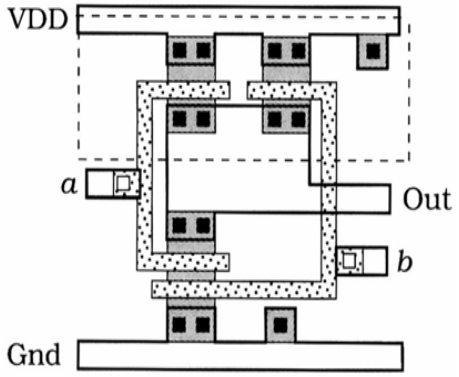
(a) Basic cell



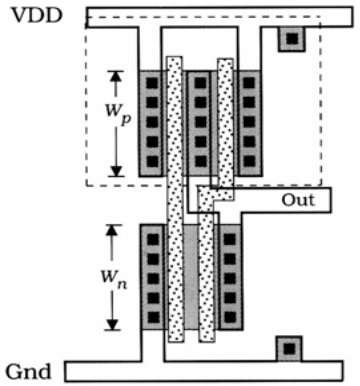
(b) 2X cell

Figure 5.43 Not layout using vertical FETs

NAND2 and NOR2

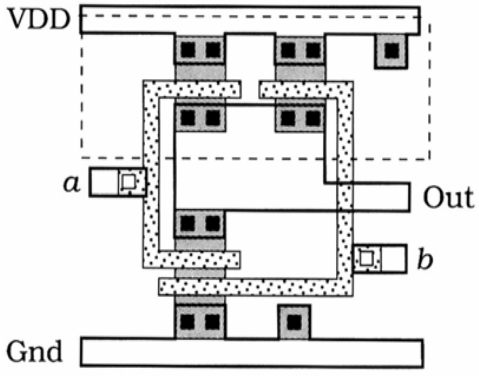


(a) NAND2

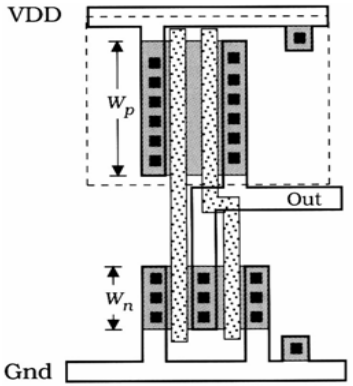


(b) NOR2

Figure 5.45 NAND2 and NOR2 layouts using vertical FETS



(a) NAND2



(b) NOR2

Figure 5.46 Alternate NAND2 and NOR2 cells

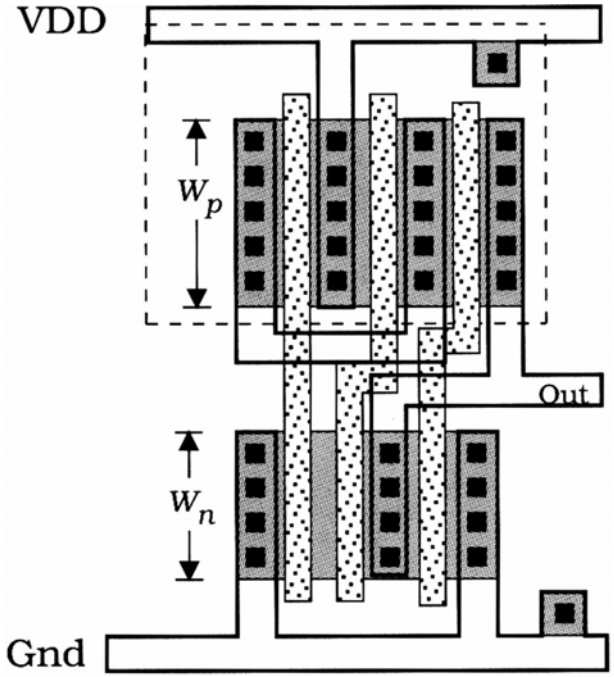


Figure 5.47 Complex logic gate example

Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- FET Sizing and the Unit Transistor
- Physical Design of Logic Gates
- Design Hierarchies

Design Hierarchies

- Top-down hierarchy design
- Bottom-up hierarchy design

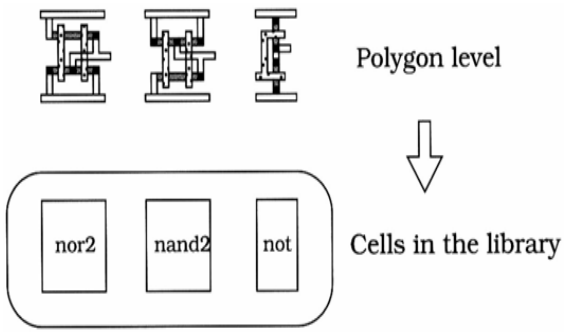


Figure 5.48 Primitive polygon-level library entries

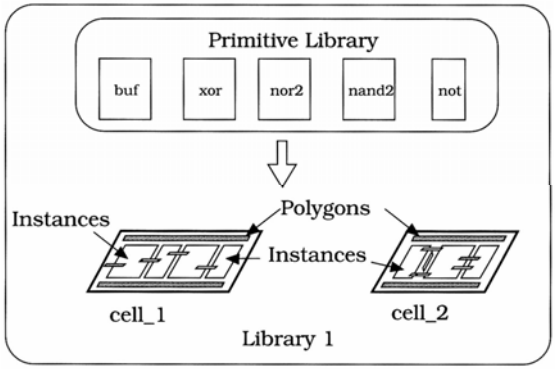


Figure 5.49 Expanding the library with more complex cells

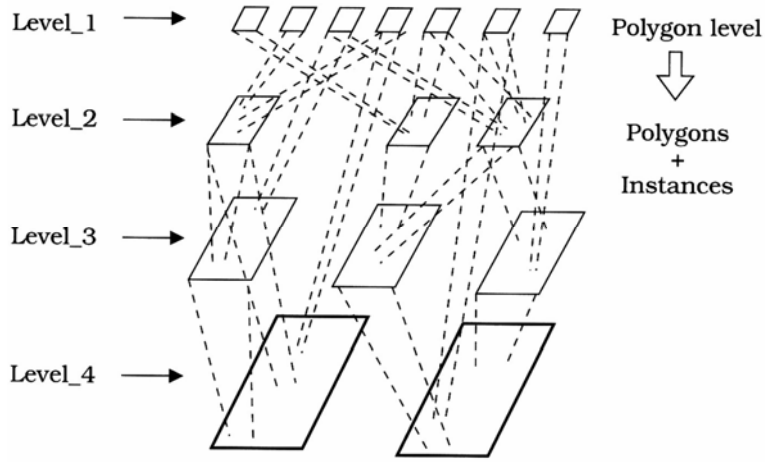


Figure 5.50 Cell hierarchy

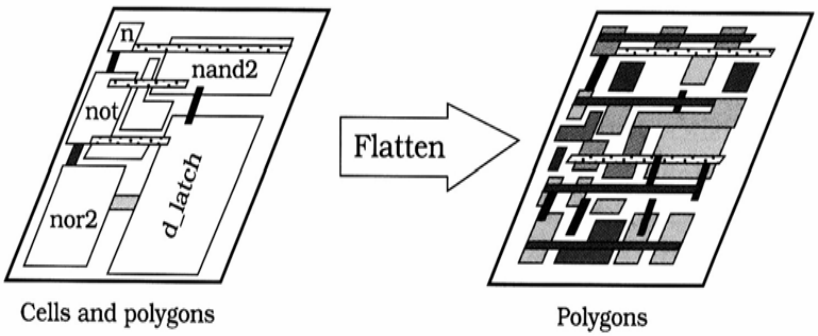


Figure 5.51 Effect of the flatten operation