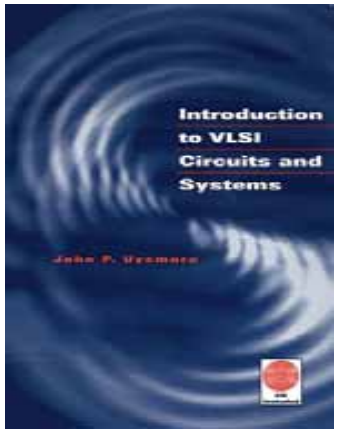
國立勤益科技大學
National Chin-Yi University of Technology

Introduction to VLSI Circuits and Systems
積體電路概論

Chapter 07
Electronic Analysis of CMOS Logic Gates



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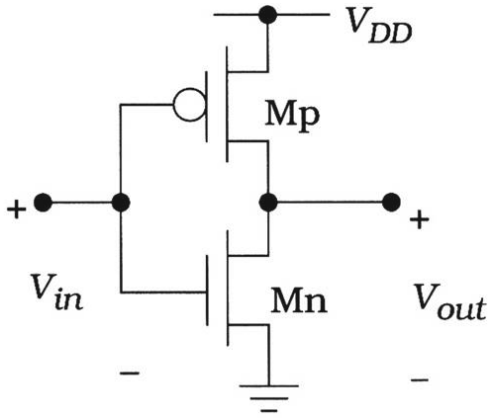
Fall 2007

Outline

- DC Characteristic of the CMOS Inverter
- Inverter Switching Characteristic
- Power Dissipation
- DC Characteristic: NAND and NOR Gates
- NAND and NOR Transient Response
- Analysis of Complex Logic Gates
- Gate Design for Transient Performance
- Transmission Gates and Pass Transistors

The Inverter Circuit

- The CMOS inverter gives the basic for calculating the electrical characteristic of logic gates
  - The conduction states of M_n and M_p is determined by input voltage V_{in}
  - Two types of calculations: *DC analysis* and *transient analysis*
- DC analysis
  - Provide a direct mapping of the input to the output, such that to determine V_{out}
- Transient analysis
  - The input voltage is an explicit function of time $V_{in}(t)$ corresponding to a changing logic value



pFET: $V_{Tp} < 0$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

nFET: $V_{Tn} > 0$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

Figure 7.1 The CMOS inverter circuit

DC Analysis of Inverter

- The DC characteristics of the inverter are portrayed in the *voltage transfer characteristic* (VTC), which is a plot of V_{out} as a function of V_{in}
  - » Simply, the output high voltage of the circuits as

$$V_{OH} = V_{DD} \quad (7.1) \quad (V_{in} = 0)$$

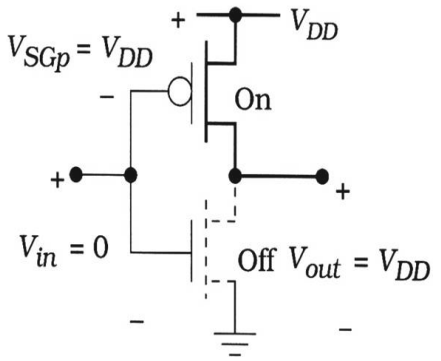
  - » The output low voltage

$$V_{OL} = 0\,V \quad (7.2) \quad (V_{in} = V_{DD})$$

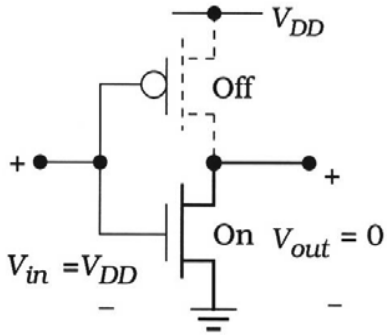
  - » The logic swing at the output is

$$V_L = V_{OH} - V_{OL} = V_{DD} \quad (7.3) \quad \text{(full-rail output)}$$

- Since this is equal to the full value of the power supply, this is called a *full-rail output*



(a) Low input voltage



(b) High input voltage

Figure 7.2 V_{OH} and V_{OL} for the inverter

VTC of the Inverter

- Starting with an input voltage of V_{in} = 0V and then increasing it up to a value of $V_{in} = V_{DD}$

$$V_{GSn} = V_{in}$$
$$V_{SGp} = V_{DD} - V_{in} \qquad (7.4)$$

  - » M_p goes into cutoff when

$$V_{in} = V_{DD} - |V_{Tp}| \qquad (7.5)$$

  - » The logic 0 and 1 voltage ranges are defined by the changing slope of the VTC
    - A logic 0 input voltage (input low voltage)

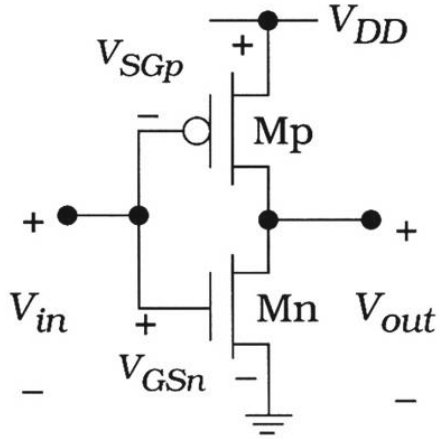
$$0 \le V_{in} \le V_{IL} \qquad (7.6)$$

    - A logic 1 input voltage (input high voltage)

$$V_{IH} \le V_{in} \le V_{DD} \qquad (7.7)$$

  - » The *voltage noise margins* give a quantitative measure of how stable the inputs are with respect to coupled electromagnetic signal interface, there are

$$VNM_H = V_{OH} - V_{IH}$$
$$VNM_L = V_{IL} - V_{OL} \qquad (7.8)$$



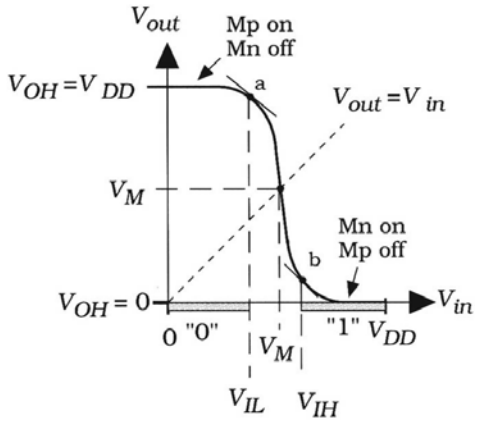
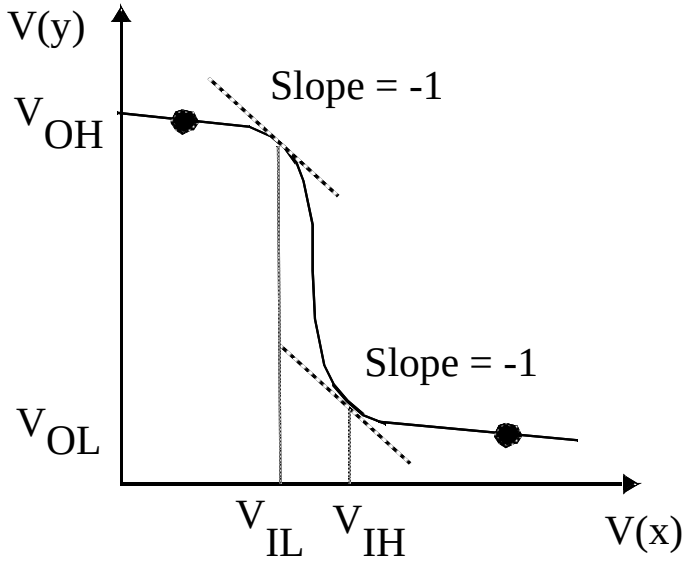
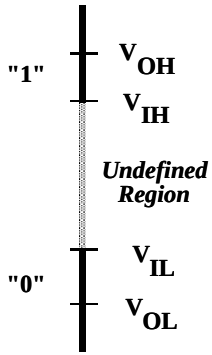


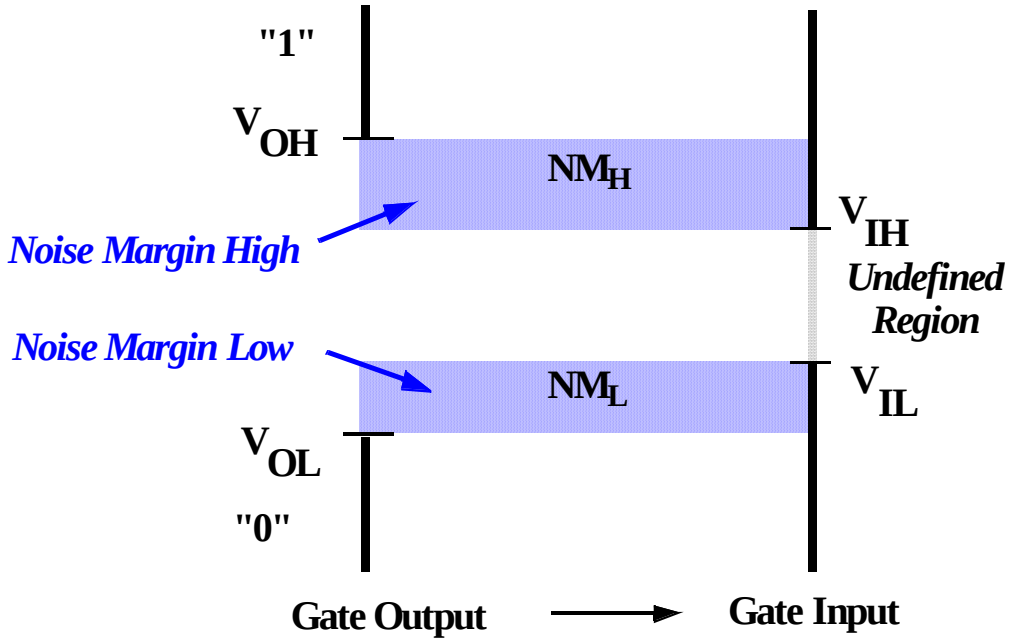
Figure 7.3 Voltage transfer curve for the NOT gate

Definition of Noise Margins





$$VNM_H = V_{OH} - V_{IH}$$
$$VNM_L = V_{IL} - V_{OL} \qquad (7.8)$$



Midpoint Voltage V_M

$$I_{Dn} = I_{Dp} \quad (Let\ V_{in} = V_{out} = V_M) \qquad (7.9)$$

$$V_{sat} = V_{GSn} - V_{Tn} = V_M - V_{Tn} \qquad (7.10)$$

$$V_{DSn} > V_{sat} = V_M - V_{Tn} \qquad (7.11)$$

$$\frac{\beta_n}{2}(V_{M-}V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2 \qquad (7.12)$$

$$\sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{Tn}) = V_{DD} - V_M - |V_{Tp}| \qquad (7.13)$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \qquad (7.14)$$

$$\frac{\beta_n}{\beta_p} = \frac{\kappa'_n \left(\frac{W}{L}\right)_n}{\kappa'_p \left(\frac{W}{L}\right)_p} \qquad (7.15)$$

$$\frac{\kappa'_n}{\kappa'_p} \approx 2\ to\ 3 \qquad (7.16)$$

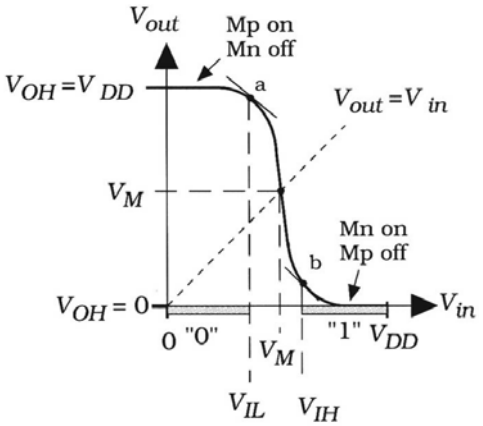
$$\frac{\kappa'_n}{\kappa'_p} = \frac{\mu_n}{\mu_p} = \gamma \qquad (7.17)$$

Symmetrical inverter principle

$$V_M = \frac{1}{2}V_{DD} \qquad (7.18)$$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{1}{2}V_{DD} - |V_{Tp}|}{\frac{1}{2}V_{DD} - V_{Tn}}\right)^2 \qquad (7.19)$$

$$\beta_n = \beta_p \qquad (7.20)$$



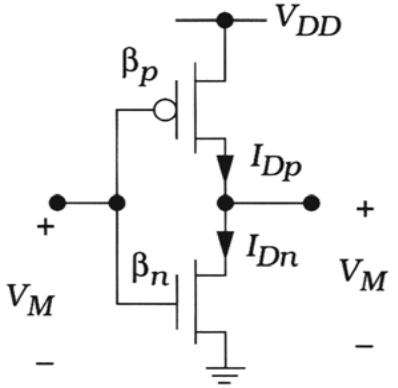
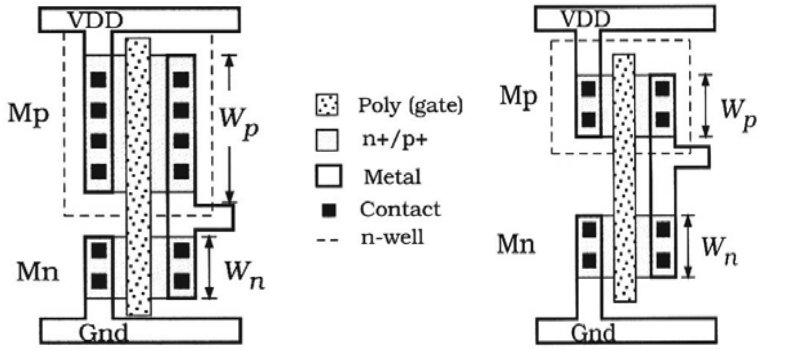


Figure 7.4 Inverter voltage for V_M calculation

VTC Variation

- In Figure 7.5(a), the pFET has a width of about $W_p \quad 2W_n$
  - » $V_M = (V_{DD}/2)$
- In Figure 7.5(b), the pFET has a width of about $W_p \quad W_n$
  - » $V_M < (V_{DD}/2)$
- At the physical level, the relative device sizes contained in the ratio (β_n/β_p) determine the switching points



(a) Large pFET design (b) Equal aspect ratios

Figure 7.5 Comparison of the layouts

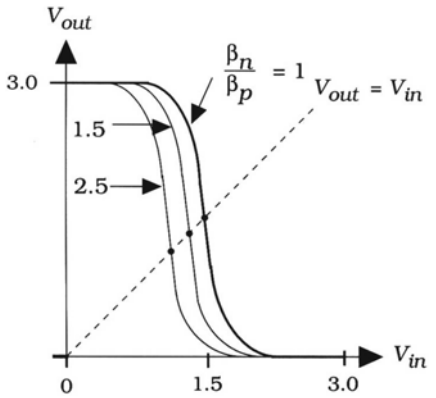


Figure 7.6 Dependence of VM on the device ratio

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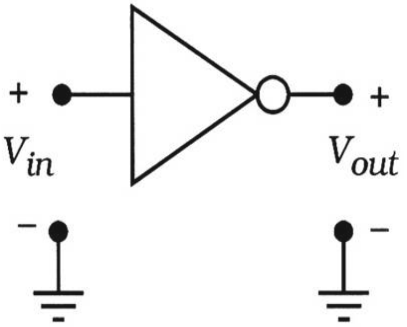
Switching Characteristic

- High-speed digital system design requires that logic gates introduce a minimum amount of time delay when the inputs change
  - » The output 1-to-0 transition introduces a *fall time* delay of t_f
  - » The output 0-to-1 transition introduces a *rise time* delay of t_r
- The rise time and fall time can be calculated by analyzing the electronic transitions of the circuits
  - » parasitic resistance
  - » parasitic capacitances of the transistors



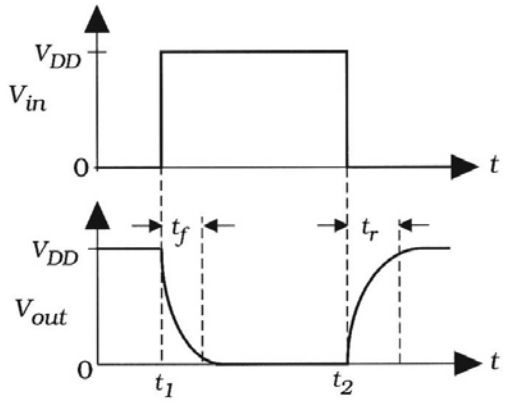


Figure 7.7 General switching waveforms

RC Model of Inverter

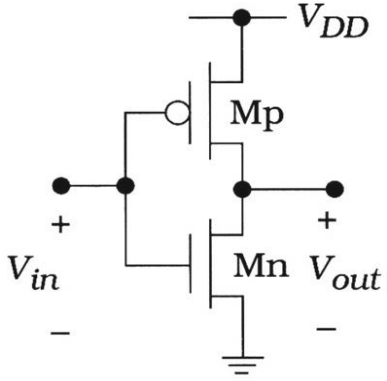
- Both FETs can be replaced by their switch equivalents, which results in the simplified RC model
  - » Given the aspect ratios $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$
$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)} \qquad (7.28)$$

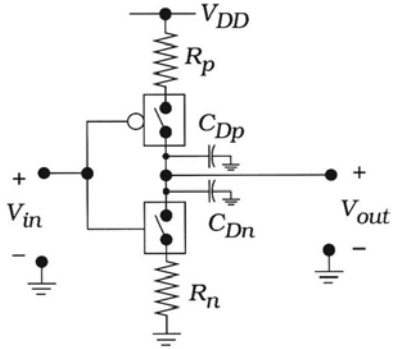
  - » Finding the capacitance C_{Dn} and C_{Dp} at the output node

$$C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2} C_{ox} L' W_n + C_{jn} A_n + C_{jswn} P_n$$
$$C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2} C_{ox} L' W_p + C_{jp} A_{pp} + C_{jswp} P_p \qquad (7.29)$$

- It is significant that increasing the channel width of a FET increases the parasitic capacitance values



(a) FET circuit



(b) RC switch model equivalent

Figure 7.8 RC switch model equivalent for the CMOS inverter

Fan-out (FO)

- The fan-out gates act as a *load* to the driving circuit because of their *input capacitance* C_{in}
  - » Therefore, the total input capacitance is (Figure 7.9(a))

$$C_{in} = C_{Gp} + C_{Gn} \qquad (7.30)$$

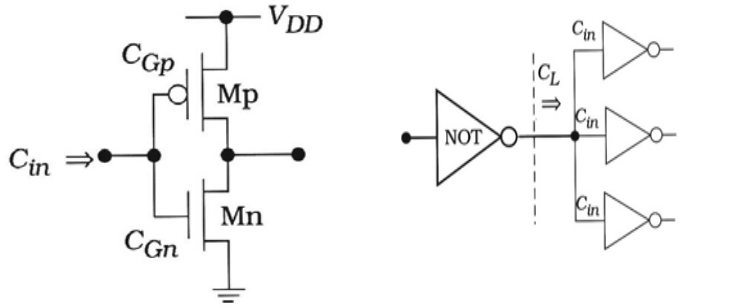
  - » In Figure 7.9(b), the external load capacitance C_L is

$$C_L = 3C_{in} \qquad (7.31)$$

- In Figure 7.10 where the total output capacitance is defined as

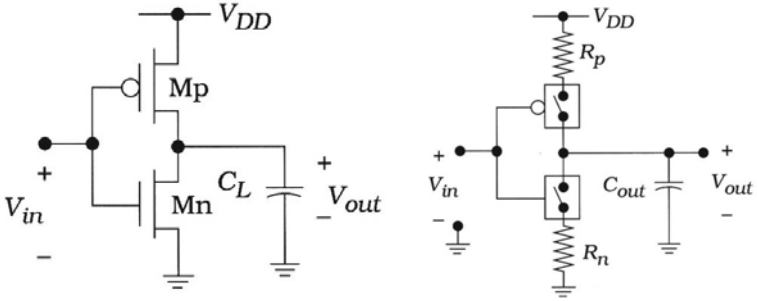
$$C_{out} = C_{FET} + C_L \qquad (7.32)$$

$$C_{FET} = C_{Dn} + C_{Dp} \qquad (7.33)$$



(a) Single stage (b) Loading due to fan-out

Figure 7.9 Input capacitance and load effects



(a) External load (b) Complete switch model

Figure 7.10 Evolution of the inverter switching model

Fall Time Calculation

- Initially, $V_{out}(0) = V_{DD}$, and $V_{in} = 0$ V and is switched to $V_{in} = V_{DD}$ at time $t = 0$; we time shift this event to occur at $t = 0$
  - » The current leaving the capacitor is

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n} \qquad (7.42)$$

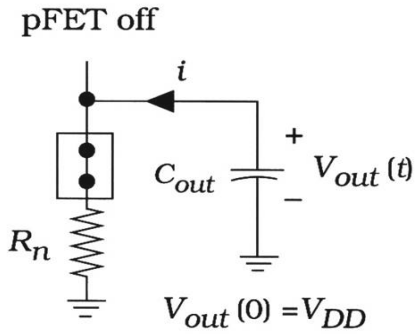
  - » The differential equation for the discharge events

$$V_{out}(t) = V_{DD}e^{-\frac{t}{\tau_n}},\ where\ \tau_n = R_nC_{out} \qquad (7.43, 44)$$

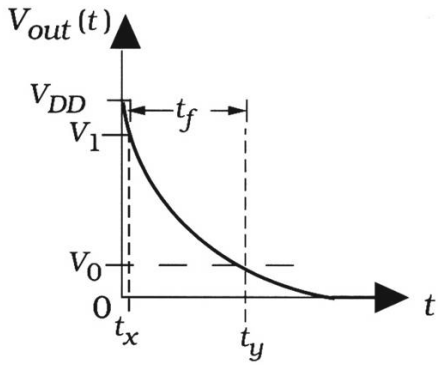
$$\Rightarrow t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right) \qquad (7.45)$$

$$t_f = t_y - t_x$$
$$= \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right) \qquad (7.46)$$
$$= \tau_n \ln(9)$$

$$\Rightarrow t_f \approx 2.2\tau_n \quad (t_{HL} = t_f) \qquad (7.48, 49)$$



(a) Discharge circuit



(b) Output waveform

Figure 7.12 Discharge circuit for the fall time calculation

The Rise Time

- Initially, $V_{out}(0) = 0$ V, and $V_{in} = V_{DD}$ and is switched to $V_{in} = 0$ V at $t = 0$; we time shift this event to occur at $t = 0$
  - The charge current is given by

$$i = C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p} \qquad (7.50)$$

  - The differential equation for the charge events

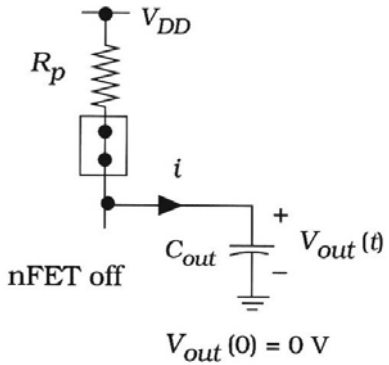
$$V_{out}(t) = V_{DD}\left[1 - e^{-\frac{t}{\tau_p}}\right], \text{ where } \tau_p = R_p C_{out} \qquad (7.51, 52)$$

$$t_r = t_v - t_u \qquad (7.53)$$

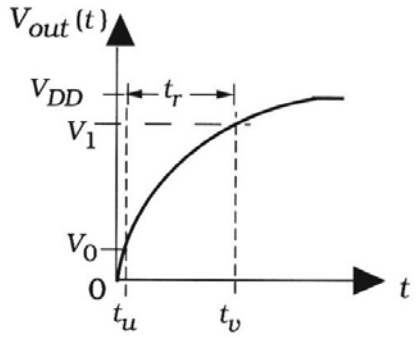
$$\Rightarrow t_r = \ln(9)\tau_p \approx 2.2\tau_p \qquad (7.54)$$

$$\Rightarrow f_{\max} = \frac{1}{t_{HL} + t_{LH}} = \frac{1}{t_r + t_f} \qquad (7.55)$$

- f_{max} is the largest frequency that can be applied to the gate and still allow the output to settle to a definable state



(a) Charge circuit



(b) Output waveform

Figure 7.13 Rise time calculation

Propagation Delay (1/2)

- The propagation delay time t_p is often used to estimate the "reaction" delay time from input to output

$$t_p = \frac{(t_{pf} + t_{pr})}{2} \qquad (7.64)$$

  - » t_{pf} is the output fall time from the maximum level to the "50%" voltage line, i.e., from V_{DD} to (V_{DD}/2)

$$t_{pf} = \ln(2)\tau_n \qquad (7.65)$$

  - » t_{pr} is the propagation rise time from 0 V to (V_{DD}/2)

$$t_{pr} = \ln(2)\tau_p \qquad (7.65)$$

$$\Rightarrow t_p \approx 0.35(\tau_n + \tau_p) \qquad (7.66)$$

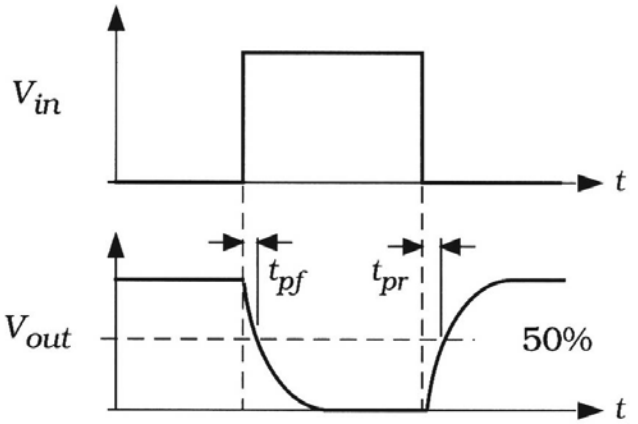


Figure 7.14 Propagation time definitions

- Commonly used in basic logic simulation programs because does not provide detailed information on the rise and fall times as individual quantities

Propagation Delay (2/2)

- The rise and fall time equations provide the basic for high-speed CMOS design

$$C_{out} = C_{FET} + C_L \tag{7.67}$$

$$\Rightarrow t_r \approx 2.2R_p(C_{FET} + C_L) \tag{7.68}$$
$$\Rightarrow t_f \approx 2.2R_n(C_{FET} + C_L)$$

$$\Rightarrow t_r = t_{r0} + \alpha_p C_L \tag{7.69}$$
$$\Rightarrow t_f = t_{f0} + \alpha_n C_L$$

Case I: When $C_L = 0$,

$$t_r = t_{r0} \approx 2.2R_p C_{FET} \tag{7.70}$$
$$t_f = t_{f0} \approx 2.2R_n C_{FET}$$

Case II: When $C_L \neq 0$,

$$\alpha_p = 2.2R_p = \frac{2.2}{\beta_p(V_{DD} - |V_{Tp}|)} \tag{7.71}$$

$$\alpha_n = 2.2R_n = \frac{2.2}{\beta_n(V_{DD} - V_{Tn})} \tag{7.72}$$

$$\beta_p = \kappa_p' \left(\frac{W}{L}\right)_p$$

$$\beta_n = \kappa_n' \left(\frac{W}{L}\right)_n \tag{7.73}$$

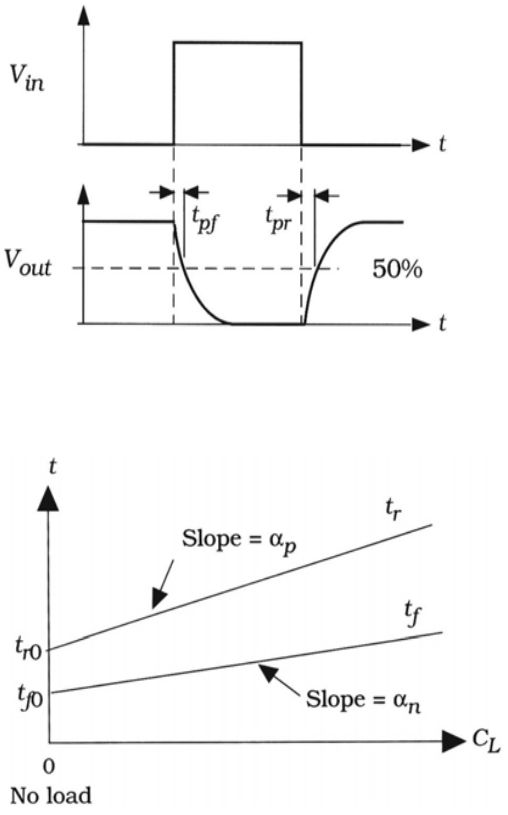
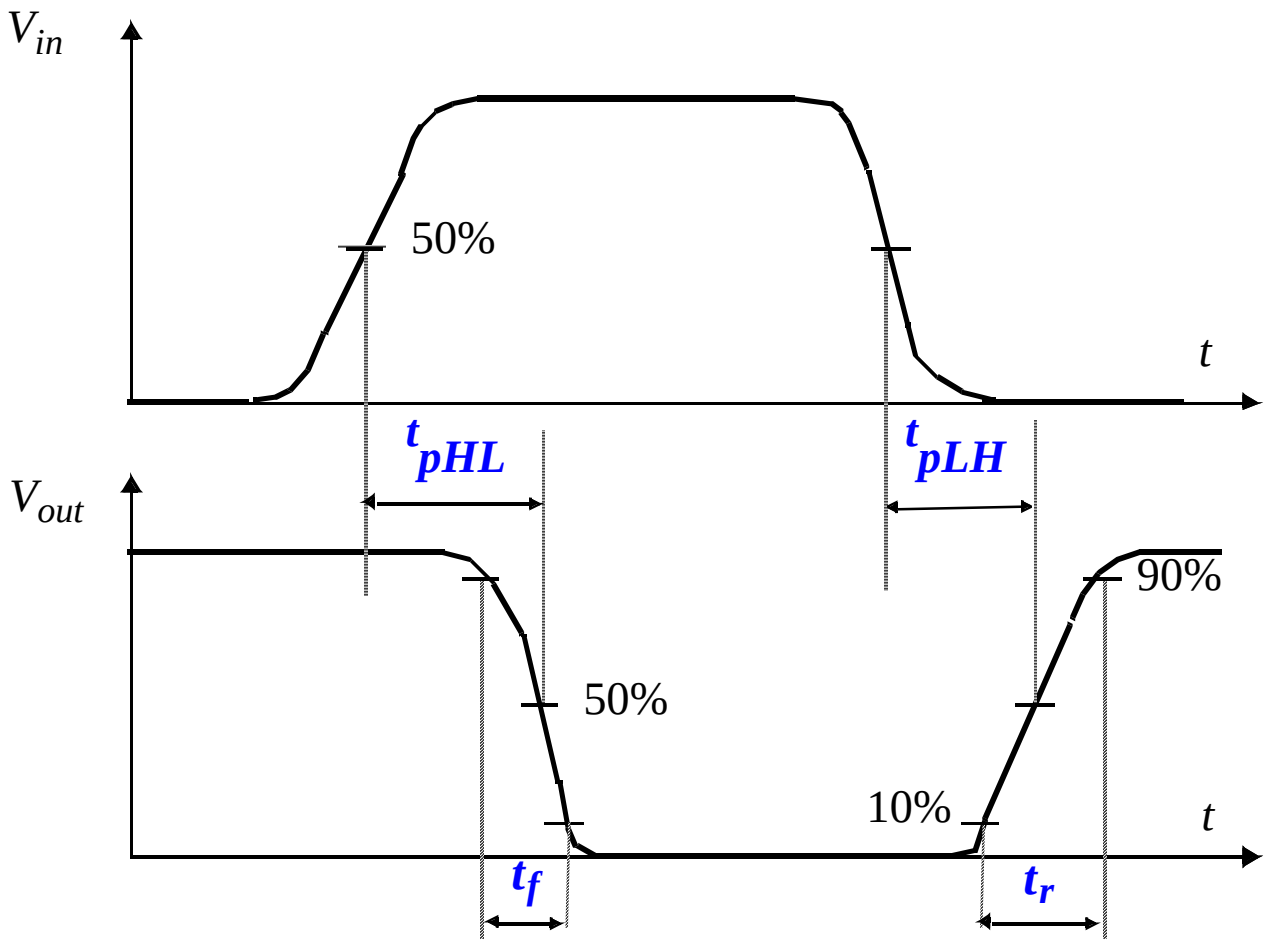


Figure 7.15 General behavior of the rise and fall time

Delay Definitions



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Power Dissipation (1/2)

- The current I_{DD} flowing from the power supply to ground gives a dissipated power of

$$P = V_{DD} I_{DD} \qquad (7.85)$$

  - Since V_{DD} is assumed to be a constant

$$P = P_{DC} + P_{dyn} \qquad (7.86)$$

    Where P_{DC} is the DC term and P_{dyn} is due to dynamic switching events

  - DC contribution

$$P_{DC} = V_{DD} I_{DDQ} \qquad (7.87)$$

    Where I_{DDQ} is leakage current

- Leakage current is very small, therefore, the value of P_{DC} is thus quite small
  - However, leakage power on today is critical for low-power Design

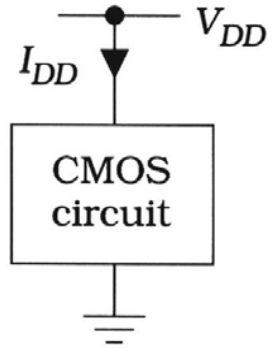
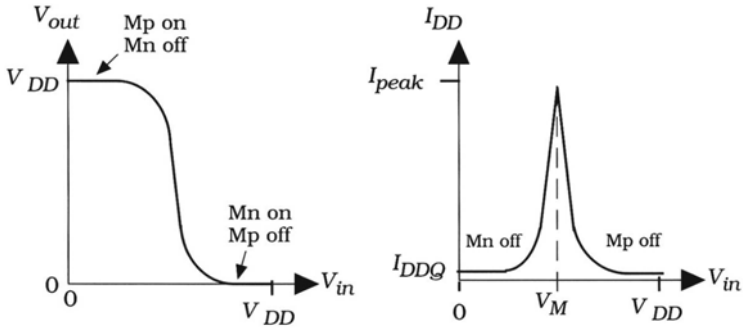


Figure 7.16 Origin of power dissipation calculation



(a) VTC (b) DC current

Figure 7.17 DC current flow

Power Dissipation (2 / 2)

- Dynamic power dissipation P_{dyn}

$$f = \frac{1}{T} \qquad (7.88)$$

  - » P_{dyn} arises from the observation that a complete cycle effectively creates a path for current to flow from the power supply to ground

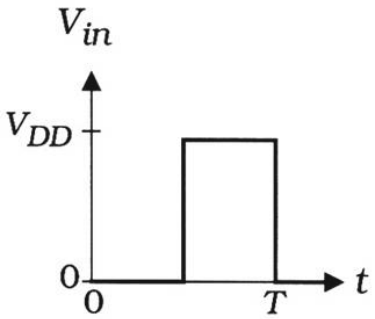
$$Q_e = C_{out} V_{DD} \qquad (7.89)$$

  - » The average power dissipation over a single cycle with a period T is

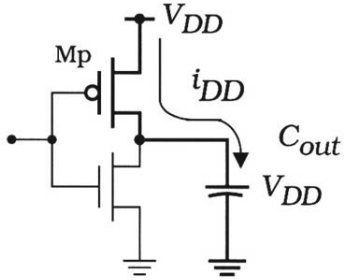
$$P_{av} = V_{DD} I_{DD} = V_{DD}\left(\frac{Q_e}{T}\right) \qquad (7.90)$$

$$\Rightarrow P_{sw} = C_{out} V_{DD}{}^2 f \qquad (7.91)$$

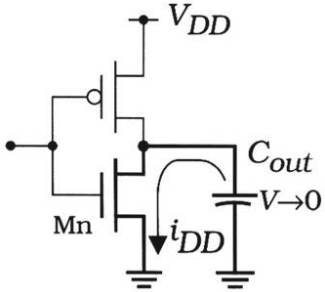
$$P = \underbrace{V_{DD} I_{DDQ}}_{\text{DC term}} + \underbrace{C_{out} V^2{}_{DD} f}_{\text{dynamic power term}} \qquad (7.92)$$



(a) Input voltage



(b) Charge



(c) Discharge

Figure 7.18 Circuit for finding the transient power dissipation

Outline

- DC Characteristic of the CMOS Inverter
- Inverter Switching Characteristic
- Power Dissipation
- DC Characteristic: NAND and NOR Gates
- NAND and NOR Transient Response
- Analysis of Complex Logic Gates
- Gate Design for Transient Performance
- Transmission Gates and Pass Transistors

NAND Analysis (1 / 2)

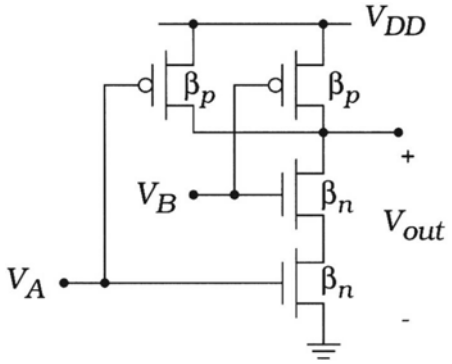


Figure 7.19 NAND2 logic circuit

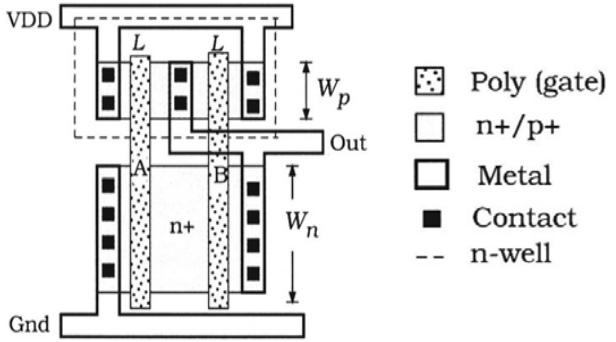
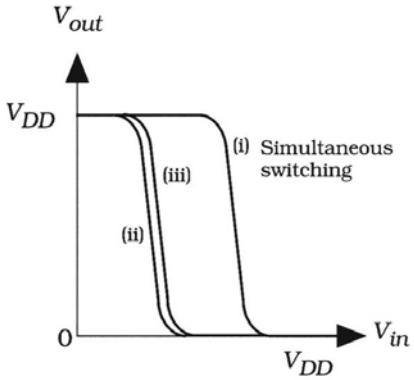


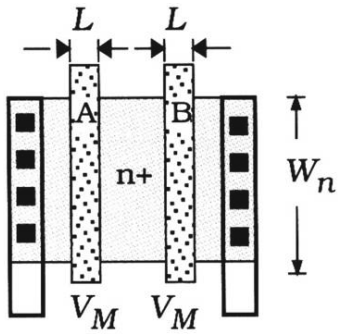
Figure 7.21 Layout of NAND2 for V_M calculation

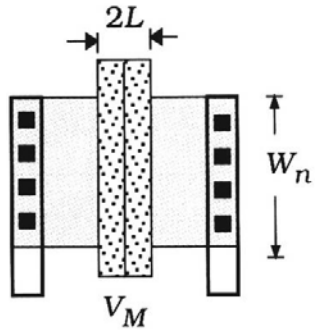
	V_A	V_B	V_{out}
(i)	0	0	V_{DD}
(ii)	0	V_{DD}	V_{DD}
(iii)	V_{DD}	0	V_{DD}
	V_{DD}	V_{DD}	0



(a) Transition table (b) VTC family

Figure 7.20 NAND 2 VTC analysis





(a) Separate transistors (b) Single equivalent FET

Figure 7.22 Simplification of the series-connected nFETs

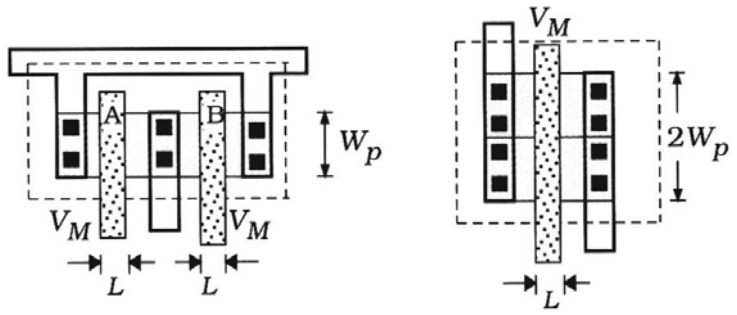
NAND Analysis (2 / 2)

- Find V_M for the case of simultaneous switching, where the nFET and pFET transconductance are ($\beta_n/2$) and 2 β_p

$$\frac{(\beta_n/2)}{2}(V_M - V_{Tn})^2 = \frac{(2\beta_p)}{2}(V_{DD} - V_M - |V_{Tp}|)^2 \qquad (7.93)$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (7.94)$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (7.95)$$



(a) Separate transistors (b) Single equivalent FET

Figure 7.23 Simplification of the series-connected nFETs

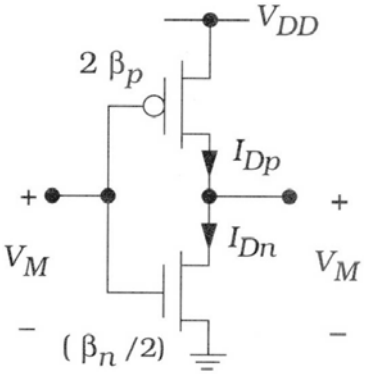


Figure 7.24 Simplified VM circuit for the NAND2 gate

NOR Analysis

$$\frac{(2\beta_n)}{2}(V_M - V_{Tn})^2 = \frac{(\beta_p/2)}{2}(V_{DD} - V_M - |V_{Tp}|)^2 \qquad (7.96)$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + 2\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + 2\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (7.97)$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + N\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + N\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (7.98)$$

$$P_{DC} = V_{DD} I_{DDQ} \qquad (7.99)$$

$$P_{sw} = C_{out} V_{DD}^{\ 2} f_{gate} \qquad (7.100)$$

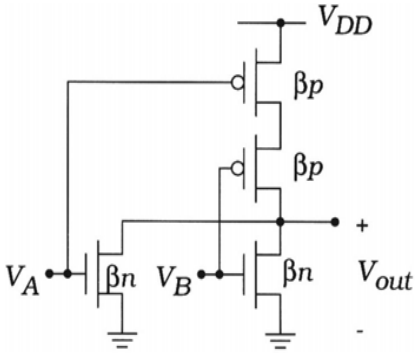


Figure 7.25 NOR2 circuit

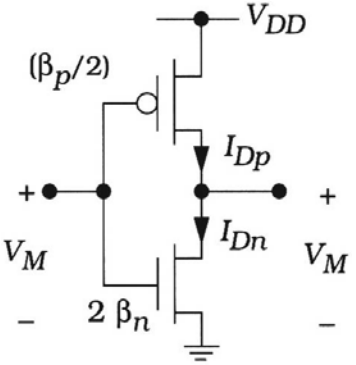
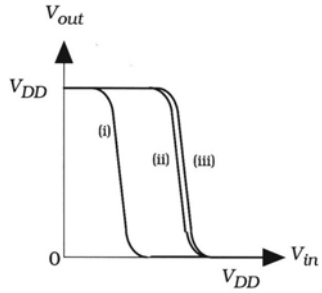


Figure 7.27 NOR23 VM calculation

	V_A	V_B	V_{out}
	0	0	V_{DD}
(iii)	0	V_{DD}	0
(ii)	V_{DD}	0	0
(i)	V_{DD}	V_{DD}	0

(a) Transition table



(b) VTC family

Figure 7.26 NOR 2 VTC analysis

Outline

- DC Characteristic of the CMOS Inverter
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- Gate Design for Transient Performance
- Transmission Gates and Pass Transistors

NAND Switching Times (1/2)

- Figure 7.28

$$C_{out} = C_{FET} + C_L \qquad (7.101)$$

$$C_{FET} = C_{Dn} + 2C_{Dp} \qquad (7.102)$$

$$R_P = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}, \quad R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} \qquad (7.103)$$

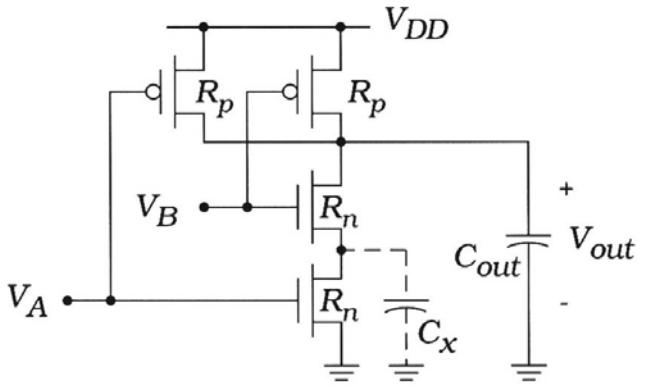


Figure 7.28 NAND2 circuit for transient calculations

- Figure 7.29 (a)

$$V_{out}(t) = V_{DD}[1 - e^{-t/\tau_p}] \qquad (7.104)$$

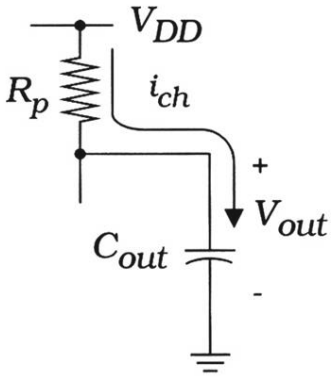
$$where\ \tau_p = R_p C_{out} \qquad (7.105)$$

$$t_r \approx 2.2\tau_p \qquad (7.106)$$

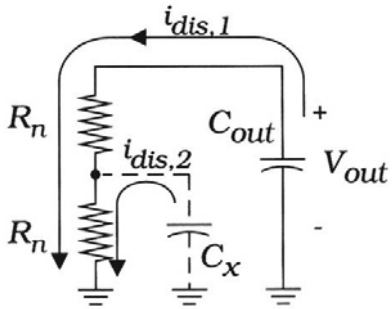
$$t_r = t_0 + \alpha_0 C_L \qquad (7.107)$$

$$t_0 = 2.2 R_p C_{FET} \qquad (7.108)$$

$$\alpha_0 = 2.2 R_p \qquad (7.109)$$



(a) Charge circuit



(b) Discharge circuit

Figure 7.29 NAND2 subcircuits for estimating rise and fall times

NAND Switching Times (2/2)

$$V_{out}(t) = V_{DD} e^{-t/\tau_n} \quad (7.110)$$

$$\tau_n = C_{out}(R_n + R_n) + C_X R_n \quad (7.111)$$

$$\tau_n = \tau_{n1} + \tau_{n2} \quad (7.112)$$

$$\text{where } \tau_{n1} = C_{out}(R_n + R_n) \quad (7.113)$$

$$\tau_{n2} = C_X R_n \quad (7.114)$$

$$t_f \approx 2.2\tau_n \quad (7.115)$$

$$t_f \approx 2.2[(C_{FET} + C_L)(2R_n) + C_X R_n] \quad (7.116)$$

$$t_f = t_1 + \alpha_1 C_L \quad (7.117)$$

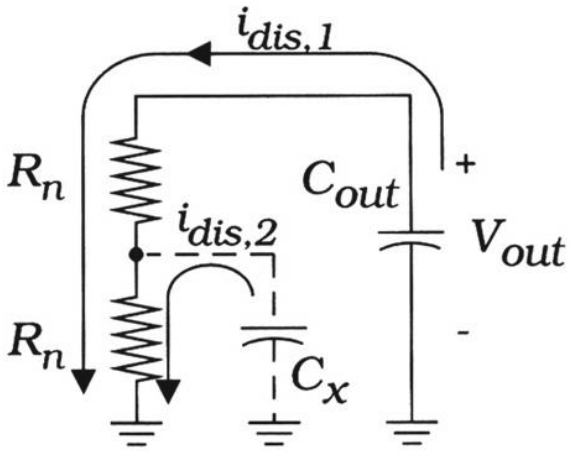
$$t_1 = 2.2R_n(2C_{FET} + C_X) \quad (7.118)$$

$$\alpha_1 = 4.4R_n \quad (7.119)$$

$$\tau_n = R_n(2C_{out} + C_X) \quad (7.120 \textit{ from } 7.111)$$

$$C_{eff} = 2C_{out} + C_X \quad (7.121)$$

$$\tau_n = C_{out}(2R_n) + C_X R_n \quad (7.122)$$



(b) Discharge circuit

NOR Switching Times (1 / 2)

- Figure 7.30

$$C_{out} = C_{FET} + C_L \qquad (7.123)$$

$$C_{FET} = 2C_{Dn} + C_{Dp} \qquad (7.124)$$

- Figure 7.31 (a)

$$V_{out}(t) = V_{DD} e^{-t/\tau_n} \qquad (7.125)$$

$$\tau_n = R_n C_{out} \qquad (7.126)$$

$$t_f \approx 2.2\tau_n \qquad (7.127)$$

$$t_f = t_1 + \alpha_1 C_L \qquad (7.128)$$

$$t_1 = 2.2 R_n C_{FET} \qquad (7.129)$$

$$\alpha_1 = 2.2 R_n \qquad (7.130)$$

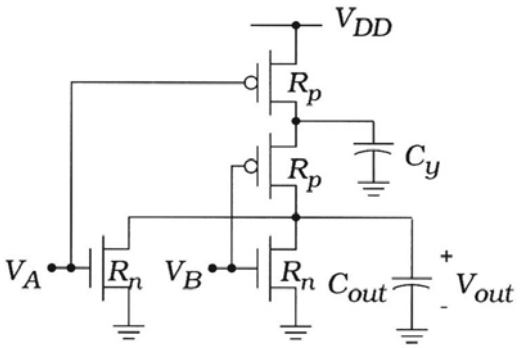
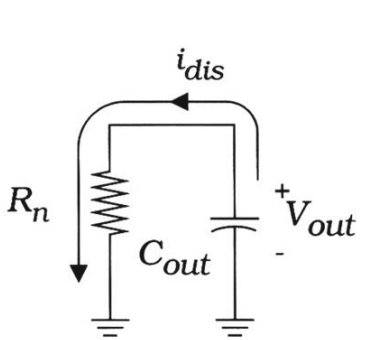
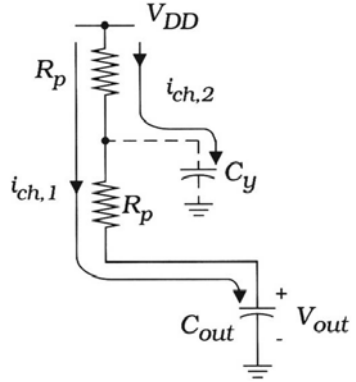


Figure 7.30 NOR2 circuit for switch time calculations



(a) Discharge circuit



(b) Charge circuit

Figure 7.31 Subcircuits for the NOR2 transient calculations

NOR Switching Times (2 / 2)

- Figure 7.31 (b)

$$V_{out}(t) = V_{DD}[1 - e^{-t/\tau_p}] \quad (7.131)$$

$$\tau_1 = C_{out}(R_p + R_p) \quad (7.132)$$

$$\tau_2 = C_y R_p \quad (7.133)$$

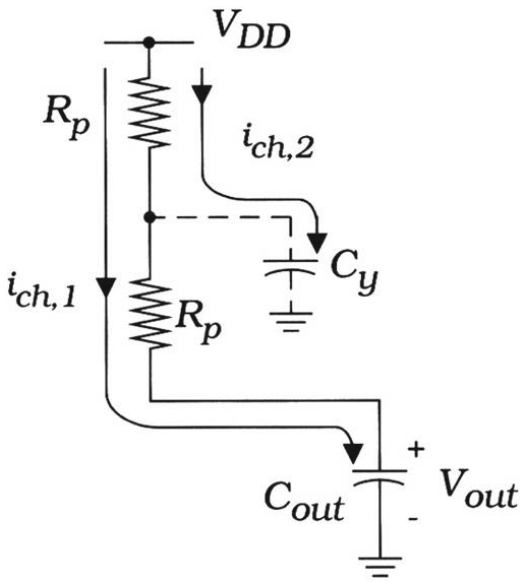
$$\tau_p = \tau_1 + \tau_2 = C_{out}(2R_p) + C_y R_p \quad (7.134)$$

$$t_r = 2.2\tau_p \quad (7.135)$$

$$t_r = t_0 + \alpha_0 C_L \quad (7.136)$$

$$where\ t_0 = 2.2R_p(2C_{FET} + C_y) \quad (7.137)$$

$$\alpha_0 = 4.4R_p \quad (7.138)$$



(b) Charge circuit

Outline

- DC Characteristic of the CMOS Inverter
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- Power Dissipation
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- Transmission Gates and Pass Transistors

Analysis of Complex Logic Gates

$$f = \overline{x \cdot (y + z)} \qquad (7.141)$$

$$\left(\frac{W}{L}\right)_{nx} = \left(\frac{W}{L}\right)_{ny} = \left(\frac{W}{L}\right)_{nz} \qquad (7.142)$$

$$C_{out} = C_{FET} + C_L \qquad (7.143)$$

$$\tau_n = R_n C_n + 2R_n C_{out} \qquad (7.144)$$

$$\begin{aligned} t_f &= 2.2\tau_n \\ &= 2.2R_n[C_n + 2(C_{FET} + C_L)] \\ &= t_1 + \alpha_1 C_L \end{aligned} \qquad (7.145)$$

$$where\ t_1 = 2.2R_n(C_n + 2C_{FET}) \qquad (7.146)$$

$$\alpha_1 = 2.2R_n \qquad (7.147)$$

$$\left(\frac{W}{L}\right)_{px} = \left(\frac{W}{L}\right)_{py} = \left(\frac{W}{L}\right)_{pz} \qquad (7.148)$$

$$\tau_p = R_p C_p + 2R_p C_{out} \qquad (7.149)$$

$$t_r = t_0 + \alpha_0 C_L \qquad (7.150)$$

$$t_0 = 2.2R_p(C_p + 2C_{FET}) \qquad (7.151)$$

$$\alpha_0 = 2.2R_p \qquad (7.152)$$

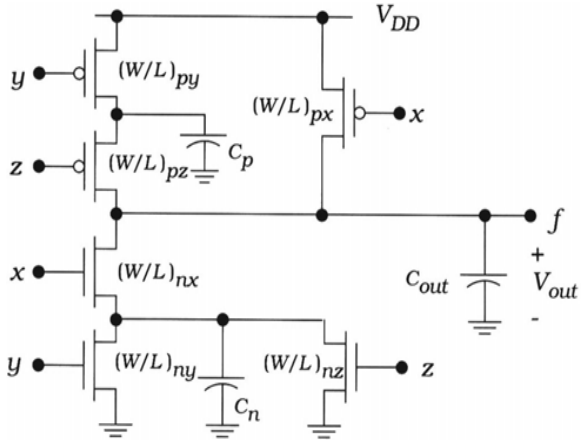

Figure 7.32 Complex logic gate circuit

Power Dissipation

- Power dissipation in a simple inverter

$$P = V_{DD} I_{DDQ} + C_{out} V_{DD}^{\ 2} f \qquad (7.153)$$

- We introduce the *activity coefficient a* that represents the probability that an output 0 → 1 transition takes place during one period

A	B	$\overline{A+B}$	$\overline{A \cdot B}$
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

Figure 7.33 Truth tables for determining activity coefficients

$$P_{dyn} = aC_{out} V_{DD}^{\ 2} f \qquad (7.154)$$

$$P_{dyn} = \sum_{i=1}^{N} a_i C_i V_i V_{DD} f \qquad (7.155)$$

$$a = p_0 p_1 \qquad (7.156)$$

$$a_{NOR2} = \left(\frac{3}{4}\right)\left(\frac{1}{4}\right) = \frac{3}{16} \qquad (7.157)$$

$$a_{NAND2} = \left(\frac{3}{4}\right)\left(\frac{1}{4}\right) = \frac{3}{16} \qquad (7.158)$$

$$a_{NOR3} = \frac{7}{64} = a_{NAND3} \qquad (7.159)$$

$$a_{XNOR2} = \frac{1}{4} = a_{XOR2} \qquad (7.160)$$

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Gate Design for Transient Performance (1 / 2)

$\beta = k'\left(\frac{W}{L}\right)$ (Inverter reference starting)

$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}, \quad R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$

$\beta_n = \beta_p$

$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$

where $r = \frac{k_n'}{k_p'}$

$\beta_P = \beta_p$ (NAND2 vs Inverter)

$R = R_N + R_N$

where $R_N = \frac{1}{\beta_N (V_{DD} - V_{Tn})}$

$R = R_n = 2R_N$

$\frac{1}{\beta_n (V_{DD} - V_{Tn})} = \frac{2}{\beta_N (V_{DD} - V_{Tn})}$

$\beta_N = 2\beta_n$

$\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n$

$\beta_N = \beta_n$ (NOR2 vs Inverter)

$\frac{1}{\beta_p (V_{DD} - |V_{Tp}|)} = \frac{2}{\beta_P (V_{DD} - |V_{Tp}|)}$

$\beta_P = 2\beta_p$

$\left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_p$

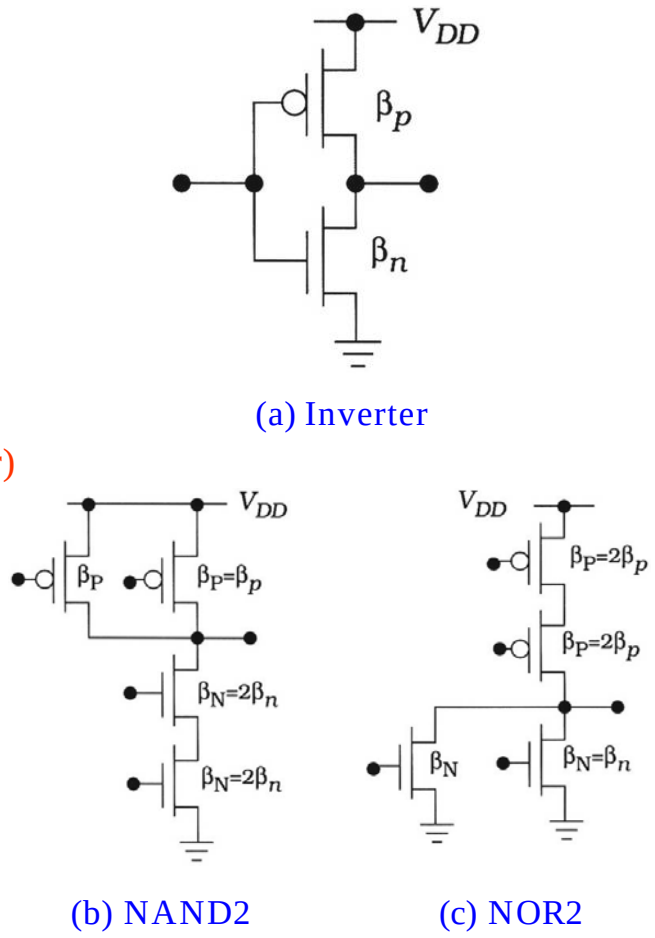


Figure 7.34 Relative FET sizing

Gate Design for Transient Performance (2 / 2)

- Extend to large chains as Figure 7.35

$$\beta_N = 3\beta_n,\ \beta_P = \beta_p \qquad (7.177)$$

$$\left(\frac{W}{L}\right)_N = 3\left(\frac{W}{L}\right)_n,\ \left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_p \qquad (7.178)$$

$$\beta_N = \beta_n,\ \beta_P = 3\beta_p \qquad (7.179)$$

$$\left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_n,\ \left(\frac{W}{L}\right)_P = 3\left(\frac{W}{L}\right)_p \qquad (7.180)$$

- Figure 7.36

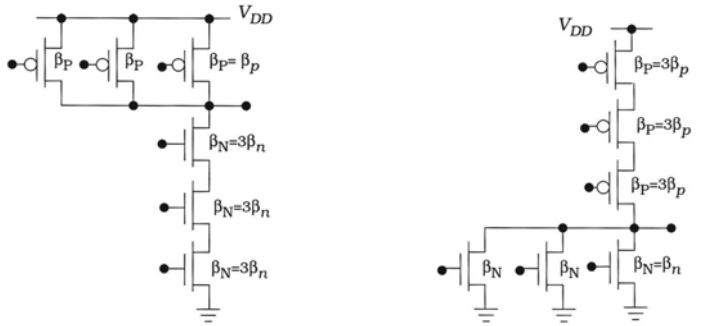
$$f = \overline{(a \cdot b + c \cdot d) \cdot x} \qquad (7.181)$$

$$\beta_N = 3\beta_n = \beta_{N1} \qquad (7.182)$$

$$\beta_P = 2\beta_p \qquad (7.183)$$

$$\beta_{P1} = \beta_p \qquad (7.184)$$

$$\beta_{P1} = \beta_P = 2\beta_P \qquad (7.185)$$



(a) NAND3 (b) NOR3

Figure 7.35 Sizing for 3-input gates

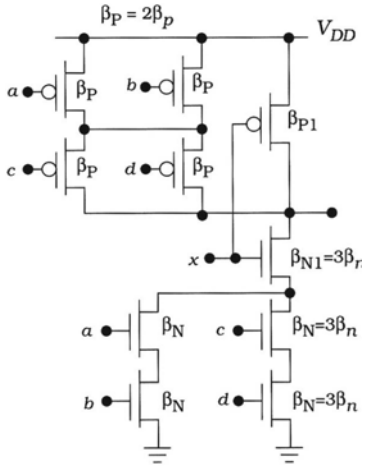


Figure 7.36 Sizing of a complex logic gate

Outline

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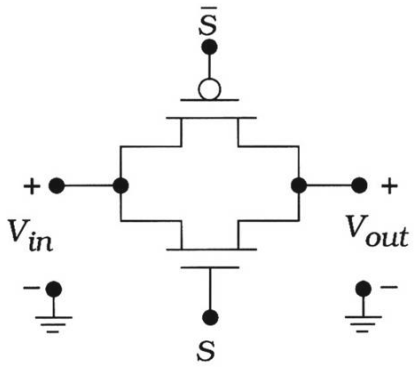
Transmission Gates

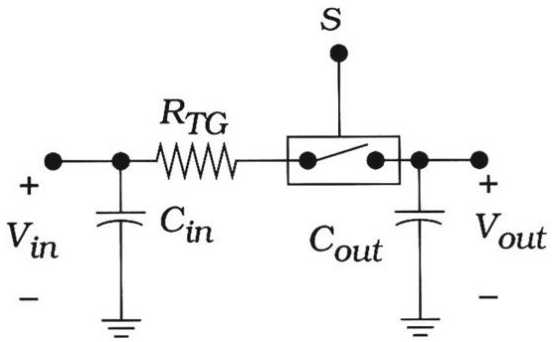
$$R_{TG} = \max(R_n, R_p) \qquad (7.186)$$

$$C_{in} = C_{S,n} + C_{D,p} \qquad (7.187)$$

- Large ratio of (W/L) decrease the resistance, but a large W implies large capacitances



(a) Circuit



(b) RC model

Figure 7.37 Transmission gate modeling

Pass Transistor

- Pass FETs can be used in place of transmission gates in most circuits
  - » Less area and wiring, but cannot pass the entire voltage range

$$V_{out}(t) = V_{\max}\left(\frac{t/2\tau_n}{1+t/2\tau_n}\right) \quad (7.188)$$

$$where\ V_{\max} = V_{DD} - V_{Tn} \quad (7.189)$$

$$\lim_{t\to\infty} V_{out}(t) = V_{\max} \quad (7.190)$$

$$\tau_n = R_n C_{out} \quad (7.191)$$

$$t_r = 18\tau_n \quad (7.192)$$

$$V_{out}(t) = V_{\max}\left(\frac{2e^{-(t/\tau_n)}}{1+e^{-(t/\tau_n)}}\right) \quad (7.193)$$

$$\lim_{t\to\infty} V_{out}(t) = 0 \quad (7.194)$$

$$t_f = \ln(19)\tau_n \approx 2.94\tau_n \quad (7.195)$$

$$t_r \approx 6t_f \quad (7.196)$$

$$t_r = 2.94\tau_p \quad (7.197)$$

$$where\ \tau_p = R_p C_{out} \quad (7.198)$$

$$V_{\min} = |V_{Tp}| \quad (7.199)$$

$$t_f = 18\tau_p \quad (7.200)$$

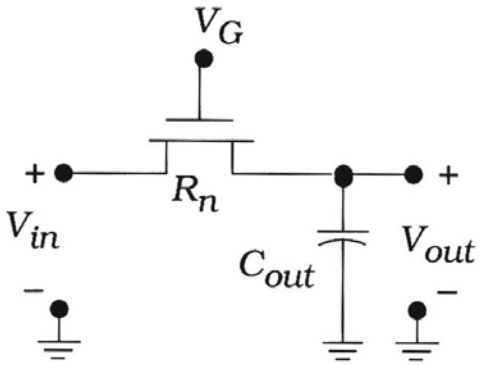


Figure 7.38 nFET pass transistor

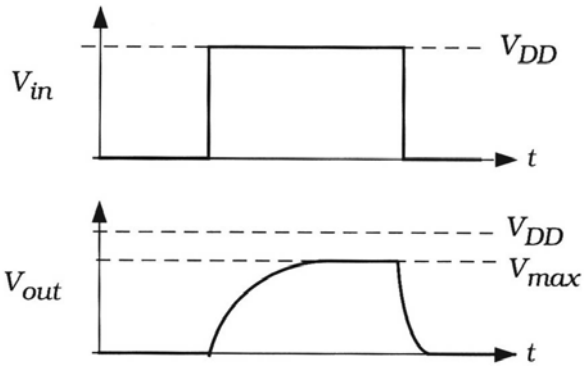


Figure 7.39 Voltage waveforms for a nFET pass transistor