Electrónica III TP1

August 20, 2018

1 Ejercicio 4

x_1	x_2	x_3	x_4	f_1	f_2	f_3	f_4
0	0	0	0	0	0	0	1
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Figure 1: Complemento a 2 de los bits de entrada

Si escribimos cada bit de salida en función de los mintérminos de los bits de entrada, nos quedan las siguientes ecuaciónes:

$$f_1(m_i) = m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8$$

$$f_2(m_i) = m_1 + m_2 + m_3 + m_4 + m_9 + m_{10} + m_{11} + m_{12}$$

$$f_3(m_i) = m_1 + m_2 + m_5 + m_6 + m_9 + m_{10} + m_{13} + m_{14}$$

$$f_4(m_i) = m_0 + m_1 + m_3 + m_5 + m_7 + m_9 + m_{11} + m_{13} + m_{15}$$

Remplazando los valores de cada mintermino, quedan las siguientes formulas:

$$f_1(x_1; x_2; x_3; x_4) =$$
$$\bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3\bar{x_4} + \bar{x_1}\bar{x_2}x_3x_4 + \bar{x_1}x_2\bar{x_3}\bar{x_4} + \bar{x_1}x_2\bar{x_3}x_4 + \bar{x_1}x_2x_3\bar{x_4} + \bar{x_1}x_2x_3x_4 + x_1\bar{x_2}\bar{x_3}\bar{x_4}$$

$$f_2(x_1; x_2; x_3; x_4) =$$
$$\bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3\bar{x_4} + \bar{x_1}\bar{x_2}x_3x_4 + \bar{x_1}x_2\bar{x_3}\bar{x_4} + x_1\bar{x_2}\bar{x_3}x_4 + x_1\bar{x_2}x_3\bar{x_4} + x_1\bar{x_2}x_3x_4 + x_1x_2\bar{x_3}\bar{x_4}$$

$$f_3(x_1; x_2; x_3; x_4) =$$
$$\bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3\bar{x_4} + \bar{x_1}x_2\bar{x_3}x_4 + \bar{x_1}x_2x_3\bar{x_4} + x_1\bar{x_2}\bar{x_3}x_4 + x_1\bar{x_2}x_3\bar{x_4} + x_1x_2\bar{x_3}x_4 + x_1x_2x_3\bar{x_4}$$

$$f_4(x_1; x_2; x_3; x_4) =$$
$$\bar{x_1}\bar{x_2}\bar{x_3}\bar{x_4} + \bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3x_4 + \bar{x_1}x_2\bar{x_3}x_4 + \bar{x_1}x_2x_3x_4 + x_1\bar{x_2}\bar{x_3}x_4 + x_1\bar{x_2}x_3x_4 + x_1x_2\bar{x_3}x_4 + x_1x_2x_3x_4$$

Si simplificamos cada ecuación, se puede llegar a las siguientes expresiones:

$$f_1(x_1; x_2; x_3; x_4) = x_1\bar{x_2}\bar{x_3}\bar{x_4} + \bar{x_1}(x_2 + x_3 + x_4)$$

$$f_2(x_1; x_2; x_3; x_4) = x_2\bar{x_3}\bar{x_4} + \bar{x_2}(x_3 + x_4)$$

$$f_3(x_1; x_2; x_3; x_4) = x_3\bar{x_4} + \bar{x_3}x_4$$

$$f_4(x_1; x_2; x_3; x_4) = x_4 + \bar{x_1}\bar{x_2}\bar{x_3}$$

Al intentar expresar dichas formulas en graficos de compuertas logicas, se consiguieron los siguientes:

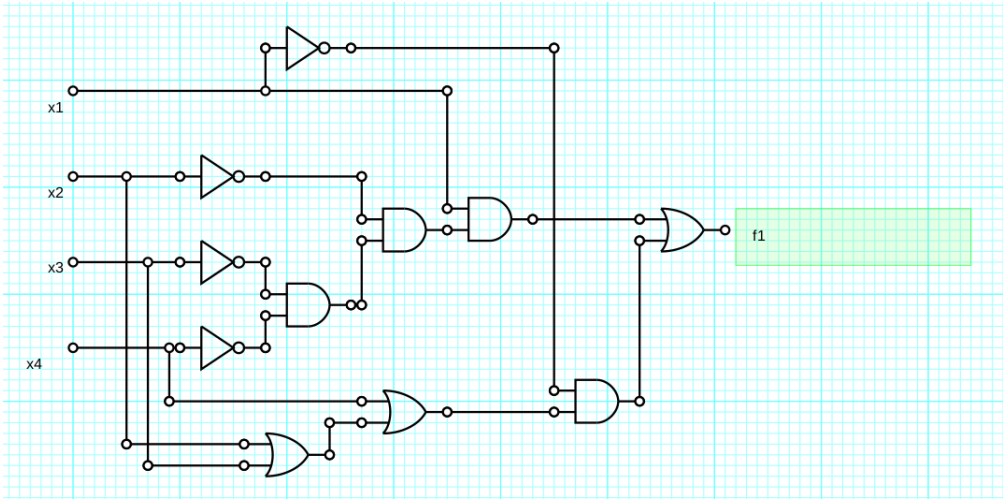

Figure 2: Grafico de compuertas logicas Bit 1

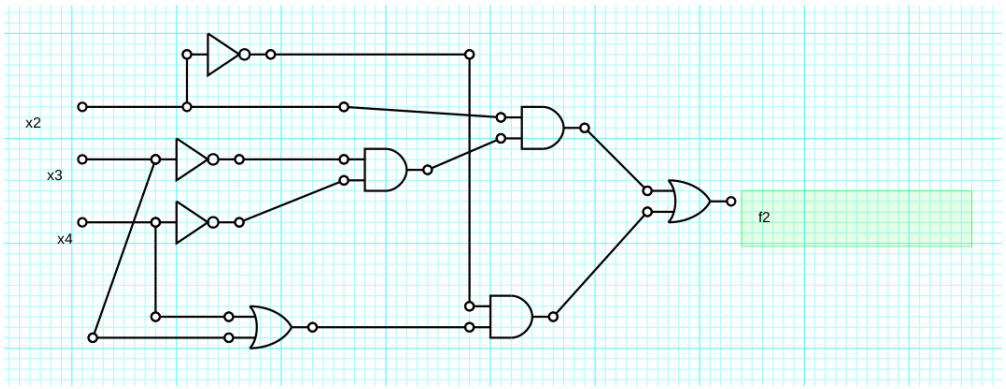

Figure 3: Grafico de compuertas logicas Bit 2

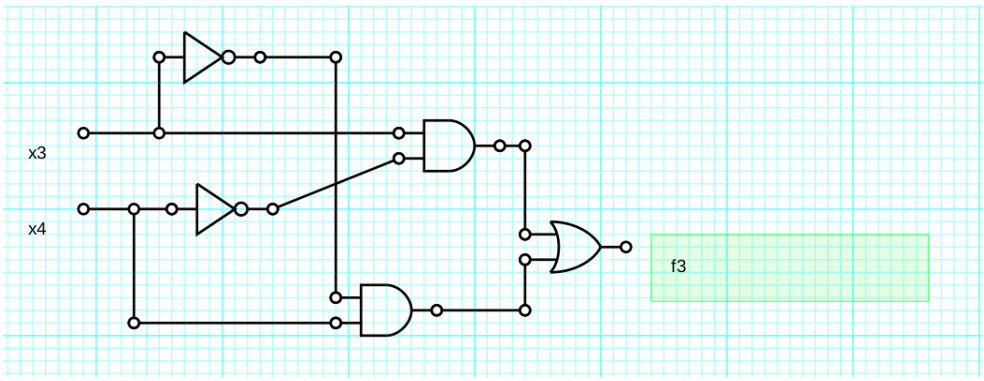

Figure 4: Grafico de compuertas logicas Bit 3

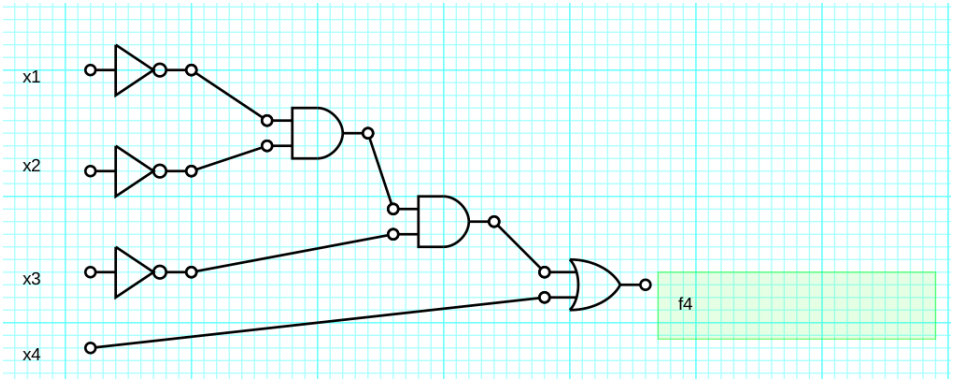

Figure 5: Grafico de compuertas logicas Bit 4

Finalmente, esta logica de compuertas fue implementada en verilog de la siguiente manera:

```
module twosComplement(x1,x2,x3,x4,f1,f2,f3,f4);
    input x1, x2, x3, x4;
    output f1, f2, f3, f4;
    wire nx1,nx2,nx3,nx4;
    not(nx1,x1);
    not(nx2,x2);
    not(nx3,x3);
    not(nx4,x4);

    //First Bit Logic
    wire temp1, temp2, temp3;
    and(temp1,x1,nx2,nx3,nx4);
    or(temp2,x2,x3,x4);
    and(temp3,temp2,nx1);
    or(f1,temp1,temp3); //First Bit output

    //Second Bit Logic
    wire t1,t2,t3;
    and(t1,x2,nx3,nx4);
    or(t2,x3,x4);
    and(t3,t2,nx2);
    or(f2,t1,t3); //Second Bit Output

    //Third Bit Logic
    wire r1,r2;
    and(r1,x3,nx4);
    and(r2,nx3,x4);
    or(f3,r1,r2); //Third Bit Output

    //Four Bit Output
    wire q;
    and(q,nx1,nx2,nx3);
    or(f4,x4,q); //Four Bit Output

endmodule
```

Figure 6: Implementacion de la logica en Verilog

y al probar el codigo con un test.v se obtuvo la siguiente salida, confirmando que el codigo se realizo de manera exitosa.

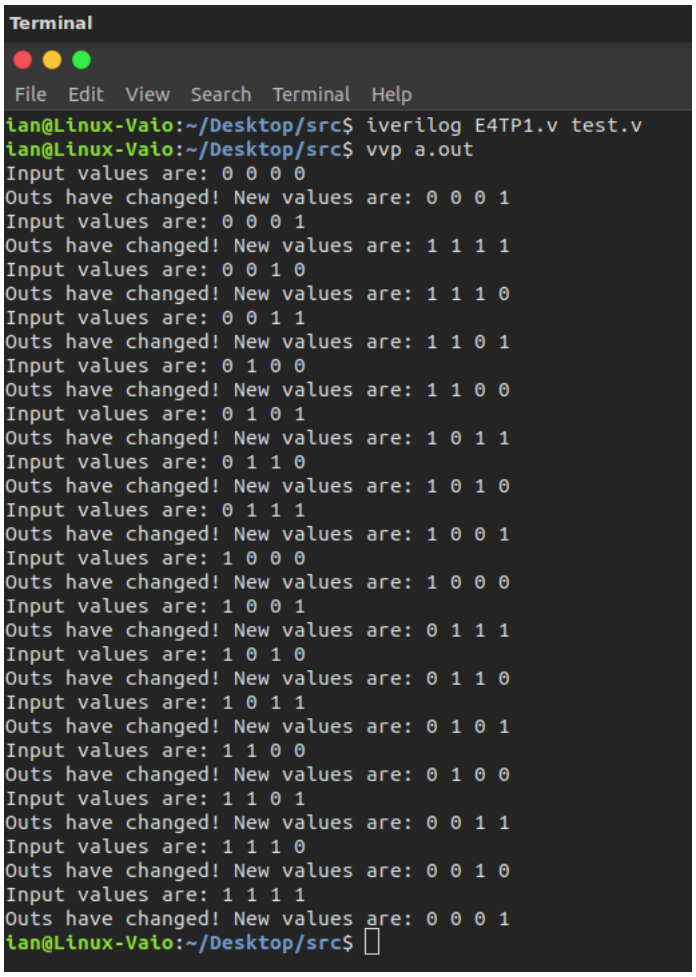

Figure 7: Salida de la implementacion en la Terminal