

1 Exercice 4

x_1	x_2	x_3	x_4	f_1	f_2	f_3	f_4
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Figure 1: Two's Complement truth table for 4 bits

If we write every single input bit according to the minterms, we have left the following equations:

$$f_1(m_i) = m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8$$

$$f_2(m_i) = m_1 + m_2 + m_3 + m_4 + m_9 + m_{10} + m_{11} + m_{12}$$

$$f_3(m_i) = m_1 + m_2 + m_5 + m_6 + m_9 + m_{10} + m_{13} + m_{14}$$

$$f_4(m_i) = m_1 + m_3 + m_5 + m_7 + m_9 + m_{11} + m_{13} + m_{15}$$

Replacing the values of each minterm, we have got the following:

$$f_1(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3\bar{x}_4 + \bar{x}_1\bar{x}_2x_3x_4 + \bar{x}_1x_2\bar{x}_3\bar{x}_4 + \bar{x}_1x_2\bar{x}_3x_4 + \bar{x}_1x_2x_3\bar{x}_4 + \bar{x}_1x_2x_3x_4 + x_1\bar{x}_2\bar{x}_3\bar{x}_4$$

$$f_2(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3\bar{x}_4 + \bar{x}_1\bar{x}_2x_3x_4 + \bar{x}_1x_2\bar{x}_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3x_4 + x_1\bar{x}_2x_3\bar{x}_4 + x_1\bar{x}_2x_3x_4 + x_1x_2\bar{x}_3\bar{x}_4$$

$$f_3(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3\bar{x}_4 + \bar{x}_1x_2\bar{x}_3x_4 + \bar{x}_1x_2x_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3x_4 + x_1\bar{x}_2x_3\bar{x}_4 + x_1x_2\bar{x}_3x_4 + x_1x_2x_3\bar{x}_4$$

$$f_4(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3x_4 + \bar{x}_1x_2\bar{x}_3x_4 + \bar{x}_1x_2x_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3x_4 + x_1\bar{x}_2x_3\bar{x}_4 + x_1x_2\bar{x}_3x_4 + x_1x_2x_3x_4$$

So, by simplification methods and properties, we can achieve this four formulas to describe each output bit according to the input bits:

$$f_1(x_1; x_2; x_3; x_4) = x_1\bar{x}_2\bar{x}_3\bar{x}_4 + \bar{x}_1(x_2 + x_3 + x_4)$$

$$f_2(x_1; x_2; x_3; x_4) = x_2\bar{x}_3\bar{x}_4 + \bar{x}_2(x_3 + x_4)$$

$$f_3(x_1; x_2; x_3; x_4) = x_3\bar{x}_4 + \bar{x}_3x_4$$

$$f_4(x_1; x_2; x_3; x_4) = x_4$$

By trying to express those formulas in logic gates graphs, we got the following:

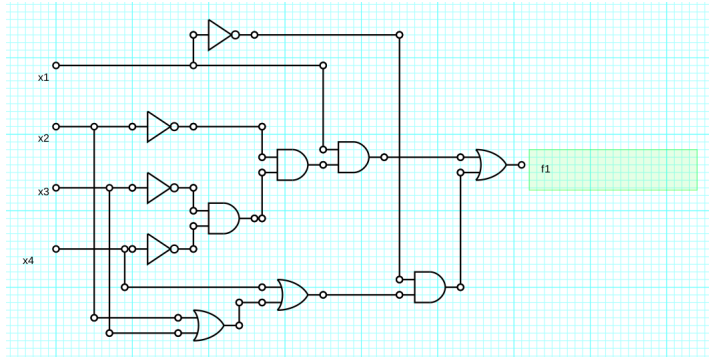


Figure 2: 1st Bit's logic gates graph

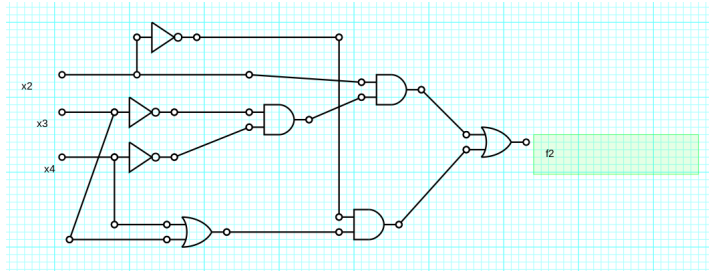


Figure 3: 2nd Bit's logic gates graph

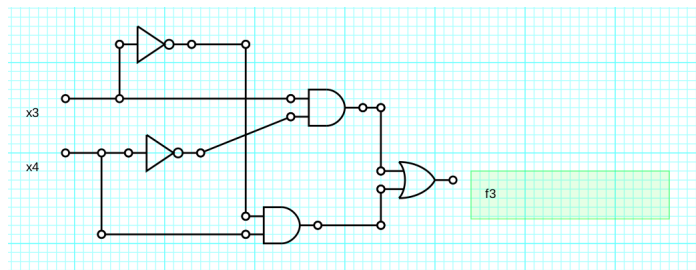


Figure 4: 3th Bit's logic gates graph

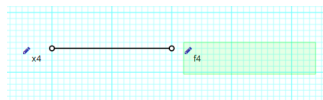


Figure 5: 4th Bit's logic gates graph

Finally, this logic was implemented on verilog as follows:

```

E4TP1.v
1  module twosComplement(x1,x2,x3,x4,f1,f2,f3,f4);
2      input x1, x2, x3, x4;
3      output f1, f2, f3, f4;
4      wire nx1,nx2,nx3,nx4;
5      not(nx1,x1);
6      not(nx2,x2);
7      not(nx3,x3);
8      not(nx4,x4);
9      //First Bit Logic
10     wire temp1, temp2, temp3;
11     and(temp1,x1,nx2,nx3,nx4);
12     or(temp2,x2,x3,x4);
13     and(temp3,temp2,nx1);
14     or(f1,temp1,temp3); //First Bit output
15
16     //Second Bit Logic
17     wire t1,t2,t3;
18     and(t1,x2,nx3,nx4);
19     or(t2,x3,x4);
20     and(t3,t2,nx2);
21     or(f2,t1,t3); //Second Bit Output
22
23     //Third Bit Logic
24     wire r1,r2;
25     and(r1,x3,nx4);
26     and(r2,nx3,x4);
27     or(f3,r1,r2); //Third Bit Output
28
29     //Four Bit Output
30     wire q;
31     and(f4,x4,x4);
32
33
34 endmodule
35

```

Figure 6: Verilog implementation

and, by testing the code with test.v, we have got the following output, confirming that the code was executed correctly.

```

lan@Linux-Vaio:~/Desktop/Electro III/GIT TPS/tp1-team-2/E4TP1/code/src$ vvp a.out
Input values are: 0 0 0 0
Outs have changed! New values are: 0 0 0 0
Input values are: 0 0 0 1
Outs have changed! New values are: 1 1 1 1
Input values are: 0 0 1 0
Outs have changed! New values are: 1 1 1 0
Input values are: 0 0 1 1
Outs have changed! New values are: 1 1 0 1
Input values are: 0 1 0 0
Outs have changed! New values are: 1 1 0 0
Input values are: 0 1 0 1
Outs have changed! New values are: 1 0 1 1
Input values are: 0 1 1 0
Outs have changed! New values are: 1 0 1 0
Input values are: 0 1 1 1
Outs have changed! New values are: 1 0 0 1
Input values are: 1 0 0 0
Outs have changed! New values are: 1 0 0 0
Input values are: 1 0 0 1
Outs have changed! New values are: 0 1 1 1
Input values are: 1 0 1 0
Outs have changed! New values are: 0 1 1 0
Input values are: 1 0 1 1
Outs have changed! New values are: 0 1 0 1
Input values are: 1 1 0 0
Outs have changed! New values are: 0 1 0 0
Input values are: 1 1 0 1
Outs have changed! New values are: 0 0 1 1
Input values are: 1 1 1 0
Outs have changed! New values are: 0 0 1 0
Input values are: 1 1 1 1
Outs have changed! New values are: 0 0 0 1
lan@Linux-Vaio:~/Desktop/Electro III/GIT TPS/tp1-team-2/E4TP1/code/src$

```

Figure 7: Terminal's output