Assignment 1

Group 2

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1 Excercise 3

Implement the following modules in Verilog:

- 4 inputs ENCODER
- 4 outputs DEMUX

2 4-Input ENCODER

2.1 Description

An encoder is an Application-Specific Integrated Circuit (ASIC) that converts information. In this case it receives a signal from a 4-bit input and returns the position of the Most Significant Bit that is currently on.

2.2 Code Implementation

The Code Implementation of both the Module and its testbench can be found in their respective directories.

2.3 Module Tests

Results of the Testbench:

Input	Output	Value
0001	00	0
0010	01	1
0100	10	2
1000	11	3
0011	01	1
0101	10	2
1001	11	3
0110	10	2
1010	11	3
1100	11	3

Table 1.1.3 ENCODER Testbench Results

2.4 Conclusions

The module is working as expected, where it is taking only the Most Significant Bit as the value to be encoded.

3 4-output DEMUX

3.1 Description

A DEMUX is an ASIC which receives an input signal and a selector signal. The selector signal determines through which output port the input signal is sent.

3.2 Code Implementation

The Code implementation for the DEMUX can be found in its corresponding folder.

3.3 Module Tests

Input	Selector	Out_0	Out_1	Out_2	Out_3
1	0	1	0	0	0
1	1	0	1	0	0
1	2	0	0	1	0
1	3	0	0	0	1

Table 1.2.3 DEMUX Testbench Results

3.4 Conclusions

The module is works as expected.