1 Exercise 4

x_1	x_2	x_3	x_4	f_1	f_2	f_3	f_4
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Figure 1: Two's Complement truth table for 4 bits

If we write every signle input bit according to the minterms, we have left the following equations:

$$f_1(m_i) = m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8$$

$$f_2(m_i) = m_1 + m_2 + m_3 + m_4 + m_9 + m_{10} + m_{11} + m_{12}$$

$$f_3(m_i) = m_1 + m_2 + m_5 + m_6 + m_9 + m_{10} + m_{13} + m_{14}$$

$$f_4(m_i) = m_1 + m_3 + m_5 + m_7 + m_9 + m_{11} + m_{13} + m_{15}$$

Replacing the values of each minterm, we have got the following:

$$f_1(x_1;x_2;x_3;x_4) = \bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3\bar{x_4} + \bar{x_1}\bar{x_2}x_3x_4 + \bar{x_1}x_2\bar{x_3}\bar{x_4} + \bar{x_1}x_2\bar{x_3}x_4 + \bar{x_1}x_2x_3\bar{x_4} + \bar{x_1}x_2x_3x_4 + x_1\bar{x_2}\bar{x_3}\bar{x_4}$$

$$f_2(x_1;x_2;x_3;x_4) = \bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3\bar{x_4} + \bar{x_1}\bar{x_2}x_3x_4 + \bar{x_1}x_2\bar{x_3}\bar{x_4} + x_1\bar{x_2}\bar{x_3}x_4 + x_1\bar{x_2}x_3\bar{x_4} + x_1\bar{x_2}x_3x_4 + x_1x_2\bar{x_3}\bar{x_4}$$

$$f_3(x_1;x_2;x_3;x_4) = \bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3\bar{x_4} + \bar{x_1}x_2\bar{x_3}x_4 + \bar{x_1}x_2x_3\bar{x_4} + x_1\bar{x_2}\bar{x_3}x_4 + x_1\bar{x_2}x_3\bar{x_4} + x_1x_2\bar{x_3}x_4 + x_1x_2x_3\bar{x_4}$$

$$f_4(x_1;x_2;x_3;x_4) = \bar{x_1}\bar{x_2}\bar{x_3}x_4 + \bar{x_1}\bar{x_2}x_3x_4 + \bar{x_1}x_2\bar{x_3}x_4 + \bar{x_1}x_2x_3x_4 + x_1\bar{x_2}\bar{x_3}x_4 + x_1\bar{x_2}x_3x_4 + x_1x_2\bar{x_3}x_4 + x_1x_2x_3x_4$$

So, by simplification methods and properties, we can achieve this four formulas to describe each output bit according to the input bits:

$$f_1(x_1;x_2;x_3;x_4) = x_1\bar{x_2}\bar{x_3}\bar{x_4} + \bar{x_1}(x_2 + x_3 + x_4)$$

$$f_2(x_1;x_2;x_3;x_4) = x_2\bar{x_3}\bar{x_4} + \bar{x_2}(x_3 + x_4)$$

$$f_3(x_1;x_2;x_3;x_4) = x_3\bar{x_4} + \bar{x_3}x_4$$

$$f_4(x_1;x_2;x_3;x_4) = x_4$$

By trying to express those formulas in logic gates graphs, we got the following:

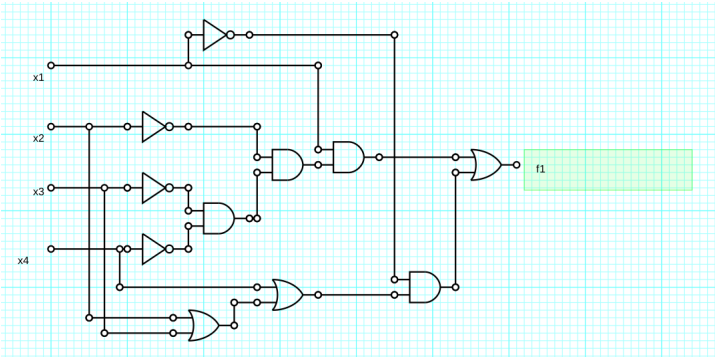

Figure 2: 1st Bit's logic gates graph

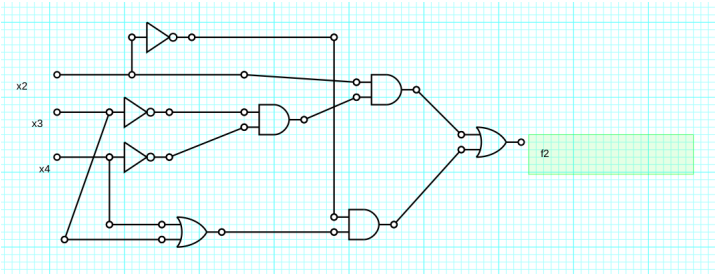

Figure 3: 2nd Bit's logic gates graph

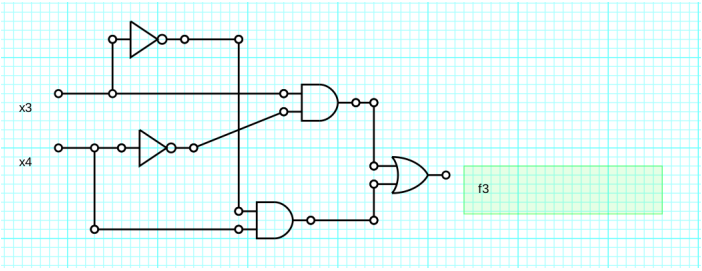

Figure 4: 3th Bit's logic gates graph

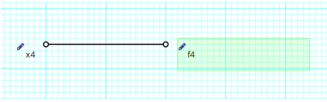

Figure 5: 4th Bit's logic gates graph

Finally, this logic was implemented on verilog as follows:

E4TP1.v

```
module twosComplement(x1,x2,x3,x4,f1,f2,f3,f4);
    input x1, x2, x3, x4;
    output f1, f2, f3, f4;
    wire nx1,nx2,nx3,nx4;
    not(nx1,x1);
    not(nx2,x2);
    not(nx3,x3);
    not(nx4,x4);
    //First Bit Logic
    wire temp1, temp2, temp3;
    and(temp1,x1,nx2,nx3,nx4);
    or(temp2,x2,x3,x4);
    and(temp3,temp2,nx1);
    or(f1,temp1,temp3); //First Bit output

    //Second Bit Logic
    wire t1,t2,t3;
    and(t1,x2,nx3,nx4);
    or(t2,x3,x4);
    and(t3,t2,nx2);
    or(f2,t1,t3); //Second Bit Output

    //Third Bit Logic
    wire r1,r2;
    and(r1,x3,nx4);
    and(r2,nx3,x4);
    or(f3,r1,r2); //Third Bit Output

    //Four Bit Output
    wire q;
    and(f4,x4,x4);


endmodule

```

Figure 6: Verilog implementation

and, by testing the code with test.v, we have got the following output, confirming that the code was executed correctly.

```
ian@Linux-Vaio:~/Desktop/Electro III/GIT TPS/tp1-team-2/E4TP1/code/src$ vvp a.out
Input values are: 0 0 0 0
Outs have changed! New values are: 0 0 0 0
Input values are: 0 0 0 1
Outs have changed! New values are: 1 1 1 1
Input values are: 0 0 1 0
Outs have changed! New values are: 1 1 1 0
Input values are: 0 0 1 1
Outs have changed! New values are: 1 1 0 1
Input values are: 0 1 0 0
Outs have changed! New values are: 1 1 0 0
Input values are: 0 1 0 1
Outs have changed! New values are: 1 0 1 1
Input values are: 0 1 1 0
Outs have changed! New values are: 1 0 1 0
Input values are: 0 1 1 1
Outs have changed! New values are: 1 0 0 1
Input values are: 1 0 0 0
Outs have changed! New values are: 1 0 0 0
Input values are: 1 0 0 1
Outs have changed! New values are: 0 1 1 1
Input values are: 1 0 1 0
Outs have changed! New values are: 0 1 1 0
Input values are: 1 0 1 1
Outs have changed! New values are: 0 1 0 1
Input values are: 1 1 0 0
Outs have changed! New values are: 0 1 0 0
Input values are: 1 1 0 1
Outs have changed! New values are: 0 0 1 1
Input values are: 1 1 1 0
Outs have changed! New values are: 0 0 1 0
Input values are: 1 1 1 1
Outs have changed! New values are: 0 0 0 1
ian@Linux-Vaio:~/Desktop/Electro III/GIT TPS/tp1-team-2/E4TP1/code/src$
```

Figure 7: Terminal's output