

1 Ejercicio 4

| x_1 | x_2 | x_3 | x_4 | f_1 | f_2 | f_3 | f_4 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Figure 1: Complemento a 2 de los bits de entrada

Si escribimos cada bit de salida en función de los mintérminos de los bits de entrada, nos quedan las siguientes ecuaciones:

$$f_1(m_i) = m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8$$

$$f_2(m_i) = m_1 + m_2 + m_3 + m_4 + m_9 + m_{10} + m_{11} + m_{12}$$

$$f_3(m_i) = m_1 + m_2 + m_5 + m_6 + m_9 + m_{10} + m_{13} + m_{14}$$

$$f_4(m_i) = m_1 + m_3 + m_5 + m_7 + m_9 + m_{11} + m_{13} + m_{15}$$

Remplazando los valores de cada mintermino, quedan las siguientes formulas:

$$f_1(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3\bar{x}_4 + \bar{x}_1\bar{x}_2x_3x_4 + \bar{x}_1x_2\bar{x}_3\bar{x}_4 + \bar{x}_1x_2\bar{x}_3x_4 + \bar{x}_1x_2x_3\bar{x}_4 + \bar{x}_1x_2x_3x_4 + x_1\bar{x}_2\bar{x}_3\bar{x}_4$$

$$f_2(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3\bar{x}_4 + \bar{x}_1\bar{x}_2x_3x_4 + \bar{x}_1x_2\bar{x}_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3x_4 + x_1\bar{x}_2x_3\bar{x}_4 + x_1\bar{x}_2x_3x_4 + x_1x_2\bar{x}_3\bar{x}_4$$

$$f_3(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3\bar{x}_4 + \bar{x}_1x_2\bar{x}_3x_4 + \bar{x}_1x_2x_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3x_4 + x_1\bar{x}_2x_3\bar{x}_4 + x_1x_2\bar{x}_3x_4 + x_1x_2x_3\bar{x}_4$$

$$f_4(x_1; x_2; x_3; x_4) = \bar{x}_1\bar{x}_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_3x_4 + \bar{x}_1x_2\bar{x}_3x_4 + \bar{x}_1x_2x_3\bar{x}_4 + x_1\bar{x}_2\bar{x}_3x_4 + x_1\bar{x}_2x_3x_4 + x_1x_2\bar{x}_3x_4 + x_1x_2x_3\bar{x}_4$$

Si simplificamos cada ecuación, se puede llegar a las siguientes expresiones:

$$f_1(x_1; x_2; x_3; x_4) = x_1\bar{x}_2\bar{x}_3\bar{x}_4 + \bar{x}_1(x_2 + x_3 + x_4)$$

$$f_2(x_1; x_2; x_3; x_4) = x_2\bar{x}_3\bar{x}_4 + \bar{x}_2(x_3 + x_4)$$

$$f_3(x_1; x_2; x_3; x_4) = x_3\bar{x}_4 + \bar{x}_3x_4$$

$$f_4(x_1; x_2; x_3; x_4) = x_4$$

Al intentar expresar dichas formulas en graficos de compuertas logicas, se consiguieron los siguientes:

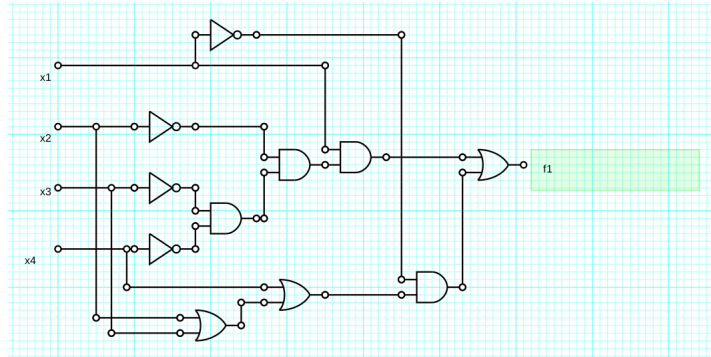


Figure 2: Grafico de compuertas logicas Bit 1

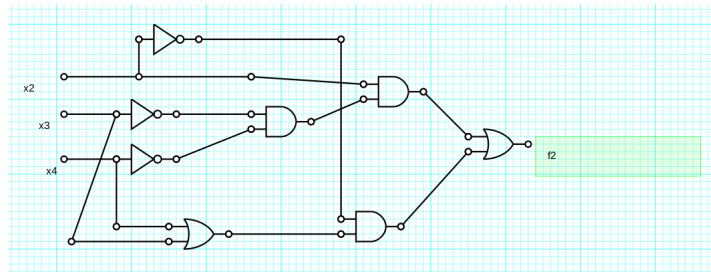


Figure 3: Grafico de compuertas logicas Bit 2

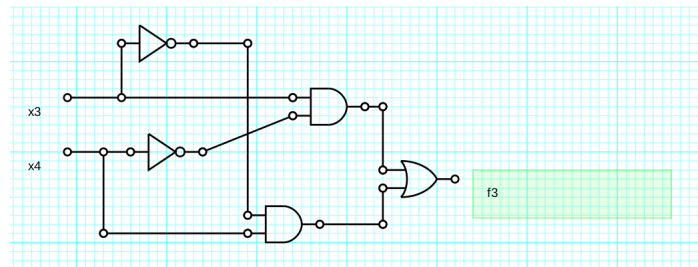


Figure 4: Grafico de compuertas logicas Bit 3

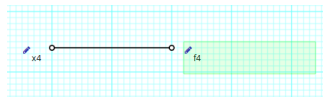


Figure 5: Grafico de compuertas logicas Bit 4

Finalmente, esta logica de compuertas fue implementada en verilog de la siguiente manera:

```

E4TP1.v
1  module twosComplement(x1,x2,x3,x4,f1,f2,f3,f4);
2      input x1, x2, x3, x4;
3      output f1, f2, f3, f4;
4      wire nx1,nx2,nx3,nx4;
5      not(nx1,x1);
6      not(nx2,x2);
7      not(nx3,x3);
8      not(nx4,x4);
9      //First Bit Logic
10     wire temp1, temp2, temp3;
11     and(temp1,x1,nx2,nx3,nx4);
12     or(temp2,x2,x3,x4);
13     and(temp3,temp2,nx1);
14     or(f1,temp1,temp3); //First Bit output
15
16     //Second Bit Logic
17     wire t1,t2,t3;
18     and(t1,x2,nx3,nx4);
19     or(t2,x3,x4);
20     and(t3,t2,nx2);
21     or(f2,t1,t3); //Second Bit Output
22
23     //Third Bit Logic
24     wire r1,r2;
25     and(r1,x3,nx4);
26     and(r2,nx3,x4);
27     or(f3,r1,r2); //Third Bit Output
28
29     //Four Bit Output
30     wire q;
31     and(f4,x4,x4);
32
33
34 endmodule
35

```

Figure 6: Implementacion de la logica en Verilog

y al probar el codigo con un test.v se obtuvo la siguiente salida, confirmando que el codigo se realizo de manera exitosa.

```

lan@Linux-Valo:~/Desktop/Electro III/GIT TPS/tp1-team-2/E4TP1/code/src$ vvp a.out
Input values are: 0 0 0 0
Outs have changed! New values are: 0 0 0 0
Input values are: 0 0 0 1
Outs have changed! New values are: 1 1 1 1
Input values are: 0 0 1 0
Outs have changed! New values are: 1 1 1 0
Input values are: 0 0 1 1
Outs have changed! New values are: 1 1 0 1
Input values are: 0 1 0 0
Outs have changed! New values are: 1 1 0 0
Input values are: 0 1 0 1
Outs have changed! New values are: 1 0 1 1
Input values are: 0 1 1 0
Outs have changed! New values are: 1 0 1 0
Input values are: 0 1 1 1
Outs have changed! New values are: 1 0 0 1
Input values are: 1 0 0 0
Outs have changed! New values are: 1 0 0 0
Input values are: 1 0 0 1
Outs have changed! New values are: 0 1 1 1
Input values are: 1 0 1 0
Outs have changed! New values are: 0 1 1 0
Input values are: 1 0 1 1
Outs have changed! New values are: 0 1 0 1
Input values are: 1 1 0 0
Outs have changed! New values are: 0 1 0 0
Input values are: 1 1 0 1
Outs have changed! New values are: 0 0 1 1
Input values are: 1 1 1 0
Outs have changed! New values are: 0 0 1 0
Input values are: 1 1 1 1
Outs have changed! New values are: 0 0 0 1
lan@Linux-Valo:~/Desktop/Electro III/GIT TPS/tp1-team-2/E4TP1/code/src$

```

Figure 7: Salida de la implementacion en la Terminal