1 Implementation of Synchronous and Asynchronous 3-bit counters

Using the schematic in Figures 1 and 2 and the circuits were implemented on a Printed Circuit Board.

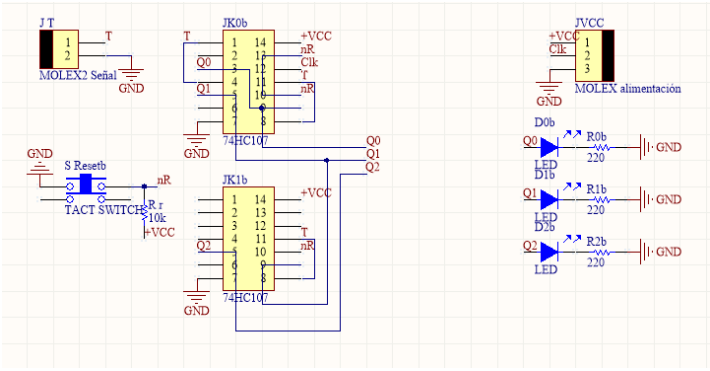

Figure 1: Shcematics for the Asynchronous counter

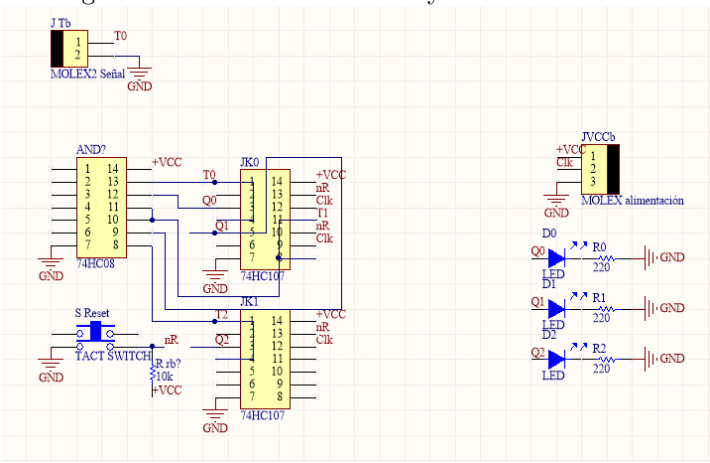

Figure 2: Schematics for the Synchronous counter

First, the behaviour of both devices was verified. Line 1 represents the Clk signal while lines 2, 3 and 4 represent a binary bit in the counter.

It can be observed from Figures 3 and 4 that at this relatively low frequency, there is no visible difference on the behaviour of both counters. However, upon increasing the frequency and measuring the delays between each negative edge slope, the differences in operation can be observed.

On Figures 5 and 6 the difference in behaviour can clearly be seen: while on the Asynchronous counter the delay between each subsequent signal is within similar values, in the Synchronous counter there is only significant delay between the clock signal(1) and all the other signals, while between signals 2, 3, and 4, is an order of magnitude lower.

When using the maximum available frequency on both counters, one can see the limitations of the Asynchronous configuration: at this frequency, the clock signal and the 3rd bit signal start to overlap (confirmed by the negative measurement of the delay between them in Figure 7), while the Synchronous configuration's waveforms remain without overlap and delays on the positive side of the scale (Figure 8).

In conclusion, despite the Asynchronous counter's economical advantage due to the use of fewer

Figure 3: Asynchronous counter test on 10 kHz

components, it runs into the limitation that it will stop working properly at high frequencies, while the Synchronous counter, despite requiring more components, it continues working properly at much higher frequencies.

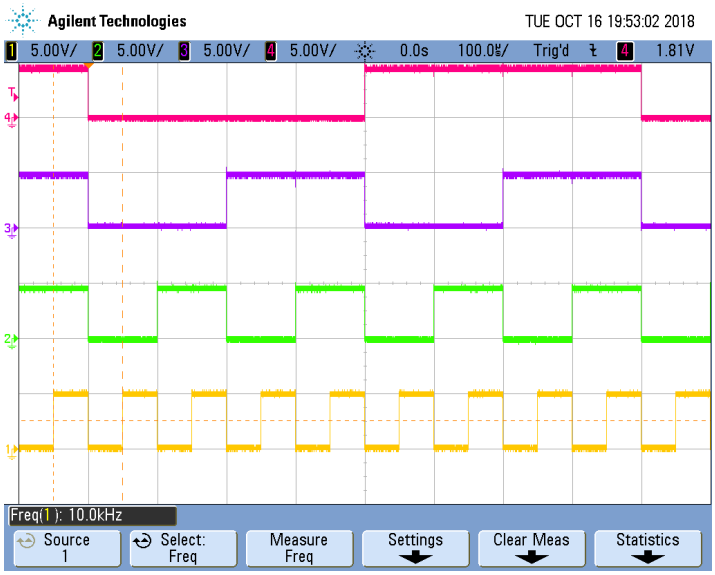

Figure 4: Sinchronous counter test on 10 kHz

Figure 5: Asynchronous counter test on 1 MHz

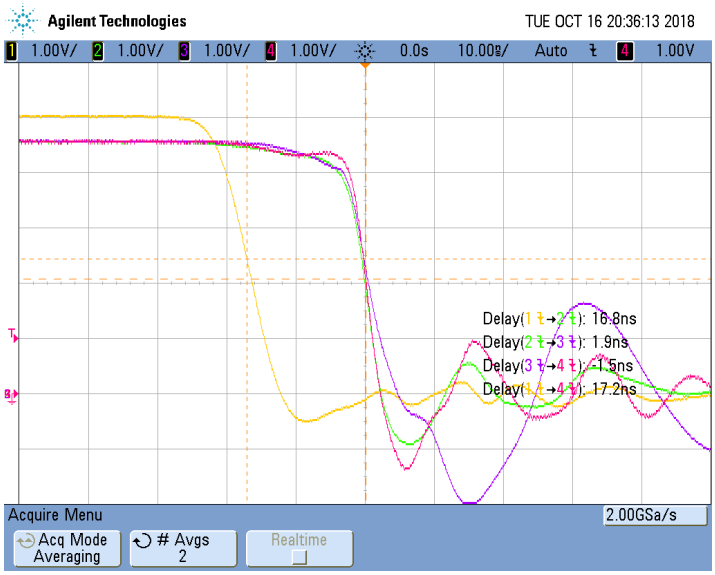

Figure 6: Synchronous counter test on 1MHz

Figure 7: Asynchronous counter test on 20 MHz

Figure 8: Synchronous counter test on 20 MHz