1 Exercise 1: Design and Implementation of NOT Gates Using Transistors

The following parameters are important when designing NOT Gates.

1.0.1 High-Level and Low-Level Input Voltages

The high-level input voltage (V_{IH}) is the minimum input voltage that is considered as high, while the low-level input voltage (V_{IL}) is the maximum input voltage that is considered as low.

1.0.2 High-Level and Low-Level Output Voltages

The high-level output voltage (V_{OH}) is the minimum output voltage that the circuit provides as a high, while the low-level output voltage (V_{OL}) is the maximum output voltage that the circuit provides as a low.

1.0.3 Noise Margin

The high noise margin (NM_H) is the gap between the high-level input voltage and the high-level output voltage, while the low noise margin (NM_L) is the gap between the low-level output voltage and the low-level input voltage.

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

1.0.4 Propagation Delays

For this assignment's meassures, when the input changes from low to hight and the output from high to low, the high-to-low propagation delay is considered as the time between the moment in which the input voltage reaches the 90% of its maximum high value, until the moment in which the output voltage reaches the 10% of its maximum high value.

$$t_{pHL} = t_{10\%V_{maxO}} - t_{90\%V_{maxI}}$$

In the case in which the input goes from high to low and the output from low to high, the low-to-high propagation delay is considered as the time between the moment in which the input voltage reaches the 10% of its maximum high value, until the moment in which the output voltage reaches the 90% of its maximum high value.

$$t_{pLH} = t_{90\%V_{maxO}} - t_{10\%V_{maxI}}$$

1.0.5 Transition Times

The high-to-low transition time or fall time (t_f) is the time that it takes the output voltage to go from its high maximum value to its low minimum value, while the low-to-high transition time or rise time (t_r) is the time that it takes for it to change from its low minimum value to tis high maximum value.

1.0.6 Maximum Output Current

The maximum output current the circuit provides in the output, which will take place when there is a capacitor, is calculated from the equation:

$$I_C = C\frac{dVc}{dt}$$

Where the maximum output current of the circuit will take place when there is a change in the voltage, form high to low or low to high.
ESTO ES NPN PARA MAX CURRENT

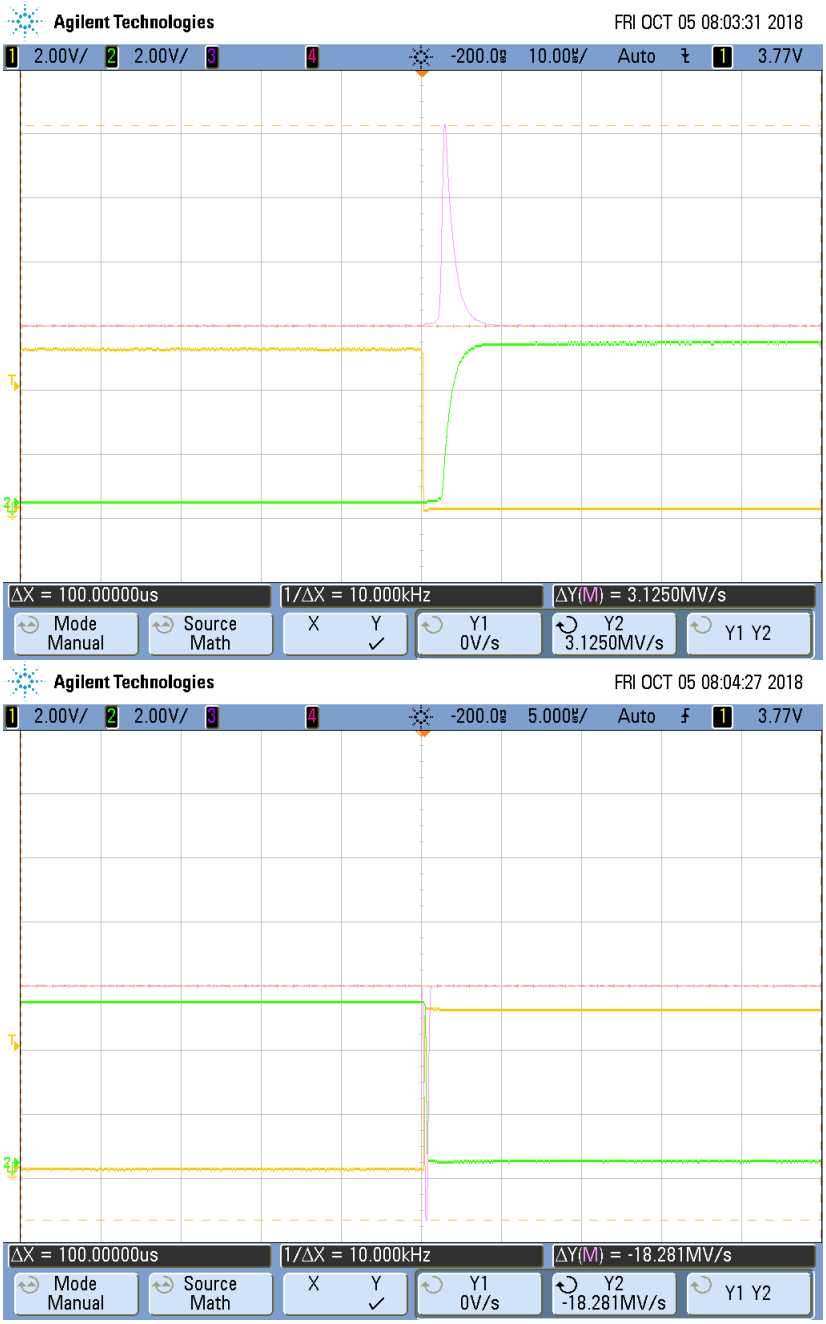

Figure 1.1: NPN Maximun output current

ESTO ES PNP PARA MAX CURRENT

1.1 NOT Gates' Designs

«««< Updated upstream Figure 1.4 represents a NOT gate built with a BJT NPN 337 transistor, while the circuit in Figure 1.4 corresponds to a NOT gate that uses a BJT PNP 327 transistor. The $4,7k\Omega$ resistors that appear in both circuits where chosen after simulations made with LTspice. We evaluated how the noise margin changed according to this resistor's value. As it is preffered to have a small noise margin because it corresponds to the "prohibited" voltage values, the $4,7k\Omega$ resistor was chosen over bigger values.

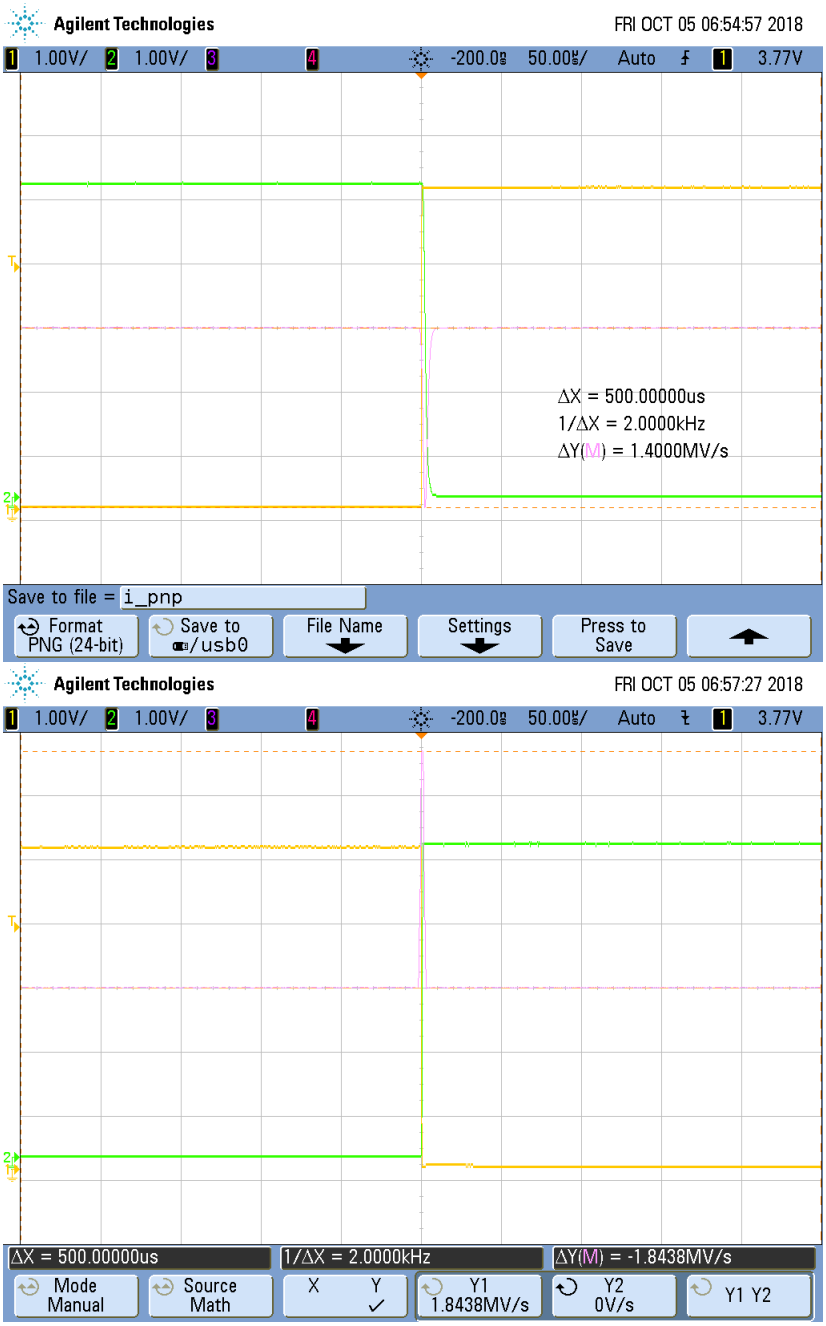

Figure 1.2: PNP Maximun output current

1.2 Measurements

The parameters defined above were measured for each of the circuits in Figures 1.3 and 1.4 in two different conditions: without loading the output and with a $1nF$ capacitor connected to the output. Te results are shown in the following table.

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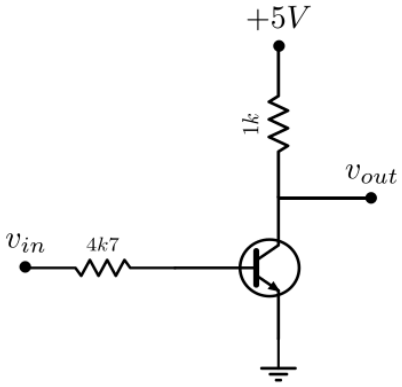

Figure 1.3: NOT Gate Using a NPN Transistor

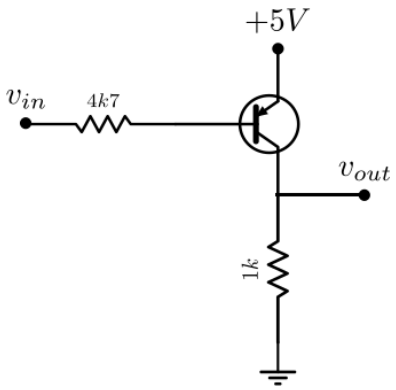

Figure 1.4: NOT Gate Using a PNP Transistor

1.3 Measurements

1.4 Using a BJT NPN 337 Transistor

1.4.1 Without Load Connected to the Output

1.4.2 With a $1nF$ Capacitor Connected to the Output

1.5 Using a BJT PNP 327 Transistor

1.5.1 Without Load Connected to the Output

»»»»> Stashed changes

	NPN	NPN with capacitor	PNP	PNP with capacitor
$V_{IH}(V)$	0,9	0,9	4,5	4,6
$V_{IL}(V)$	0,5V	0,6	4,2	4,3
$V_{OH}(V)$	4,96V	4,56	4,77	5
$V_{OL}(V)$	0,1	0,12	0,05	0,45
$NM_H(V)$	4,06	3,66	0,27	0,4
$NM_L(V)$	0,4	0,48	4,15	3,85
t_{pHL}	87ns	$2,7\mu s$	$2,72\mu s$	101ns
t_{pLH}	$2,94\mu s$	104ns	73ns	$2,23\mu s$
t_f	69,5ns	84ns	575ns	770ns
t_r	505ns	520ns	83ns	86 ns
I_{OutMax}				