1 Exercise 1: Design and Implementation of NOT Gates Using Transistors

The following parameters are important when designing NOT Gates.

1.0.1 High-Level and Low-Level Input Voltages

The high-level input voltage (V_{IH}) is the minimum input voltage that is considered as high, while the low-level input voltage (V_{IL}) is the maximum input voltage that is considered as low. These values correspond to the values of the input voltage when the output voltage's slope is -1.

1.0.2 High-Level and Low-Level Output Voltages

The high-level output voltage (V_{OH}) is the output voltage that the circuit provides as a high, while the low-level output voltage (V_{OL}) is the output voltage that the circuit provides as a low.

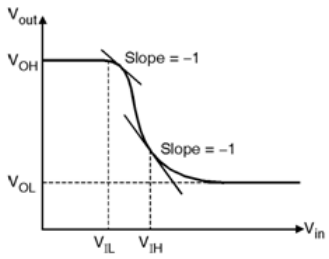

Figure 1.1: High-Level and Low-Level Output and Input Voltages

1.0.3 Noise Margin

The high noise margin (NM_H) is the gap between the high-level input voltage and the high-level output voltage, while the low noise margin (NM_L) is the gap between the low-level output voltage and the low-level input voltage.

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

1.0.4 Propagation Delays

When the input changes from low to hight and the output from high to low, the high-to-low propagation delay is considered as the time between the moment in which the input voltage reaches the 50% of its maximum high value, until the moment in which the output voltage reaches the 50% of its maximum high value.

$$t_{pHL} = t_{50\%V_{maxO}} - t_{50\%V_{maxI}}$$

In the case in which the input goes from high to low and the output from low to high, the low-to-high propagation delay is considered as the time between the moment in which the input voltage reaches the 50% of its maximum high value, until the moment in which the output voltage reaches the 50% of its maximum high value.

$$t_{pLH} = t_{50\%V_{maxO}} - t_{50\%V_{maxI}}$$

1.0.5 Transition Times

The high-to-low transition time or fall time (t_f) is the time that it takes the output voltage to go from its high maximum value to its low minimum value, while the low-to-high transition time or rise time (t_r) is the time that it takes for it to change from its low minimum value to tis high maximum value.

1.0.6 Maximum Output Current

The maximum output current the circuit provides when there is a capacitor, is calculated from the equation:

$$I_C = C\frac{dVc}{dt}$$

Where the maximum output current of the circuit will take place when there is a change in the voltage, form high to low or low to high.

1.1 NOT Gates' Designs

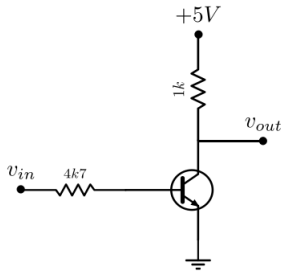

Figure 1.2: NOT Gate Using a NPN Transistor

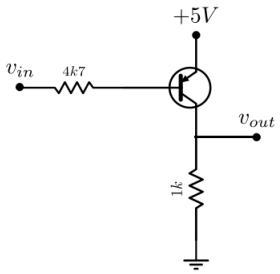

Figure 1.3: NOT Gate Using a PNP Transistor

Figure 1.3 represents a NOT gate built with a BJT NPN 337 transistor, while the circuit in Figure 1.3 corresponds to a NOT gate that uses a BJT PNP 327 transistor. The $4,7k\Omega$ resistors that appear in both circuits where chosen after simulations made with LTspice. We evaluated how the noise margin changed according to this resistor's value. As it is preffered to have a small noise margin because it corresponds to the "prohibited" voltage values, the $4,7k\Omega$ resistor was chosen over bigger values. The simulations were made as it is seen in the following figure. The blue line corresponds to the output voltage. The green line above corresponds to its derivate and the red line has a constant value of -1. This red constant line allowed to find visually quickly the range between both points of intersection with the derivate of the output voltage. These intersections are the cases in which the slope of the output voltage is equal to -1.

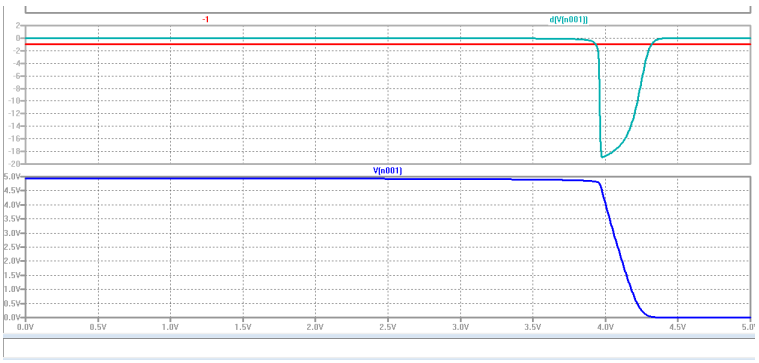

Figure 1.4: Simulation with $4,7k\Omega$ resistor for the PNP circuit

1.2 Measurements

The parameters defined above were measured for each of the circuits in Figures 1.2 and 1.3 in two different conditions: without loading the output and with a $1nF$ capacitor connected to the output. Te results are shown in the following Table 1.1.

	NPN	NPN with capacitor	PNP	PNP with capacitor
$V_{IH}(V)$	0,9	0,9	4,5	4,6
$V_{IL}(V)$	0,5V	0,6	4,2	4,3
$V_{OH}(V)$	4,96V	4,56	4,77	5
$V_{OL}(V)$	0,1	0,12	0,05	0,45
$NM_H(V)$	4,06	3,66	0,27	0,4
$NM_L(V)$	0,4	0,48	4,15	3,85
t_{pHL} (ns)	87	2700	2720	101
t_{pLH} (ns)	2940	104	73	2230
t_f (ns)	69,5	84	575	770
t_r (ns)	505	520	83	86
$I_{OutMax}(mA)$	-	18,28	-	1,8438

Table 1.1: Measurements of voltage levels, noise margins, propagation delays and transition times.

Note: The maximum output current was important to be measured in the cases with the capacitor in the output. In the following figures it can be seen how the maximum current was obtained using the osciloscope. By obtaining the derivate of the output voltage, it is multiplied by the value of the capacitance added in order to get the value of the current. It can be seen in the following images that the output current is not the same when responding to a possitive edge than to a negative edge from the imput's signal. The maximum from both cases is the one shown in table 1.1.

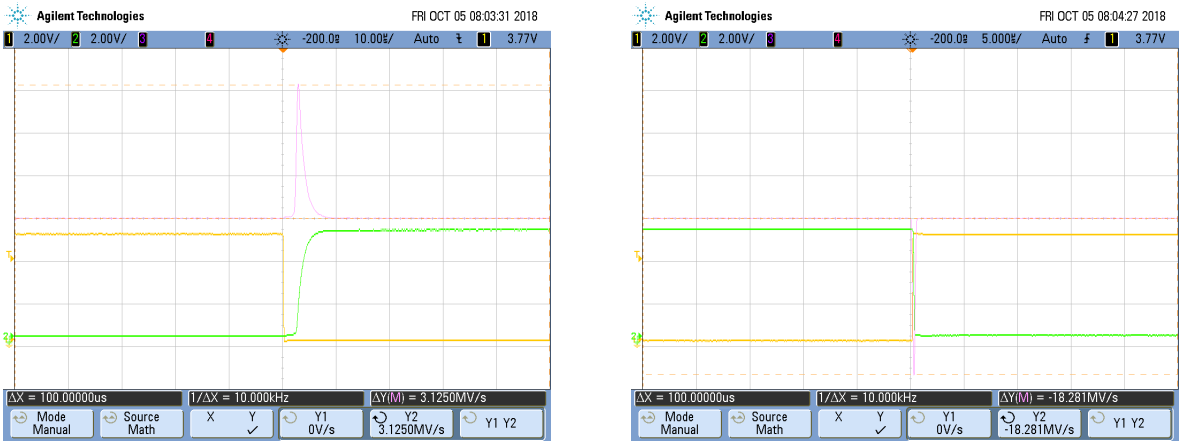

Figure 1.5: NPN Maximun output current

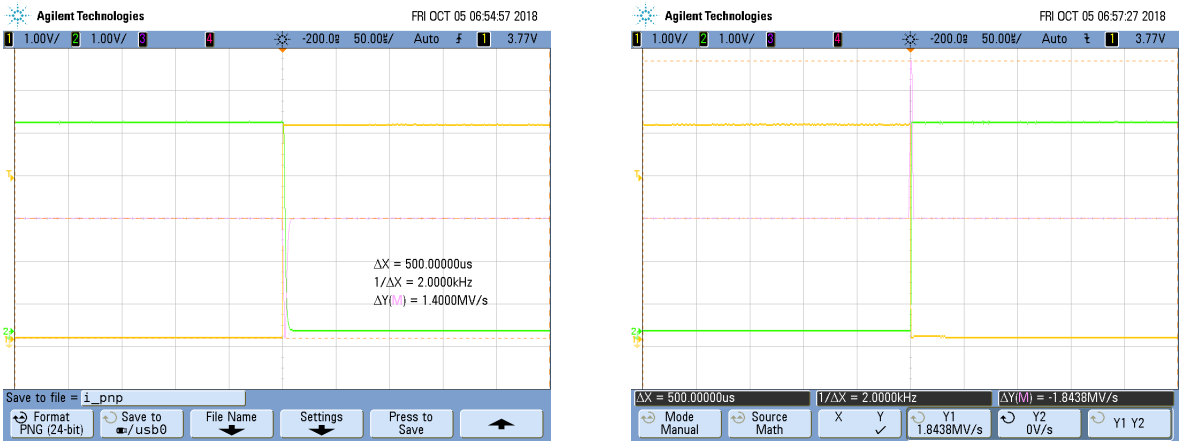

Figure 1.6: PNP Maximun output current