INSTITUTO TECNOLÓGICO DE BUENOS AIRES

Assignment N^o2

Electrónica 3 - 2018

Group 2

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1 Exercise 1: Design and Implementation of NOT Gates Using Transistors

The following parameters are important when designing NOT Gates.

1.0.1 High-Level and Low-Level Input Voltages

The high-level input voltage (V_{IH}) is the minimum input voltage that is considered as high, while the low-level input voltage (V_{IL}) is the maximum input voltage that is considered as low. These values correspond to the values of the input voltage when the output voltage's slope is -1.

1.0.2 High-Level and Low-Level Output Voltages

The high-level output voltage (V_{OH}) is the output voltage that the circuit provides as a high, while the low-level output voltage (V_{OL}) is the output voltage that the circuit provides as a low.

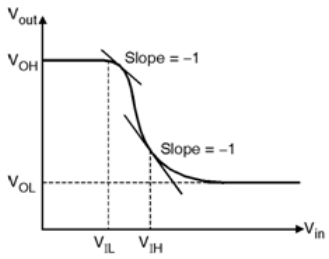

Figure 1.1: High-Level and Low-Level Output and Input Voltages

1.0.3 Noise Margin

The high noise margin (NM_H) is the gap between the high-level input voltage and the high-level output voltage, while the low noise margin (NM_L) is the gap between the low-level output voltage and the low-level input voltage.

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

1.0.4 Propagation Delays

When the input changes from low to hight and the output from high to low, the high-to-low propagation delay is considered as the time between the moment in which the input voltage reaches the 50% of its maximum high value, until the moment in which the output voltage reaches the 50% of its maximum high value.

$$t_{pHL} = t_{50\%V_{maxO}} - t_{50\%V_{maxI}}$$

In the case in which the input goes from high to low and the output from low to high, the low-to-high propagation delay is considered as the time between the moment in which the input voltage reaches the 50% of its maximum high value, until the moment in which the output voltage reaches the 50% of its maximum high value.

$$t_{pLH} = t_{50\%V_{maxO}} - t_{50\%V_{maxI}}$$

1.0.5 Transition Times

The high-to-low transition time or fall time (t_f) is the time that it takes the output voltage to go from its high maximum value to its low minimum value, while the low-to-high transition time or rise time (t_r) is the time that it takes for it to change from its low minimum value to tis high maximum value.

1.0.6 Maximum Output Current

The maximum output current the circuit provides when there is a capacitor, is calculated from the equation:

$$I_C = C\frac{dVc}{dt}$$

Where the maximum output current of the circuit will take place when there is a change in the voltage, form high to low or low to high.

1.1 NOT Gates' Designs

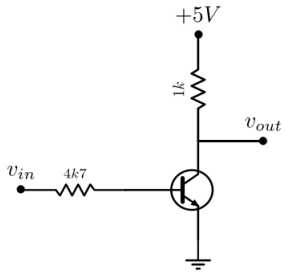

Figure 1.2: NOT Gate Using a NPN Transistor

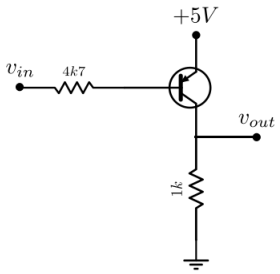

Figure 1.3: NOT Gate Using a PNP Transistor

Figure 1.3 represents a NOT gate built with a BJT NPN 337 transistor, while the circuit in Figure 1.3 corresponds to a NOT gate that uses a BJT PNP 327 transistor. The $4,7k\Omega$ resistors that appear in both circuits where chosen after simulations made with LTspice. We evaluated how the noise margin changed according to this resistor's value. As it is preffered to have a small noise margin because it corresponds to the "prohibited" voltage values, the $4,7k\Omega$ resistor was chosen over bigger values. The simulations were made as it is seen in the following figure. The blue line corresponds to the output voltage. The green line above corresponds to its derivate and the red line has a constant value of -1. This red constant line allowed to find visually quickly the range between both points of intersection with the derivate of the output voltage. These intersections are the cases in which the slope of the output voltage is equal to -1.

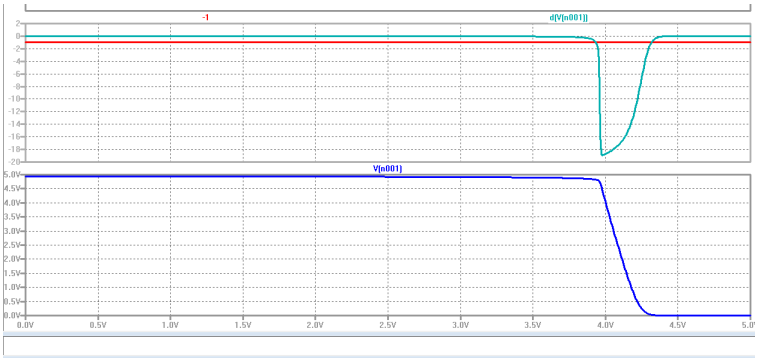

Figure 1.4: Simulation with $4,7k\Omega$ resistor for the PNP circuit

1.2 Measurements

The parameters defined above were measured for each of the circuits in Figures 1.2 and 1.3 in two different conditions: without loading the output and with a $1nF$ capacitor connected to the output. Te results are shown in the following Table 1.1.

	NPN	NPN with capacitor	PNP	PNP with capacitor
$V_{IH}(V)$	0,9	0,9	4,5	4,6
$V_{IL}(V)$	0,5V	0,6	4,2	4,3
$V_{OH}(V)$	4,96V	4,56	4,77	5
$V_{OL}(V)$	0,1	0,12	0,05	0,45
$NM_H(V)$	4,06	3,66	0,27	0,4
$NM_L(V)$	0,4	0,48	4,15	3,85
t_{pHL} (ns)	87	2700	2720	101
t_{pLH} (ns)	2940	104	73	2230
t_f (ns)	69,5	84	575	770
t_r (ns)	505	520	83	86
$I_{OutMax}(mA)$	-	18,28	-	1,8438

Table 1.1: Measurements of voltage levels, noise margins, propagation delays and transition times.

Note: The maximum output current was important to be measured in the cases with the capacitor in the output. In the following figures it can be seen how the maximum current was obtained using the osciloscope. By obtaining the derivate of the output voltage, it is multiplied by the value of the capacitance added in order to get the value of the current. It can be seen in the following images that the output current is not the same when responding to a possitive edge than to a negative edge from the imput's signal. The maximum from both cases is the one shown in table 1.1.

2 Exercise 2: The Effect of the Noise Margin

Having three different technology integrated circuits, 74HC02, 74HCT02 and 74LS02, we compare the noise margin between them and analyze the possible results when loading them with each other us follow:

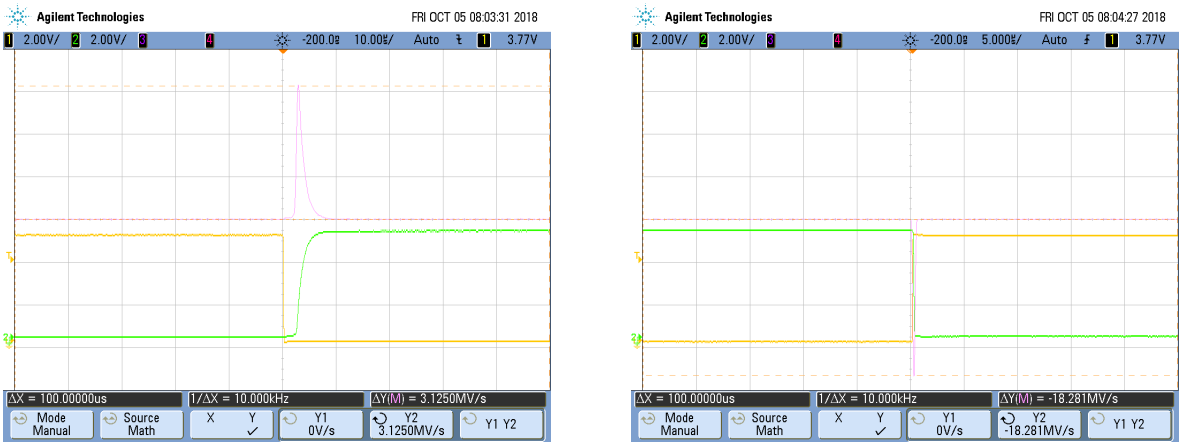

Figure 1.5: NPN Maximun output current

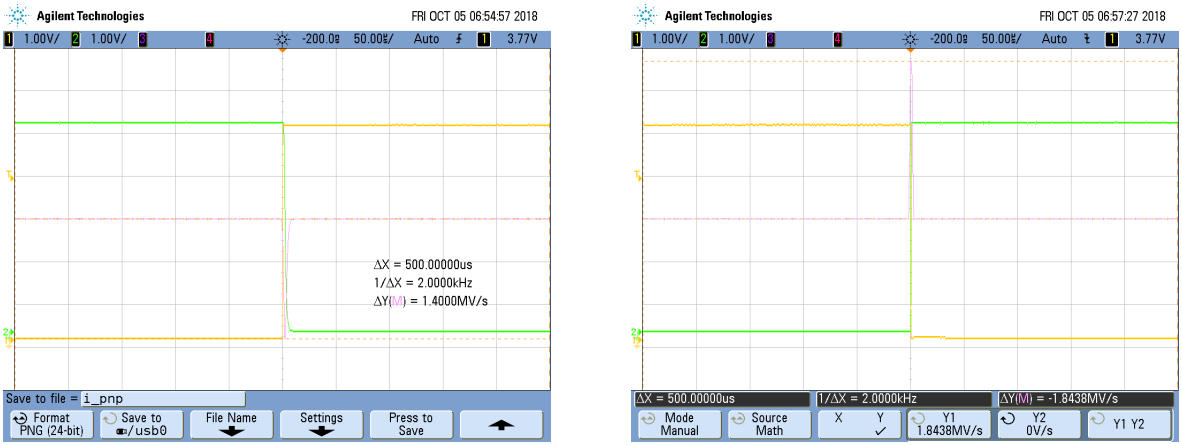

Figure 1.6: PNP Maximun output current

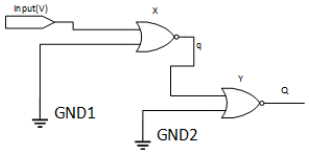

Figure 2.1: Logical circuit

-Input(V): Input voltage; -X: First component name; -Y: Second component name; -q: First result voltage; -Q: Final result

2.1 Theoretically

From the data-sheet of the components we obtain the following data when the power supply is $4.5V$ in the 74HC02 and 74HCT02 and around $5V$ for 74LS02:
Within the mentioned values of power supply, the fanout of the components were: 74HC02 and 74HCT02 are 20, with $I_l = \pm 1\mu A$ and $I_o = -20\mu A$; and 74LS02 is 80, with $I_l = 0.1mA$ and $I_o = 8mA$. As we load the components together, to avoid hurting the circuit, the maximum fanout allow shall be the minimum of the components, this is to say 20 in this case when we load HC with LS or HCT with LS.
Connecting the circuit like the figure **??** being X the second column and Y the forth column, analyzing the possible results would be:

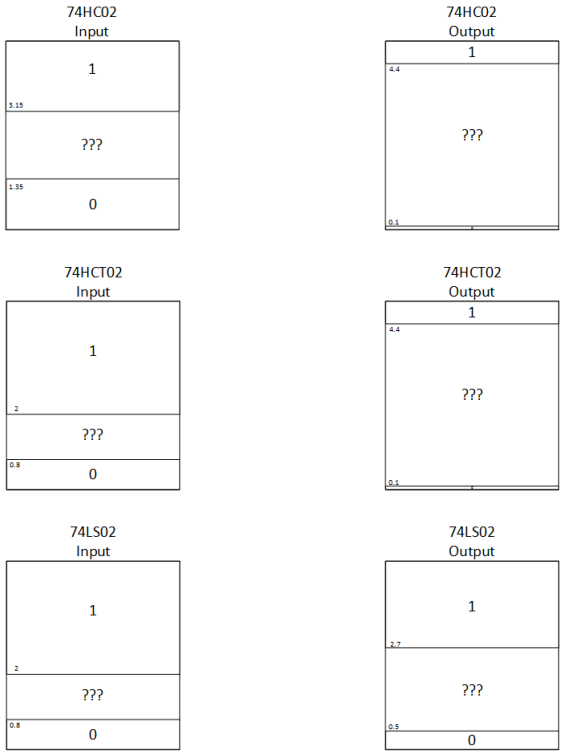

Figure 2.2: Theoretical Noise Margin in Input and Output

Input(V)	74HC02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<1.35	0	1	4.4<V<5	1	0	0<V<0.5
1.35<V<3.15	?	?	0<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
3.15<V<5	1	0	0<V<0.1	0	1	2.7<V<5

Table 2.1: 74HC02 load to 74LS02

Input(V)	74LS02		q	74HC02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<3.15	?	?	0.1<V<4.4
			3.15<V<5	1	0	0<V<0.1
0.8<V<2	?	?	0.5<V<1.35	0	1	4.4<V<5
			1.35<V<2.7	?	?	0.1<V<4.4
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 2.2: 74LS02 load to 74HC02

Input(V)	74LS02		q	74HCT02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<5	1	0	4.4<V<5
0.8<V<2	?	?	0.5<V<0.8	0	1	4.4<V<5
			0.8<V<2	?	?	0.1<V<4.4
			2<V<2.7	1	0	0<V<0.1
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 2.3: 74LS02 load to 74HCT02

Input(V)	74HCT02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	4.4<V<5	1	0	0<V<0.5
0.8<V<2	?	?	0.1<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
2<V<5	1	0	0<V<0.1	0	1	2.7<V<5

Table 2.4: 74HCT02 load to 74LS02

Therefore we expect when loading the components there will be are some irregularities in the Q output value when the input value aren't the recommended in the data-sheet.

2.2 Experimentally

Building the circuit in the figure **??** with the power supply to the integrated circuits equal to 5V with a square signal, altering its maximum value. The measured result were:

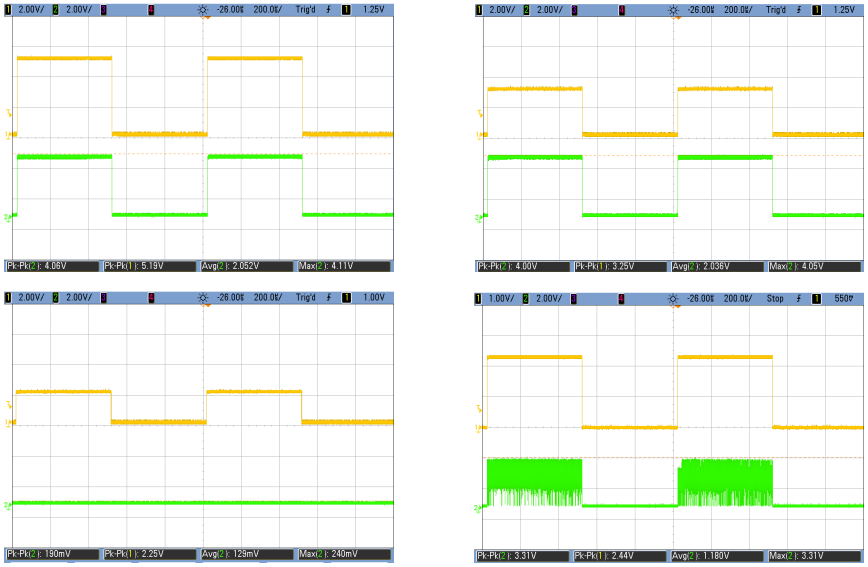

Figure 2.3: 74HC02 load to 74LS02

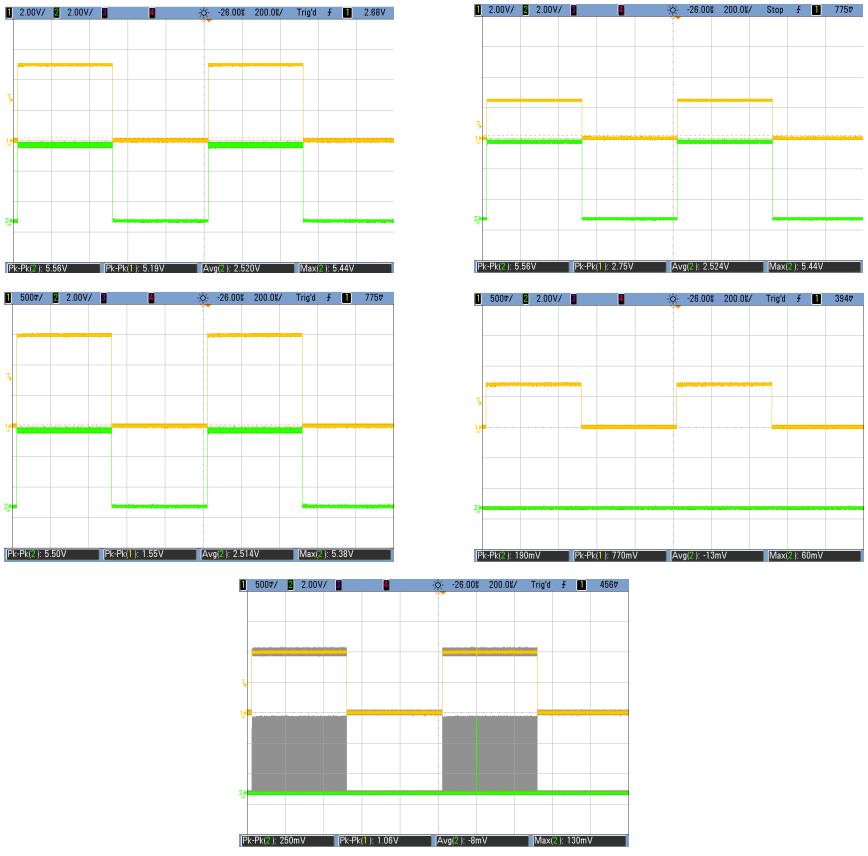

Figure 2.4: 74LS02 load to 74HC02

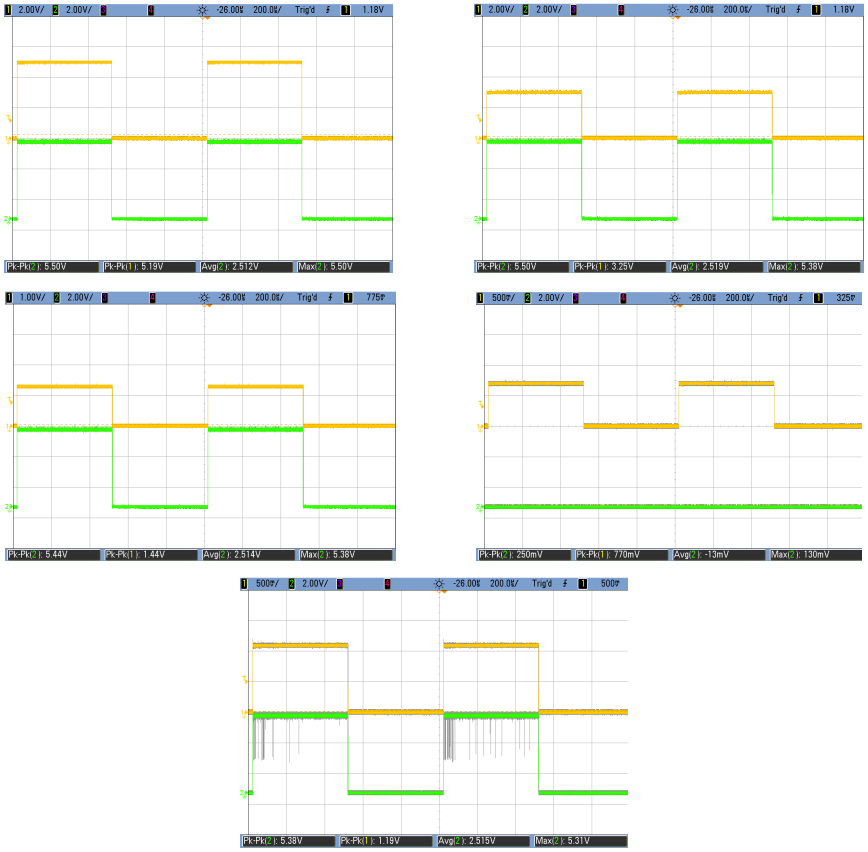

Figure 2.5: 74LS02 load to 74HCT02

Figure 2.6: 74HCT02 load to 74LS02

Analyzing the results in Q it is clear that the irregularities are odd to find, this could be because the manufacturer always leaves a bigger margin to ovoid conflicts within each unique component. Moreover as mention in the theoretical table when the input voltage isn't a logical input, in other words the supply voltage is in the prohibited zone because the circuit cannot decide if the the value of the voltage is low or high, the output value q could mean something in the second component leading to misunderstandings or errors in the logical function. In the other hand, we can notice that using the HCT with the LS integrated circuits, their irregularity is lower in amplitude and not so define as HC with LS, cause their input noise margin are similar.

3 Exercise 3: Simplification and Implementation of a Truth Table

In this section, we will show how using the lower cost technology to implement a truth table, can result in some glitches and issues. For this exercise, we were asked to simplify the truth Table on Table 3.1

A	B	C	O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Table 3.1: Truth Table

When we express this in the form of the Karnaugh map, we'va got the Figure 3.1. As we see there, if we do not take into account the yellow minterm, there are two separate subsets of ones that can represent the Table 3.1. However, as we know, because the two subsets have no element in common, representing this truth tables with just two minterms can cause glitches.
By implementing this wit NAND gates we've got the circuit shown on Figure 3.2.
Finally, when we tried to test the circuit shown, we noticed some glitches of time less than 10 micorseconds, thes glitches are shown on Figure 3.3.
This little negative peaks shouldn't be there since we were changing from one positive state, to another positive state in both cases. To resolve this, we only need to add a third minterm to the equation, and this would be the yellow minterm on Figure 3.1.

4 Exercise 4: Behaviour Analysis of Circuits Including a 74HC02 Gate

The 74HC02 is an integrated circuit of NOR gates. Firstly, the propagation delays and the transition times are measured for this gate in a no-load output condition. Then these parameters are measured in the case in which the gate is connected in the circuit in Figure 4.1.

4.0.1 Propagation and Transition Times' Measurements

In the following table, the results of the mentioned measures are shown. The "loaded with circuit" column of the following table corresponds to the circuit from figure 4.1.

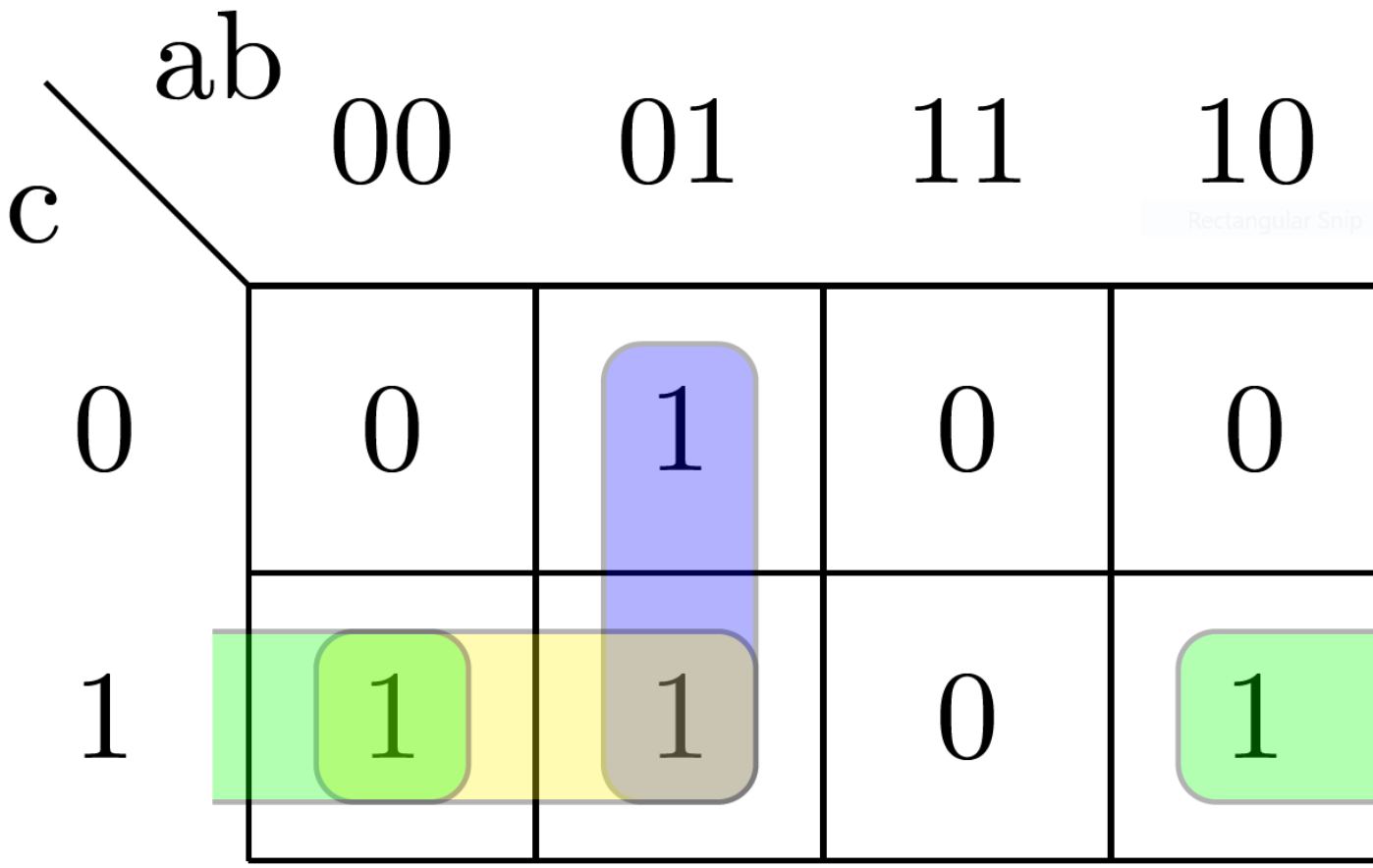

Figure 3.1: Karnaugh's Map

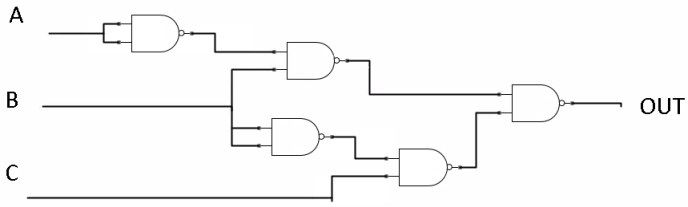

Figure 3.2: NAND Circuit Implementation

	No-load	Loaded with circuit
t_{pHL}	1,5ns	1,05ns
t_{pLH}	12,5ns	14,4ns
t_f	32ns	30,7ns
t_r	41,4ns	43,2ns

Table 4.1: Measurements of propagation delays and transition times.

In the previous table 4.1 it can be seen that the four parameters remain practically the same while being the 74HC02 in the no-load situation and incorporated in the circuit. However, the small differences have

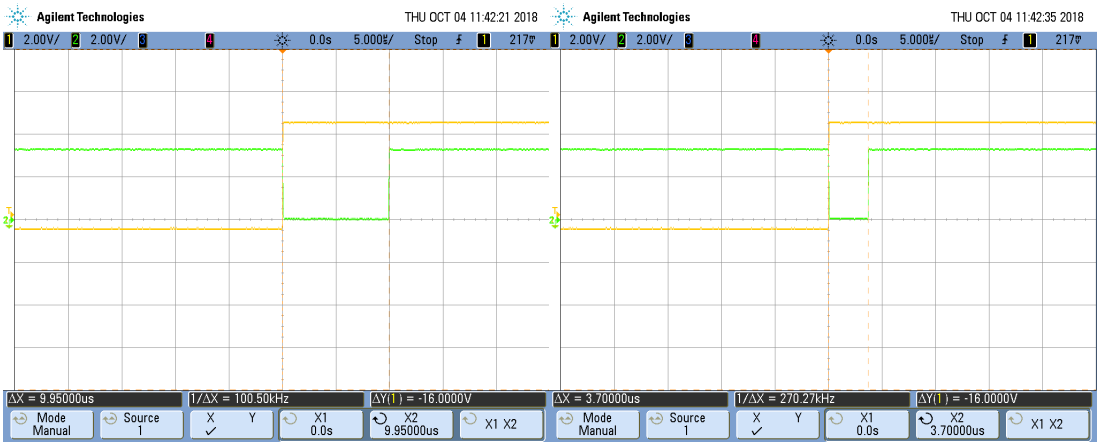

Figure 3.3: Glitches

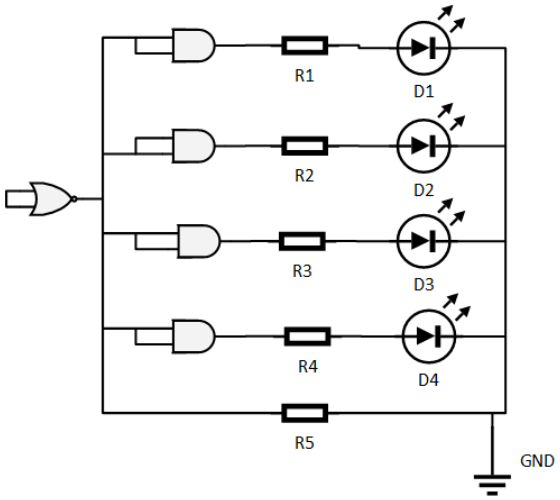

Figure 4.1: 74HC02 connected to a circuit with ANDS and leds.

opposite behaviours depending on the input signal's edge. In the case of a rising edge in the input signal, the propagation delay t_{pLH} and the transition time t_r are bigger if the 74HC02 forms part of the circuit, than if the 74HC02 is in a no-load situation. But the opposite occurs with the falling edge of the input. This is probably caused by the bigger capacitance in the wires and in the components of the circuit.

4.0.2 Circuit's Response to Frequency Increment

No significable temperature changes were noticed in the integrated circuits nor in any component of the entire circuit. The dynamic power is the power dissipated when changing from one state to another. The power discipated by the integrated circuit depends of the input signal's frequency as the dynamic power is $P_D = fCV_{DD}^2$; being f the input frequency, C the circuit's capacitance and V_{DD}=5V. Therefore, a temperature augmentation should be perceived by increasing the frequency from 1Hz to 100kHz. However, no significable temperature changes were noticed in the integrated circuit nor in any component of the entire circuit. Only a small temperature increase was perceived.

4.0.3 Alimentation Voltage of the IC

It is seen in the osciloscope from Figure 4.2 that the alimentation voltage of the circuit in Figure 4.1 has a ripple when there is an edge of the square input signal. This is due to the big ammount of current that the

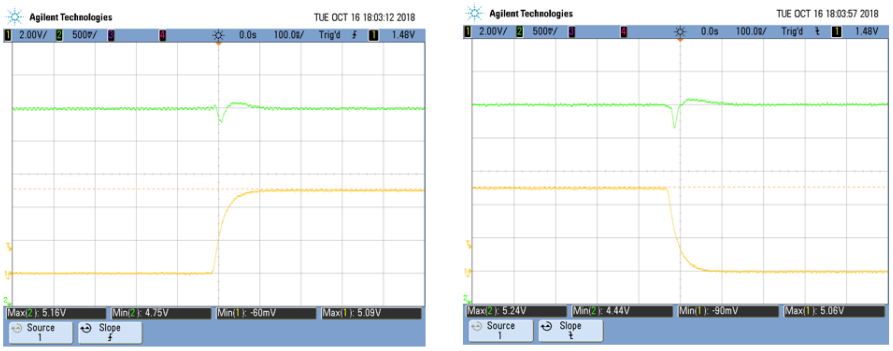

Figure 4.2: Alimentation Voltage of the IC, with a ripple-response to an input signal's edge.

integrated circuit of NOR gates demands from the voltage source when the input signal rises from 0V to 5V or when it falls from 5V to 0V. In order to reduce this "ripple-shape" response of the circuits to such edges, a capacitor has to be added between the +Vcc and the GND terminals of the integrated circuit. The goal is to add a capacitor in a way that the less inductance is added to the circuit. This capacitor has to be the nearest possible to such terminals, to avoid adding long wires that add inductance. Moreover, the best capacitors' technology for this case is the multilayer capacitor as it doesn't add as much inductance as other technologies of this component. As it is preffered to use a multilayer capacitor between 10nF and 100nF for this situation, we decided to use a 100nF capacitor for the ripple to decrease, as it can be seen in Figure 4.3. By adding the capacitor, again, no significant temperature changes are noticed while varying the input signal's frequency, although when the circuit's capacitance increases, the dynamic power varies too.

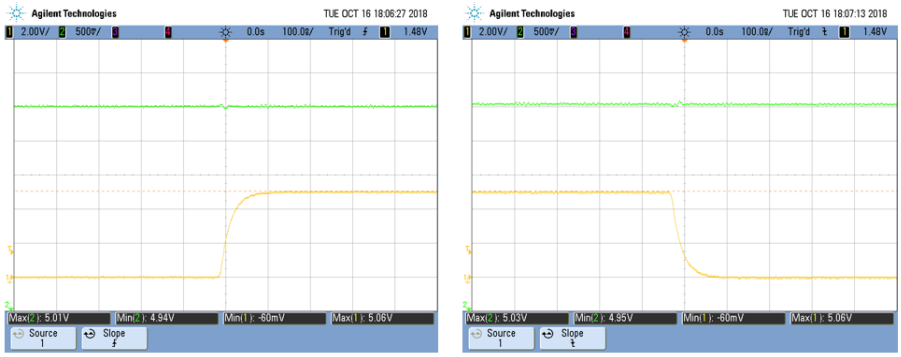

Figure 4.3: Alimentation Voltage of the IC with decoupling capacitor, with a smaller ripple-response to an input signal's edge.

5 Exercise 5: Compatibility between TTL and CMOS

5.1 Floating input in TTL and CMOS

Connecting the following circuit in figure 5.1 and 5.2 leaving one of the inputs floating having $Vcc = 5V$. For the 74LS08, the TTL component, the output port value shown was a logical 1 constantly. On the other hand, the 74HC32, the CMOS component, the results were random with a frequency of 50Hz, having a quadratic function from 0 to 5V or 3 to 5V or a 0 to 0.8V amplitude function.

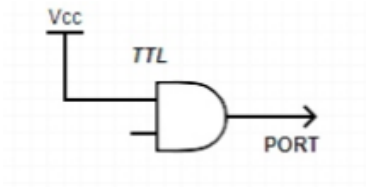

Figure 5.1: Floating TTL

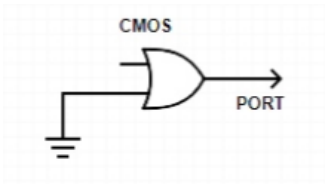

Figure 5.2: Floating CMOS

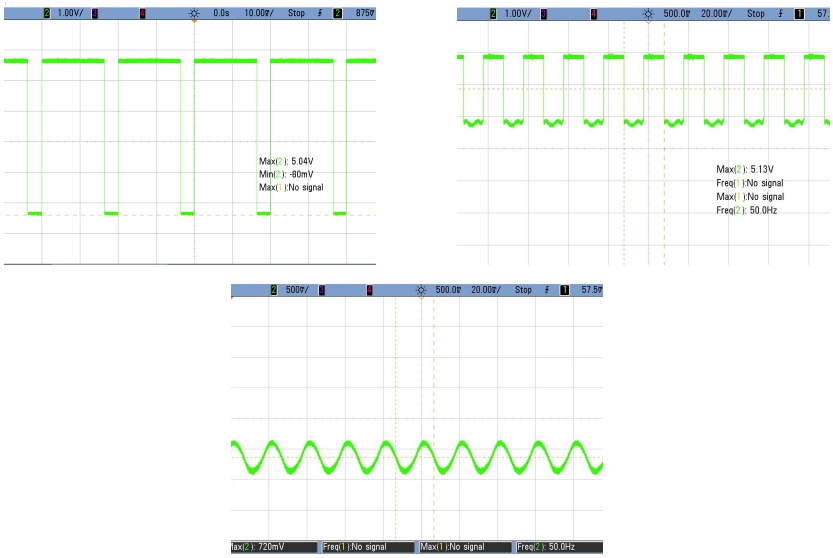

Figure 5.3: 74HC02 load to 74LS02

The reason for this variation in CMOS could be explain by the high impedance at the input making the floating pin induce electric current by noise, creating random values to the output. For this reason, it is recommended in the data-sheet to connect the floating input to the GND or to Vcc depending to the situation, so that unexpected variations wouldn't affect the measurements.

5.2 TTL LOADED TO CMOS

Having the TTL loaded to CMOS as the following figure, with a input value being a quadratic function.

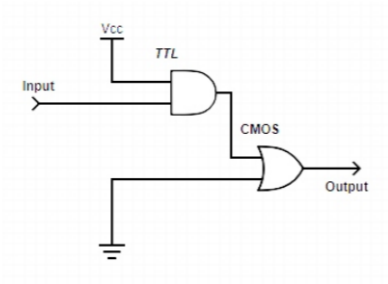

Figure 5.4: TTL loaded to CMOS circuit

When the TTL output value is a logical 1, a voltage from 2.4 to 5V is generated. But there is a problem within this values because the input values for a 1 in CMOS components is from 3.15 to 5V, so in the range of 2.4 to 3.15V the input value for the CMOS is undefined which may causing problems while measuring the two components loaded.

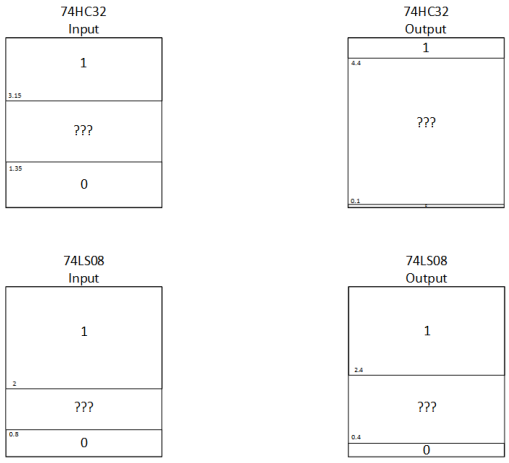

Figure 5.5: Theoretical input and output noise margins

A solution to this problem may be utilizing the same technology components, this is to say using only TTL or CMOS, so that the defined values of the output from the first component is always in range of the input values in the second one. Another solution for this could be utilizing a HCT integrated circuit, a CMOS sub-family, which can make possible the the compatibility between TTL and CMOS by having the following noise margin characteristics.

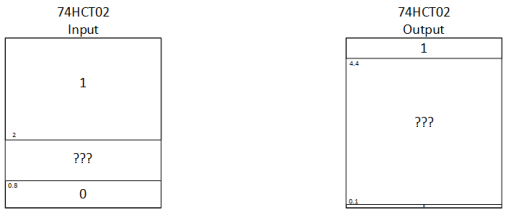

Figure 5.6: HCT noise margins