# 1 Implementation of Flip-Flop D and SR Latch with discrete logic gates

Using the schematic on Figure 1 the logic gates were implemented on a PCB.

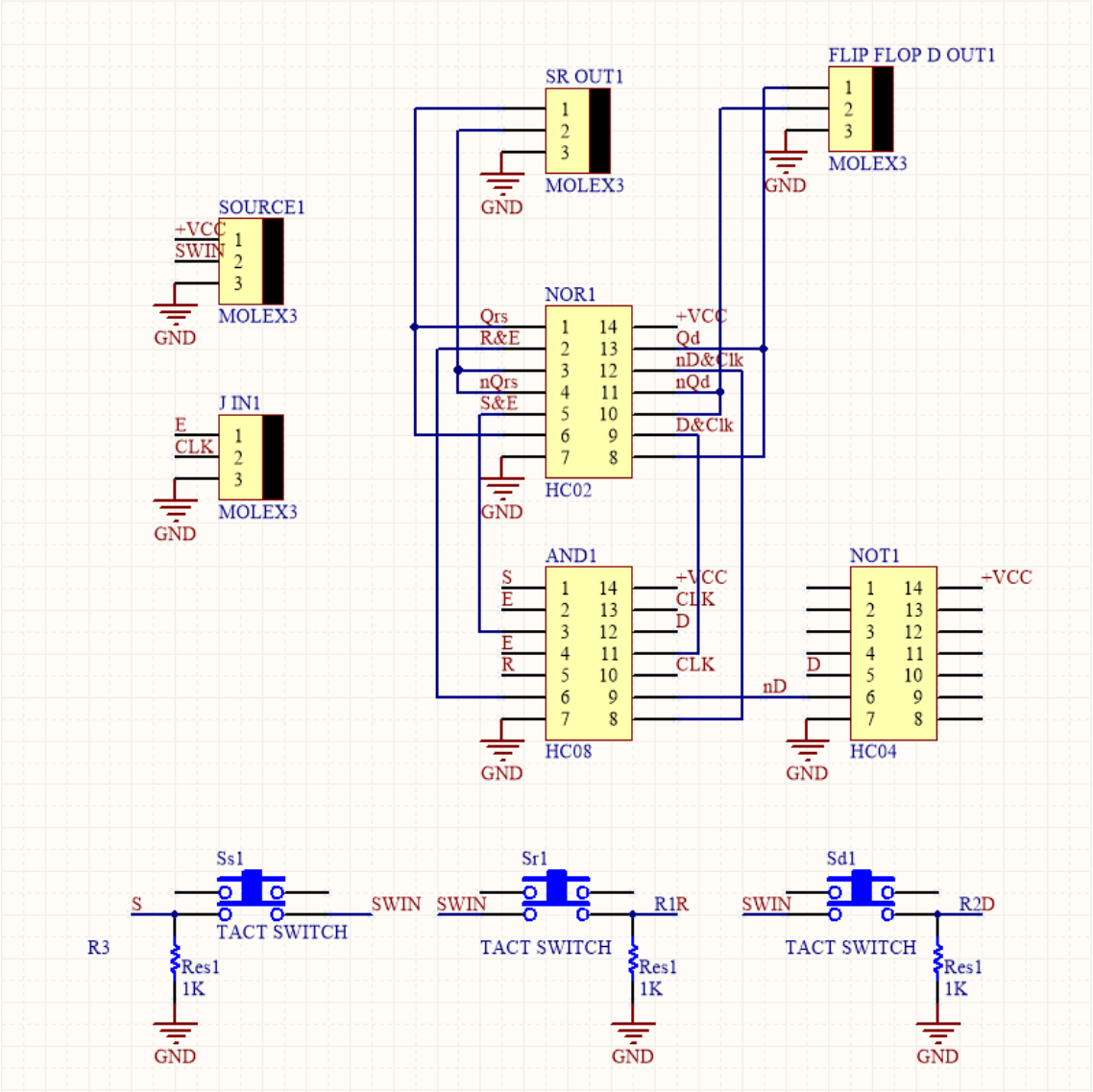


Figure 1: Schematic of the SR Latch (on the left) and Flip-Flop D (on the right)

The resulting circuits were tested and compared to their resulting counterparts as shown in Table 1 and Table 2.

| Symbol | Parameter | 74HC74 | | | Experimental | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply Voltage | 2 | 5 | 6 | 1.5 | 5 | ? | V |
| $V_{IH}$ | High-level input voltage | 3.15 | – | – | 2.64 | – | – | V |
| $V_{IL}$ | Low-level input voltage | – | – | 1.35 | – | – | 2.57 | V |
| $V_I$ | Input voltage | 0 | – | $V_{CC}$ | 0 | – | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | – | $V_{CC}$ | -0.2 | – | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input rise and fall time | – | – | 0.5 | – | – | 16.05 | $\mu$s |
| $V_{OH}$ | High-level output voltage | 3.84 | 4.3 | – | 3,725 | $V_{CC}$ | – | V |
| $V_{OL}$ | Low-level output voltage | – | 0.17 | 0.4 | – | -0.2 | 1.0875 | V |
| $t_{pd}$ | Phase Difference | – | 20 | 44 | – | 28 | 380 | ns |

Table 1: Comparison of measured circuit characteristics for the Flip-Flop D

| Symbol | Parameter | SN54279 | | | Experimental | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | MIN | N/T | MAX | MIN | N/T | MAX | |
| $V_{CC}$ | Supply Voltage | 4.75 | 5 | 5.25 | 0.7 | 5 | ? | V |
| $V_{IH}$ | High-level input voltage | 2 | – | – | 3.79 | – | – | V |
| $V_{IL}$ | Low-level input voltage | – | – | 0.8 | – | – | 1.35[1] | V |
| $V_{OH}$ | High-level output voltage | 2.4 | 3.4 | – | 3.88 | 5 | – | V |
| $V_{OL}$ | Low-level output voltage | – | 0.2 | 0.4 | – | 0 | 0.06 | V |
| $t_{pHL}$ | Phase Difference | – | 9 | 15 | – | – | 10 | ns |
| $t_{pLH}$ | Phase Difference | – | 12 | 22 | – | – | 20 | ns |

Table 2: Comparison of measured circuit characteristics for the Latch SR