

Assignment *Nº2*

Electrónica 3 - 2018

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1 EXERCISE 1: DESIGN AND IMPLEMENTATION OF NOT GATES USING TRANSISTORS

The following parameters are important when designing NOT Gates.

1.0.1 HIGH-LEVEL AND LOW-LEVEL INPUT VOLTAGES

The high-level input voltage (V_{IH}) is the minimum input voltage that is considered as high, while the low-level input voltage (V_{IL}) is the maximum input voltage that is considered as low. These values correspond to the values of the input voltage when the output voltage's slope is -1.

1.0.2 HIGH-LEVEL AND LOW-LEVEL OUTPUT VOLTAGES

The high-level output voltage (V_{OH}) is the output voltage that the circuit provides as a high, while the low-level output voltage (V_{OL}) is the output voltage that the circuit provides as a low.

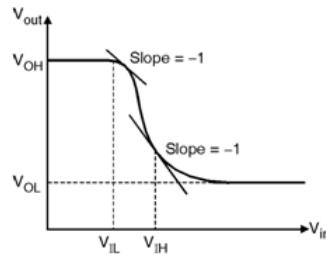


Figure 1.1: High-Level and Low-Level Output and Input Voltages

1.0.3 NOISE MARGIN

The high noise margin (NM_H) is the gap between the high-level input voltage and the high-level output voltage, while the low noise margin (NM_L) is the gap between the low-level output voltage and the low-level input voltage.

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

1.0.4 PROPAGATION DELAYS

When the input changes from low to high and the output from high to low, the high-to-low propagation delay is considered as the time between the moment in which the input voltage reaches the 50% of its maximum high value, until the moment in which the output voltage reaches the 50% of its maximum high value.

$$t_{pHL} = t_{50\%V_{maxO}} - t_{50\%V_{maxI}}$$

In the case in which the input goes from high to low and the output from low to high, the low-to-high propagation delay is considered as the time between the moment in which the input voltage reaches the 50% of its maximum high value, until the moment in which the output voltage reaches the 50% of its maximum high value.

$$t_{pLH} = t_{50\%V_{maxO}} - t_{50\%V_{maxI}}$$

1.0.5 TRANSITION TIMES

The high-to-low transition time or fall time (t_f) is the time that it takes the output voltage to go from its high maximum value to its low minimum value, while the low-to-high transition time or rise time (t_r) is the time that it takes for it to change from its low minimum value to its high maximum value.

1.0.6 MAXIMUM OUTPUT CURRENT

The maximum output current the circuit provides when there is a capacitor, is calculated from the equation:

$$I_C = C \frac{dV_C}{dt}$$

Where the maximum output current of the circuit will take place when there is a change in the voltage, from high to low or low to high.

1.1 NOT GATES' DESIGNS

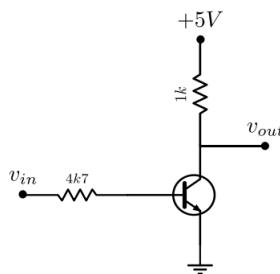


Figure 1.2: NOT Gate Using a NPN Transistor

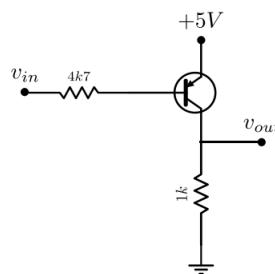


Figure 1.3: NOT Gate Using a PNP Transistor

Figure 1.3 represents a NOT gate built with a BJT NPN 337 transistor, while the circuit in Figure 1.3 corresponds to a NOT gate that uses a BJT PNP 327 transistor. The 4,7kΩ resistors that appear in both circuits were chosen after simulations made with LTspice. We evaluated how the noise margin changed according to this resistor's value. As it is preferred to have a small noise margin because it corresponds to the "prohibited" voltage values, the 4,7kΩ resistor was chosen over bigger values. The simulations were made as it is seen in the following figure. The blue line corresponds to the output voltage. The green line above corresponds to its derivative and the red line has a constant value of -1. This red constant line allowed to find visually quickly the range between both points of intersection with the derivative of the output voltage. These intersections are the cases in which the slope of the output voltage is equal to -1.

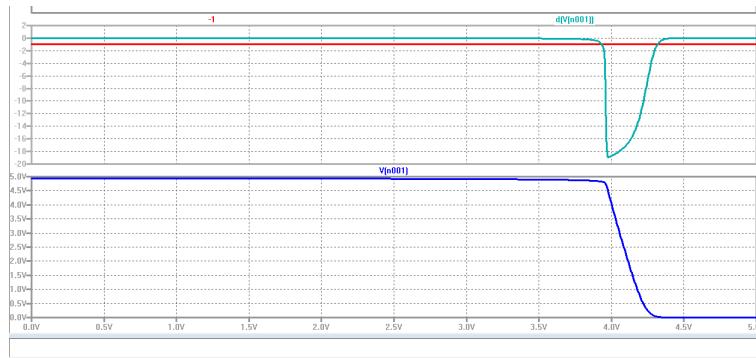


Figure 1.4: Simulation with $4,7\text{k}\Omega$ resistor for the PNP circuit

1.2 MEASUREMENTS

The parameters defined above were measured for each of the circuits in Figures 1.2 and 1.3 in two different conditions: without loading the output and with a $1n\text{F}$ capacitor connected to the output. The results are shown in the following Table 1.1.

	NPN	NPN with capacitor	PNP	PNP with capacitor
$V_{IH}(V)$	0,9	0,9	4,5	4,6
$V_{IL}(V)$	0,5V	0,6	4,2	4,3
$V_{OH}(V)$	4,96V	4,56	4,77	5
$V_{OL}(V)$	0,1	0,12	0,05	0,45
$NM_H(V)$	4,06	3,66	0,27	0,4
$NM_L(V)$	0,4	0,48	4,15	3,85
t_{pHL} (ns)	87	2700	2720	101
t_{pLH} (ns)	2940	104	73	2230
t_f (ns)	69,5	84	575	770
t_r (ns)	505	520	83	86
$I_{OutMax}(mA)$	-	18,28	-	1,8438

Table 1.1: Measurements of voltage levels, noise margins, propagation delays and transition times.

Note: The maximum output current was important to be measured in the cases with the capacitor in the output. In the following figures it can be seen how the maximum current was obtained using the oscilloscope. By obtaining the derivate of the output voltage, it is multiplied by the value of the capacitance added in order to get the value of the current. It can be seen in the following images that the output current is not the same when responding to a positive edge than to a negative edge from the input's signal. The maximum from both cases is the one shown in table 1.1.

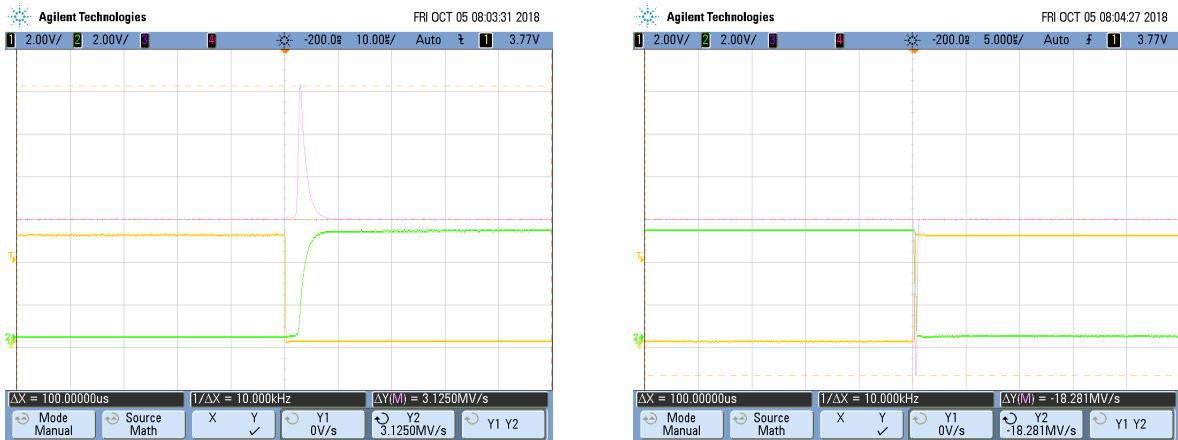


Figure 1.5: NPN Maximum output current

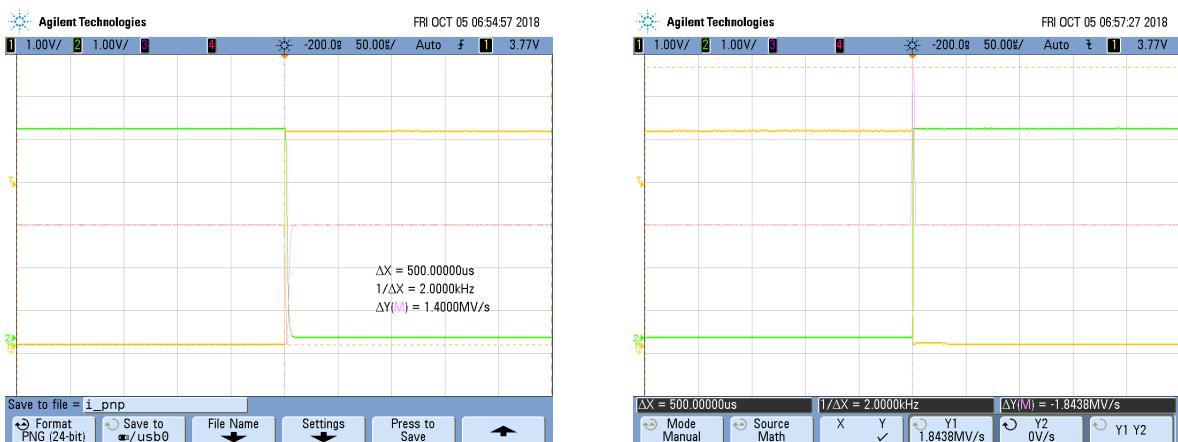


Figure 1.6: PNP Maximum output current

2 EXERCISE 2: THE EFFECT OF THE NOISE MARGIN

Having three different technology integrated circuits (74HC02, 74HCT02 and 74LS02), we compare the noise margin between them and analyze the possible results when loading them with each other as follows:

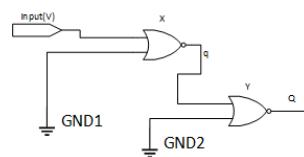


Figure 2.1: Logical circuit

- Input(V): Input voltage;
- X: First component name;
- Y: Second component name;
- q : First result voltage;
- Q: Final result

2.1 THEORETICALLY

From the data-sheet of the components we obtain the following data when the power supply is $4.5V$ in the 74HC02 and 74HCT02 and around $5V$ for 74LS02:

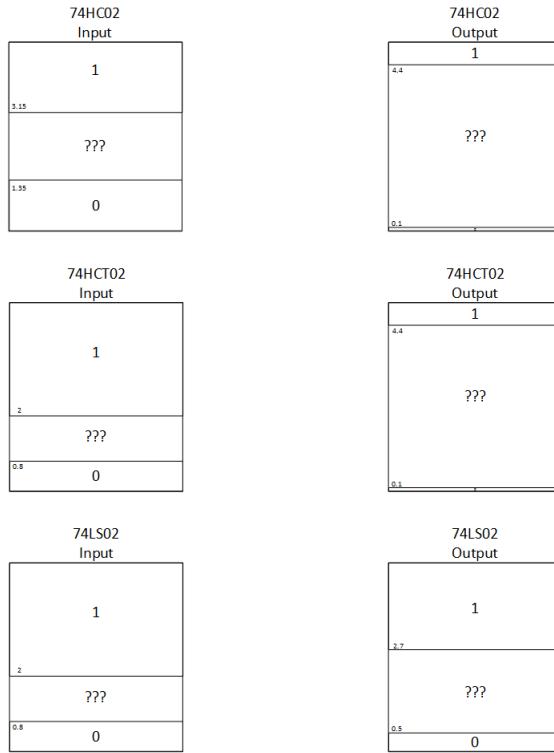


Figure 2.2: Theoretical Noise Margin in Input and Output

Within the mentioned values of power supply, the fanout of the components for 74HC02 and 74HCT02 is 20, with $I_l = \pm 1\mu A$ and $I_o = -20\mu A$; and for 74LS02 is 80, with $I_l = 0.1mA$ and $I_o = 8mA$. As we load the components together, to avoid damaging the circuit, the maximum fanout allowed shall be the minimum of the components, this is to say 20 in this case when we load HC with LS or HCT with LS.

Connecting the circuit like in figure 2.1 being X the second column and Y the forth column, analysing the possible results would be:

Input(V)	74HC02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<1.35	0	1	4.4<V<5	1	0	0<V<0.5
1.35<V<3.15	?	?	0<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
			0<V<0.1	0	1	2.7<V<5

Table 2.1: 74HC02 load to 74LS02

Input(V)	74LS02		q	74HC02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<3.15	?	?	0.1<V<4.4
			3.15<V<5	1	0	0<V<0.1
0.8<V<2	?	?	0.5<V<1.35	0	1	4.4<V<5
			1.35<V<2.7	?	?	0.1<V<4.4
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 2.2: 74LS02 load to 74HC02

Input(V)	74LS02		q	74HCT02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<5	1	0	4.4<V<5
0.8<V<2	?	?	0.5<V<0.8	0	1	4.4<V<5
			0.8<V<2	?	?	0.1<V<4.4
2<V<5	1	0	2<V<2.7	1	0	0<V<0.1
			0<V<0.5	0	1	4.4<V<5

Table 2.3: 74LS02 load to 74HCT02

Input(V)	74HCT02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	4.4<V<5	1	0	0<V<0.5
0.8<V<2	?	?	0.1<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
2<V<5	1	0	2<V<4.4	1	0	0<V<0.5
			0<V<0.1	0	1	2.7<V<5

Table 2.4: 74HCT02 load to 74LS02

Therefore, we expect, when loading the components, irregularities in the Q output value when the input value isn't the recommended in the data-sheet.

2.2 EXPERIMENTALLY

Building the circuit in the figure 2.1, with a square 0-5V signal, the measured results are:

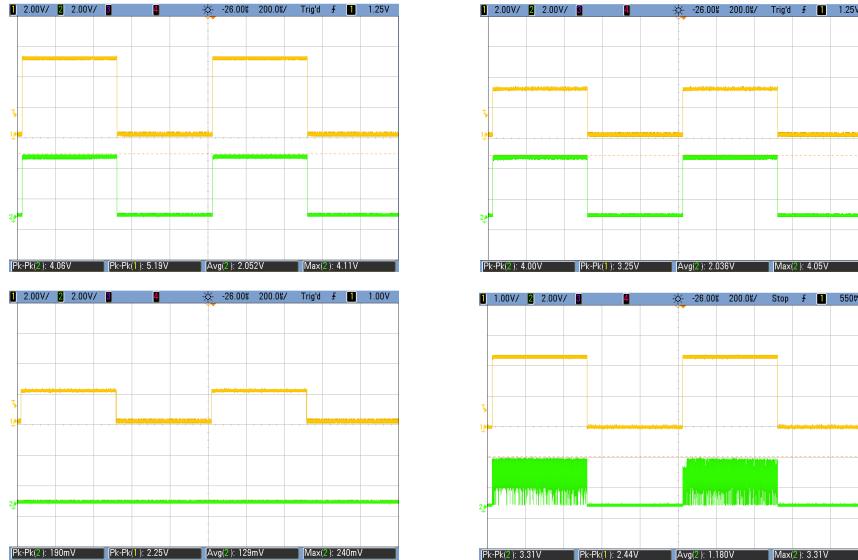


Figure 2.3: 74HC02 load to 74LS02

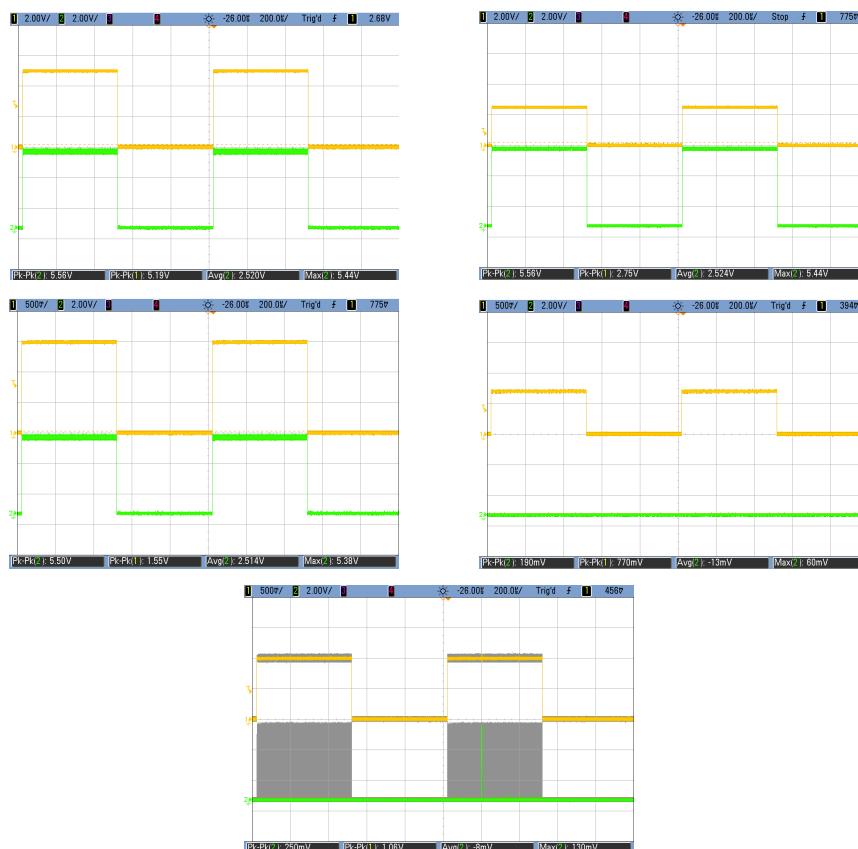


Figure 2.4: 74LS02 load to 74HC02

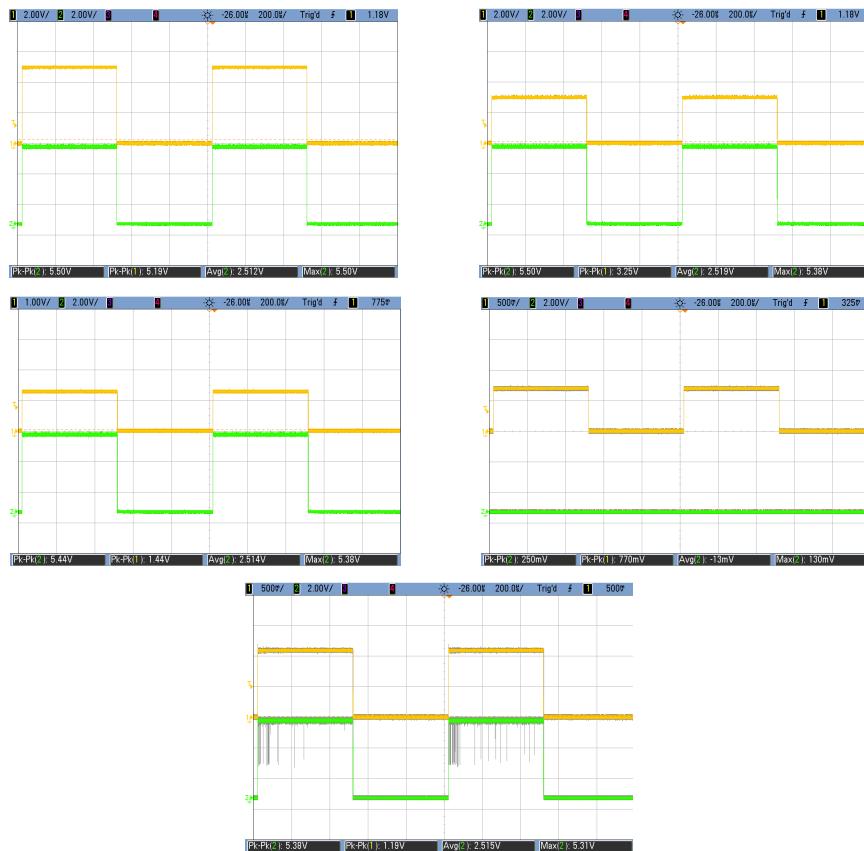


Figure 2.5: 74LS02 load to 74HCT02



Figure 2.6: 74HCT02 load to 74LS02

Analysing the results in Q it is clear that the irregularities are odd to find, this could be because the manufacturer always leaves a bigger margin to avoid conflicts within each component. Moreover, as mentioned in the theoretical table when the input voltage isn't a logical input, the supply voltage is in the prohibited zone because the circuit cannot decide if the value of the voltage is low or high, the output value q could mean something in the second component leading to misunderstandings or errors in the logical function. On the other hand, we can notice that using the HCT with the LS integrated circuits, their irregularity is lower in amplitude and not so defined as HC with LS, because their input noise margins are similar.

3 EXERCISE 3: SIMPLIFICATION AND IMPLEMENTATION OF A TRUTH TABLE

In this section, we will show how using the lower cost technology to implement a truth table, can result in some glitches and issues. For this exercise, we were asked to simplify the truth Table on Table 3.1

A	B	C	O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Table 3.1: Truth Table

When we express this in the form of the Karnaugh map, we've got the Figure 3.1. As we see there, if we do not take into account the yellow minterm, there are two separate subsets of ones that can represent the Table 3.1. However, as we know, because the two subsets have no element in common, representing this truth tables with just two minterms can cause glitches.

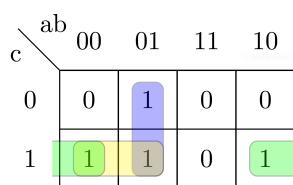


Figure 3.1: Karnaugh's Map

By implementing this with NAND gates we've got the circuit shown on Figure 3.2.

Finally, when we tried to test the circuit shown, we noticed some glitches of time less than 10 micoseconds, these glitches are shown on Figure 3.3.

This little negative peaks shouldn't be there since we were changing from one positive state, to another positive state in both cases. To resolve this, we only need to add a third minterm to the equation, and this would be the yellow minterm on Figure 3.1.

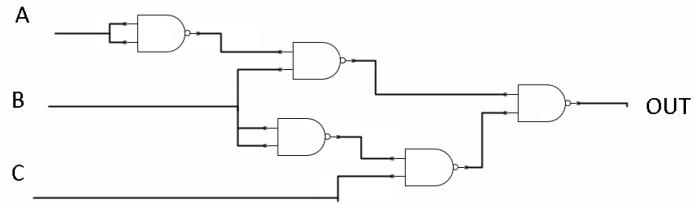


Figure 3.2: NAND Circuit Implementation

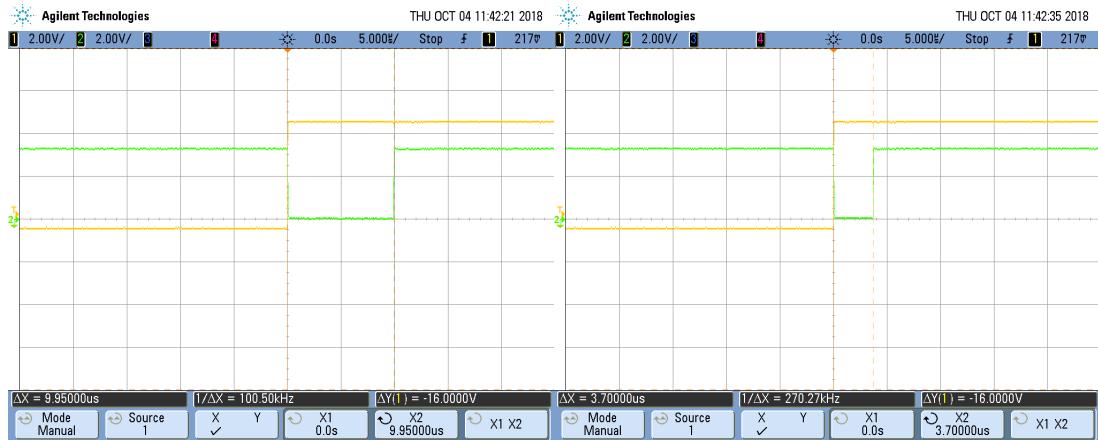


Figure 3.3: Glitches

4 EXERCISE 4: BEHAVIOUR ANALYSIS OF CIRCUITS INCLUDING A 74HC02 GATE

The 74HC02 is an integrated circuit of NOR gates. Firstly, the propagation delays and the transition times are measured for this gate in a no-load output condition. Then these parameters are measured in the case in which the gate is connected in the circuit in Figure 4.1.

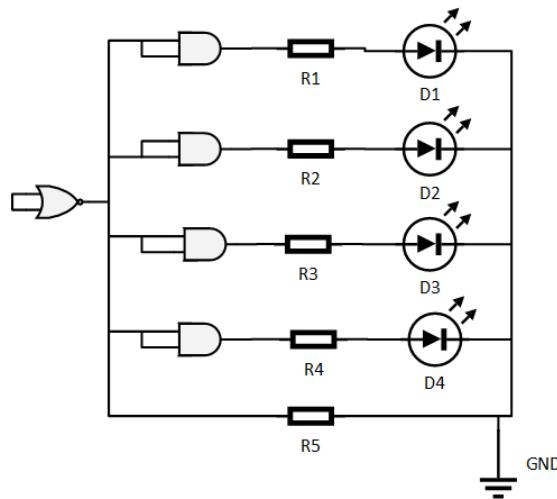


Figure 4.1: 74HC02 connected to a circuit with ANDs and LEDs.

4.0.1 PROPAGATION AND TRANSITION TIMES' MEASUREMENTS

In the following table, the results of the mentioned measures are shown. The "loaded with circuit" column of the following table corresponds to the circuit from figure 4.1.

	No-load	Loaded with circuit
t_{pHL}	1,5ns	1,05ns
t_{pLH}	12,5ns	14,4ns
t_f	32ns	30,7ns
t_r	41,4ns	43,2ns

Table 4.1: Measurements of propagation delays and transition times.

In the previous table 4.1 it can be seen that the four parameters remain practically the same while being the 74HC02 in the no-load situation and incorporated in the circuit. However, the small differences have opposite behaviours depending on the input signal's edge. In the case of a rising edge in the input signal, the propagation delay t_{pLH} and the transition time t_r are bigger if the 74HC02 forms part of the circuit, than if the 74HC02 is in a no-load situation. But the opposite occurs with the falling edge of the input. This is probably caused by the bigger capacitance in the wires and in the components of the circuit.

4.0.2 CIRCUIT'S RESPONSE TO FREQUENCY INCREMENT

No significant temperature changes were noticed in the integrated circuits nor in any component of the entire circuit. The dynamic power is the power dissipated when changing from one state to another. The power dissipated by the integrated circuit depends of the input signal's frequency as the dynamic power is $P_D = fCV_{DD}^2$; being f the input frequency, C the circuit's capacitance and $V_{DD}=5V$. Therefore, a temperature augmentation should be perceived by increasing the frequency from 1Hz to 100kHz. However, no significant temperature changes were noticed in the integrated circuit nor in any component of the entire circuit. Only a small temperature increase was perceived.

4.0.3 ALIMENTATION VOLTAGE OF THE IC



Figure 4.2: Alimentation Voltage of the IC, with a ripple-response to an input signal's edge.

It is seen in the oscilloscope from Figure 4.2 that the alimentation voltage of the circuit in Figure 4.1 has a ripple when there is an edge of the square input signal. This is due to the big amount of current that the

integrated circuit of NOR gates demands from the voltage source when the input signal rises from 0V to 5V or when it falls from 5V to 0V. In order to reduce this "ripple-shape" response of the circuits to such edges, a capacitor has to be added between the +Vcc and the GND terminals of the integrated circuit. The goal is to add a capacitor in a way that the less inductance is added to the circuit. This capacitor has to be the nearest possible to such terminals, to avoid adding long wires that add inductance. Moreover, the best capacitors' technology for this case is the multilayer capacitor as it doesn't add as much inductance as other technologies of this component. As it is preferred to use a multilayer capacitor between 10nF and 100nF for this situation, we decided to use a 100nF capacitor for the ripple to decrease, as it can be seen in Figure 4.3. By adding the capacitor, again, no significant temperature changes are noticed while varying the input signal's frequency, although when the circuit's capacitance increases, the dynamic power varies too.



Figure 4.3: Alimentation Voltage of the IC with decoupling capacitor, with a smaller ripple-response to an input signal's edge.

5 EXERCISE 5: COMPATIBILITY BETWEEN TTL AND CMOS

5.1 FLOATING INPUT IN TTL AND CMOS

Connecting the following circuit in figure 5.1 and 5.2 leaving one of the inputs floating having $V_{cc} = 5V$.

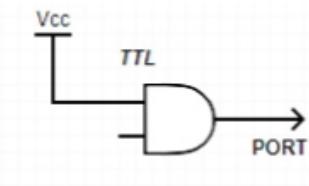


Figure 5.1: Floating TTL

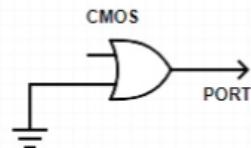


Figure 5.2: Floating CMOS

For the 74LS08, the TTL component, the output port value shown was a logical 1 constantly. On the other hand, the 74HC32, the CMOS component, the results were random with a frequency of 50Hz, having a quadratic function from 0 to 5V or 3 to 5V or a 0 to 0.8V amplitude function.

The reason for this variation in CMOS could be explained by the high impedance at the input making the floating pin induce electric current by noise, creating random values to the output. For this reason, it is recommended in the data-sheet to connect the floating input to the GND or to Vcc depending on the situation, so that unexpected variations wouldn't affect the measurements.

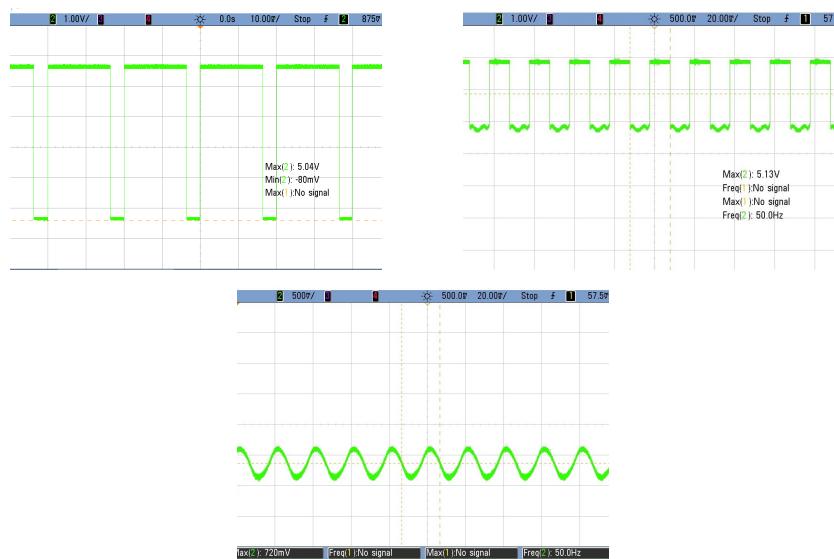


Figure 5.3: 74HC02 load to 74LS02

5.2 TTL LOADED TO CMOS

Having the TTL loaded to CMOS as the following figure, with a input value being a quadratic function.

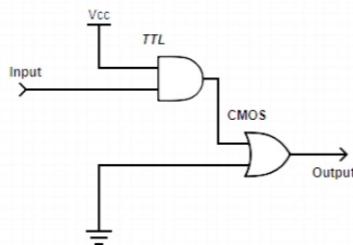


Figure 5.4: TTL loaded to CMOS circuit

When the TTL output value is a logical 1, a voltage from 2.4 to 5V is generated. But there is a problem within this values because the input values for a 1 in CMOS components is from 3.15 to 5V, so in the range of 2.4 to 3.15V the input value for the CMOS is undefined which may causing problems while measuring the two components loaded.

A solution to this problem may be utilizing the same technology components, this is to say using only TTL or CMOS, so that the defined values of the output from the first component is always in range of the input values in the second one. Another solution for this could be utilizing a HCT integrated circuit, a CMOS sub-family, which can make possible the compatibility between TTL and CMOS by having the following noise margin characteristics.

6 EXERCISE 6: IMPLEMENTATION OF FLIP-FLOP D AND SR LATCH WITH DISCRETE LOGIC GATES

Using the schematic on Figure 6 the logic gates were implemented on a PCB.

The resulting circuits were tested and compared to their resulting counterparts as shown in Table 6.1 and Table 6.2.

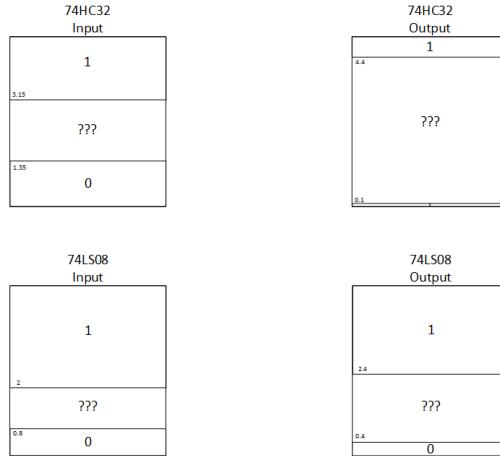


Figure 5.5: Theoretical input and output noise margins

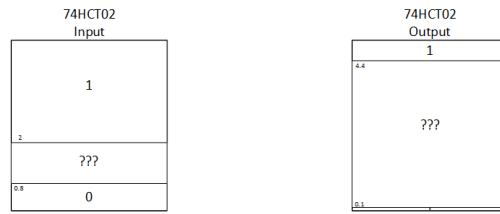


Figure 5.6: HCT noise margins

Symbol	Parameter	SN54279			Experimental			Unit
		MIN	N/T	MAX	MIN	N/T	MAX	
V_{CC}	Supply Voltage	4.75	5	5.25	0.7	5	?	V
V_{IH}	High-level input voltage	2	—	—	3.79	—	—	V
V_{IL}	Low-level input voltage	—	—	0.8	—	—	1.35 ¹	V
V_{OH}	High-level output voltage	2.4	3.4	—	3.88	5	—	V
V_{OL}	Low-level output voltage	—	0.2	0.4	—	0	0.06	V
t_{pHL}	Phase Difference	—	9	15	—	—	10	ns
t_{pLH}	Phase Difference	—	12	22	—	—	20	ns

Table 6.1: Comparison of measured circuit characteristics for the Latch SR

First, in Table 6.1 we can see that the operating conditions of the circuit are vastly different: We can see that, for example, V_{CC} has a wider operating range in the experimental circuit than the Integrated circuit it is compared to. The fact that the fabricated circuit was made from more modern components than the SN54279 might account for this difference in operating conditions. On the other hand, the phase differences are fairly similar for both circuits.

Second, in Table 6.2 there are notable differences on the characteristics of the circuit: the operating voltages are clearly different from those of its commercial counterpart, and the delays between the input and output signals are significantly higher. Given that the fabricated device has wires between each logic gate, it is expected that signals would take longer to travel between each component; therefore, the delay between the

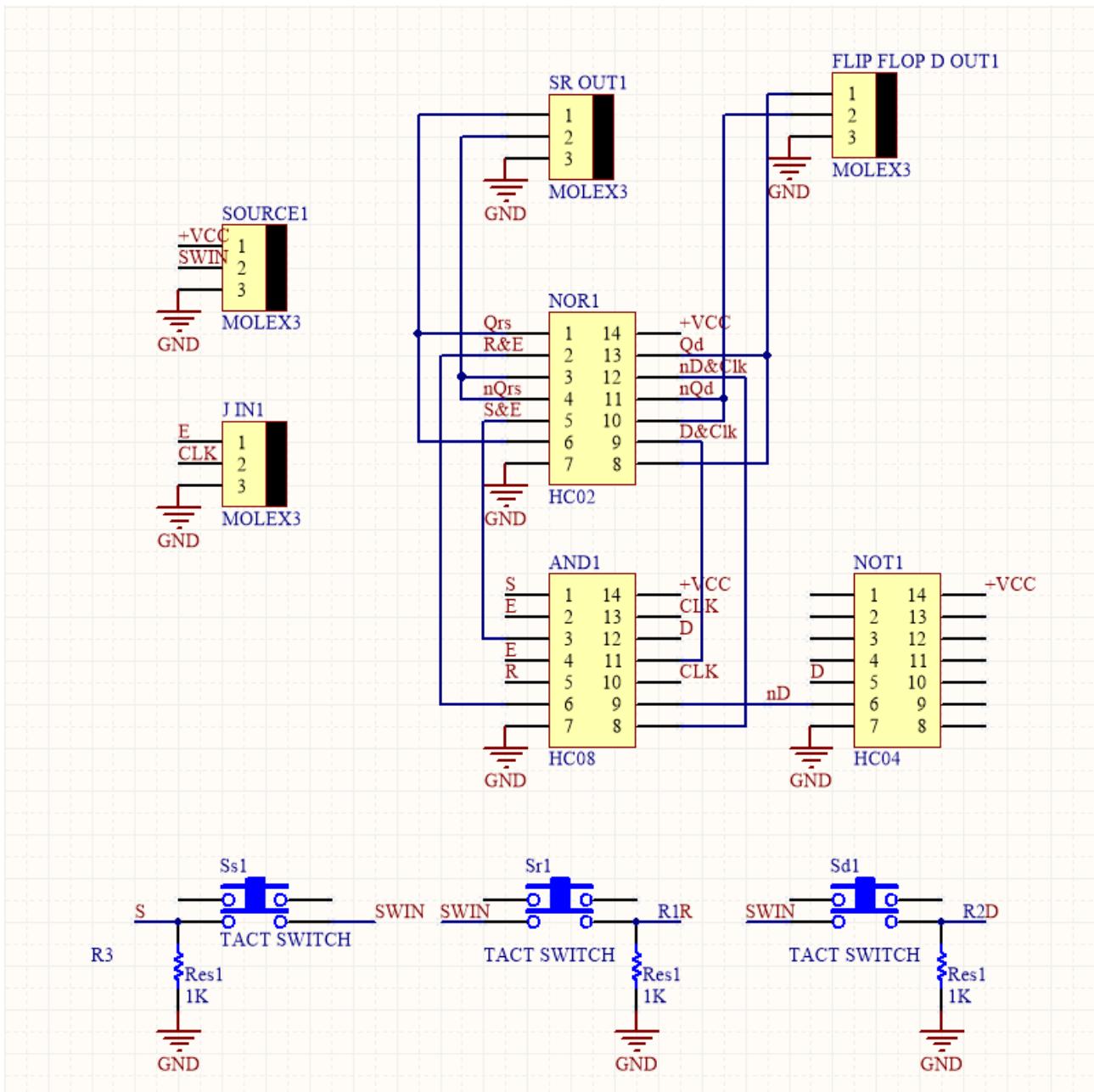


Figure 6.1: Schematic of the SR Latch (on the left) and Flip-Flop D (on the right)

input signal and the output signal will be longer in the experimental circuit than in an Integrated Circuit. From the differences observed in both devices, one can conclude that both experimentally fabricated devices can be used interchangeably with their commercially available counterparts as long as they are not used in highly time-sensitive conditions. Otherwise, when one is working with signals at the order of *MHz* it is advised to use the commercially available equivalents.

7 EXERCISE 7: IMPLEMENTATION OF SYNCHRONOUS AND ASYNCHRONOUS 3-BIT COUNTERS

Using the schematic in Figures 7.1 and 7.2 and the circuits were implemented on a Printed Circuit Board. First, the behaviour of both devices was verified. Line 1 represents the Clk signal while lines 2, 3 and 4

Symbol	Parameter	74HC74			Experimental			Unit
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	2	5	6	1.5	5	?	V
V_{IH}	High-level input voltage	3.15	—	—	2.64	—	—	V
V_{IL}	Low-level input voltage	—	—	1.35	—	—	2.57	V
V_I	Input voltage	0	—	V_{CC}	0	—	V_{CC}	V
V_O	Output voltage	0	—	V_{CC}	-0.2	—	V_{CC}	V
$\Delta t/\Delta v$	Input rise and fall time	—	—	0.5	—	—	16.05	μs
V_{OH}	High-level output voltage	3.84	4.3	—	3.725	V_{CC}	—	V
V_{OL}	Low-level output voltage	—	0.17	0.4	—	-0.2	1.09	V
t_{pd}	Phase Difference	—	20	44	—	28	56	ns

Table 6.2: Comparison of measured circuit characteristics for the Flip-Flop D

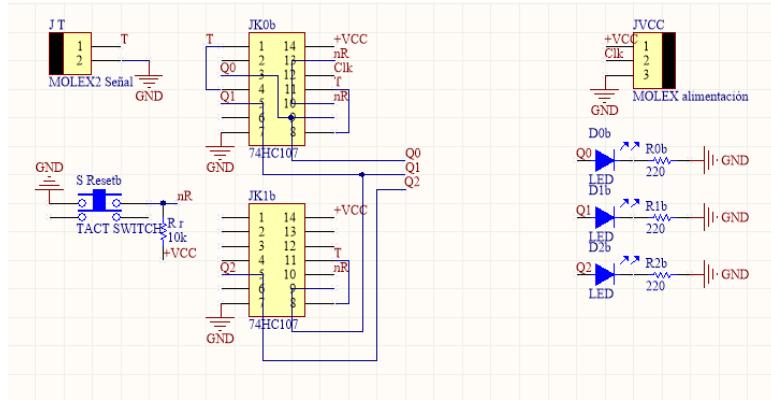


Figure 7.1: Shcematics for the Asynchronous counter

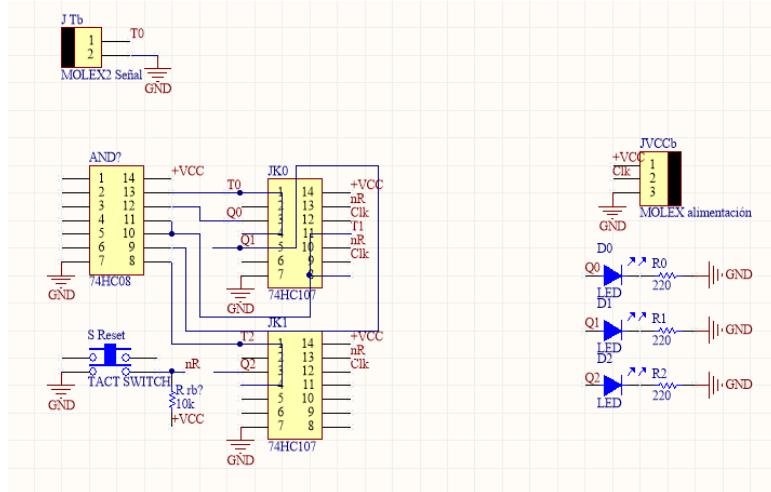


Figure 7.2: Schemas for the Synchronous counter

represent a binary bit in the counter.

It can be observed from Figures 7.3 and 7.4 that at this relatively low frequency, there is no visible difference on the behaviour of both counters. However, upon increasing the frequency and measuring the delays



Figure 7.3: Asynchronous counter test on 10 kHz

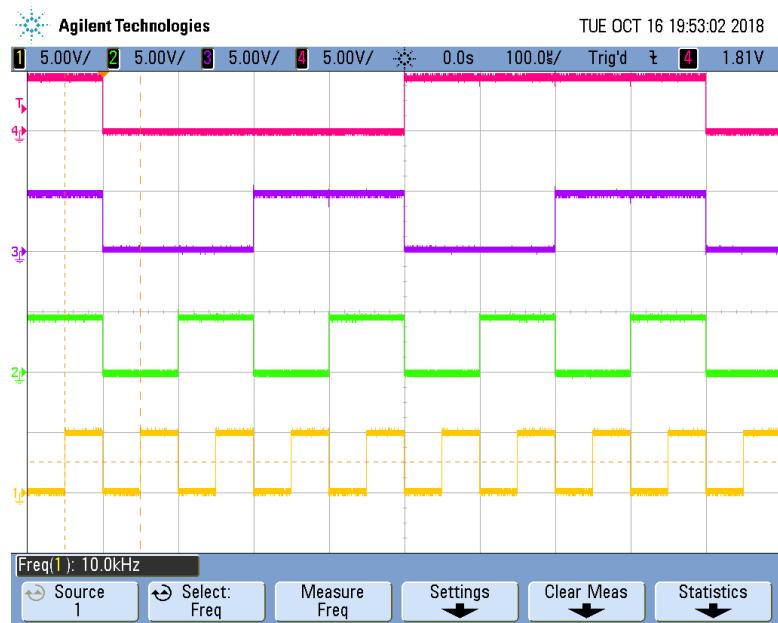


Figure 7.4: Synchronous counter test on 10 kHz

between each negative edge slope, the differences in operation can be observed.

On Figures 7.5 and 7.6 the difference in behaviour can clearly be seen: while on the Asynchronous counter the delay between each subsequent signal is within similar values, in the Synchronous counter there is only significant delay between the clock signal(1) and all the other signals, while between signals 2, 3, and 4, is an order of magnitude lower.

When using the maximum available frequency on both counters, one can see the limitations of the Asynchronous configuration: at this frequency, the clock signal and the 3rd bit signal start to overlap (confirmed by the negative measurement of the delay between them in Figure 7.7), while the Synchronous configuration's waveforms remain without overlap and delays on the positive side of the scale (Figure 7.8).



Figure 7.5: Asynchronous counter test on 1 MHz



Figure 7.6: Synchronous counter test on 1MHz

In conclusion, despite the Asynchronous counter's economical advantage due to the use of fewer components, it runs into the limitation that it will stop working properly at high frequencies, while the Synchronous counter, despite requiring more components, it continues working properly at much higher frequencies.



Figure 7.7: Asynchronous counter test on 20 MHz

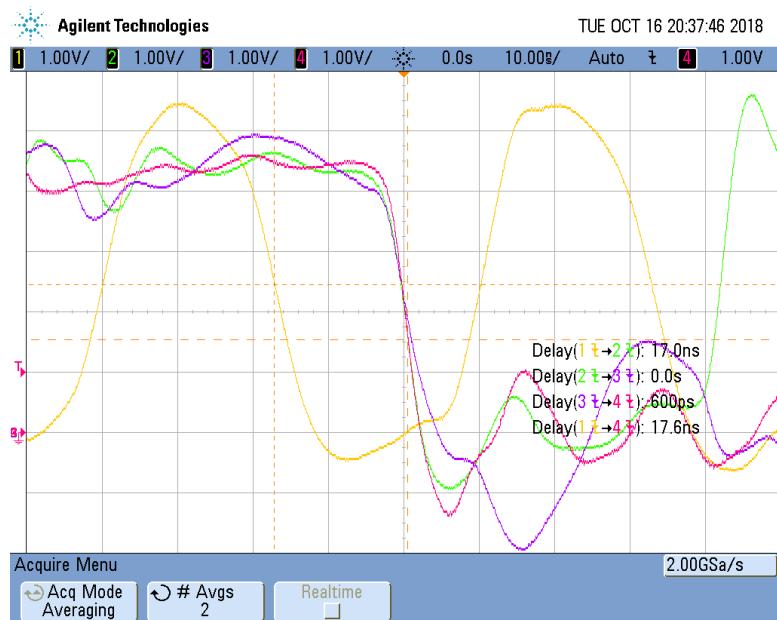


Figure 7.8: Synchronous counter test on 20 MHz

8 EXERCISE 8

In this section we will explain how we developed the PCB that made the sensor HC-SR04 work using only digital electronics.

First of all we have to explain how that sensor works.

8.1 SENSOR OPERATION

This sensor has 4 pins, 2 for supply voltage (VCC and GND), and another pair for control, these are 'Trig' and 'Echo'. The operation of this sensor is pretty simple, you have to send a pulse of time greater than $10\mu s$



Figure 8.1: Sensor HC-SR04

and after some time, it will return into pin Echo, a response pulse of duration that we will call T . If we find a method to measure the time T , we can calculate the distance measured with the following formula.

$$\text{Distance} = \frac{T}{58}$$

It's important to know that the time T has to be in units of μs for the formula to work properly, and *Distance* is in centimeters.

A diagram of this can be found in Figure 8.2

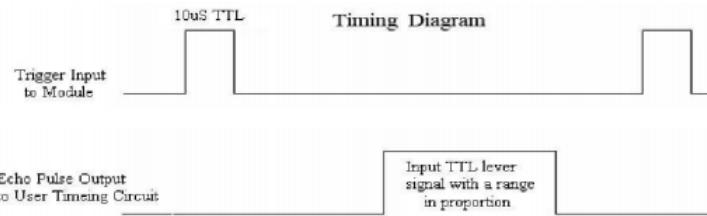


Figure 8.2: Sensor Input and output

8.2 COMPONENTS USED FOR THIS PRINTED CIRCUIT BOARD

For this development we utilized the following Integrated Circuits and components:

- 74HC4040 Counter
- 74HC74 D-type flip-flop
- Two 74HC00 NAND gates
- Two NE555 Precision Timers
- Seven Capacitors
- Sixteen Resistors
- Two Diodes
- Eight Light Emitting Diodes

The disposition of this elements in the PCB will be explained as we understand how we made this work.

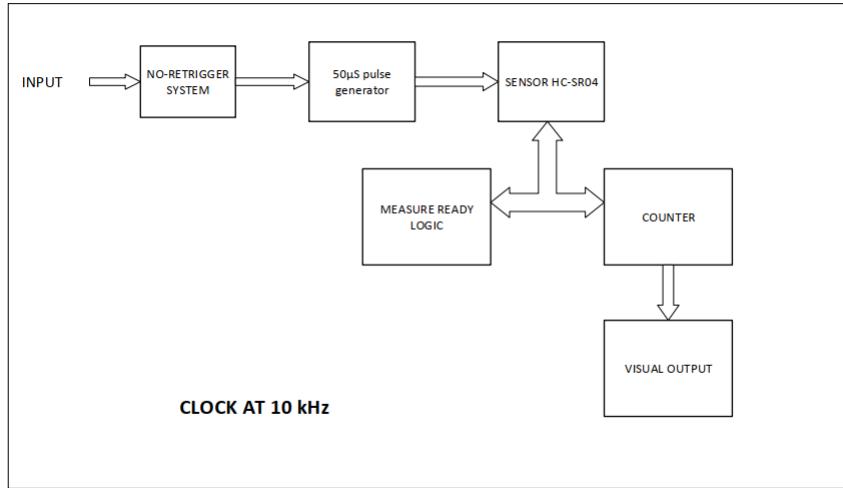


Figure 8.3: PCB diagram

8.3 PCB OPERATION

To make this happen, we develop this board that roughly operates as shown in Figure 8.3

First, we have a No-Retrigger System (NRS) that filters all the retriggered pulses we have because of buttons, that can make our board function in an unappropriate way. Then we generate a $50\mu S$ pulse with the pulse generator, to send to the Trig pin of the sensor. Once we have the response of the sensor, we connect the Echo pin with the counter and the measure ready logic. And finally, we plug a visual output to the counter to see the measurement we have made. Every module seen on this diagram, is powered by a $10kHz$ clock.

8.3.1 NO-RETRIGGER SYSTEM OPERATION

This system is powered by a 74HC74 D-type flip flop that with the proper connections we've changed it to an asynchronous SR Flip-Flop(SRFF). To make this, we connected the SRFF pins as follows:

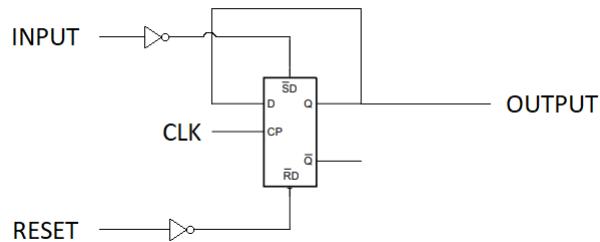


Figure 8.4: No-Retrigger System Connections

By making this connections we made a feedback with the Q and D pins so by every positive-edge clock Q is maintained to its previous value, unless RESET is on. So, summarizing, by connecting the INPUT pin to the input button, and the RESET pin to the reset button, we've created a No-Retrigger System for our board.

8.3.2 50 MICROSECONDS PULSE GENERATOR

Making this pulse generator was a challenge, but we achieved it by creating two submodules into the $50\mu S$ Pulse Generator Module, these are the differentiator circuit, and the pulse generator circuit. Tough the

Differentiator Circuit is placed before the Pulse Generator Circuit (PGC), we will explain first the PGC to better understand the utility of the Differentiator.

PULSE GENERATOR CIRCUIT To power this pulse generator we've used a NE555 Precision Timer, that by connecting it as shown in Figure 8.5, we have made a Pulse generator of the time we wanted.

The formula to obtain the Pulse time at the output is the following

$$T = \ln(3)C3.R2$$

But there is a problem, this pulse generator only works if the input pulse time is less than the time calculated on the previous formula. So if we have a pulse generated by a human that is obviously greater than $50\mu S$ we need a way to make this still work. So here is where the Differentiator Circuit comes to help.

DIFFERENTIATOR CIRCUIT This circuit basically differentiates an input, for us, this means that whenever a pulse is made, a set of dirac's deltas comes out of the circuit, one positive, and another negative. If we define τ as

$$\tau = RC$$

and we choose the appropriate values to the resistor and capacitor to make $5\tau \leq 50\mu S$ we can have a really good differentiator circuit that for every input pulse, it creates an output of less than $50\mu S$, and we can make work our Pulse Generator.

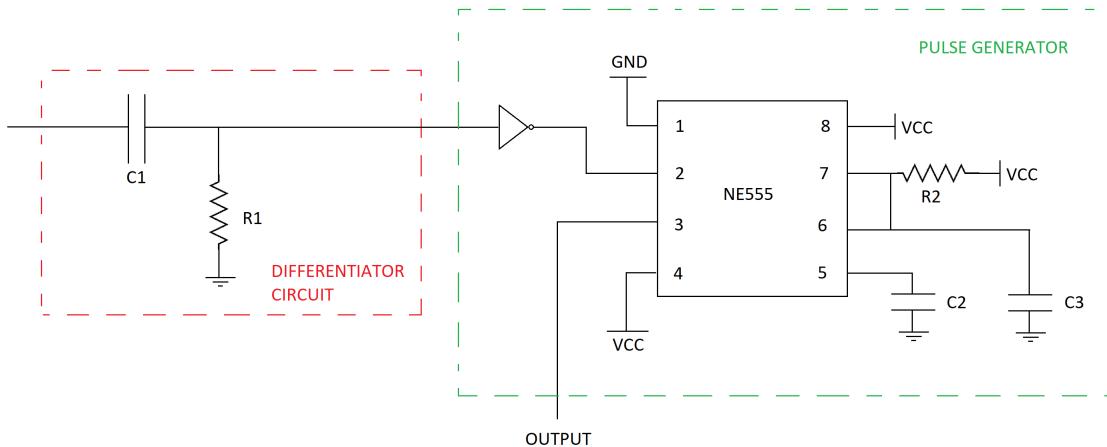


Figure 8.5: Pulse Generator

8.3.3 MEASURE READY LOGIC

The measure ready logic is powered by a 74HC74 D-type flip flop used equally as the No-Retrigger System, and a differentiator circuit almost as equal as the Pulse generator differentiator circuit. But it has one little difference, the 74HC74 is very sensitive to negative voltage, and it can stop working properly according to its datasheet, so we had to add a little protection to erase the negative delta provided by the differentiator circuit. We made this by simply adding a diode that cancels that delta. So the circuit became as shown in the Figure 8.6

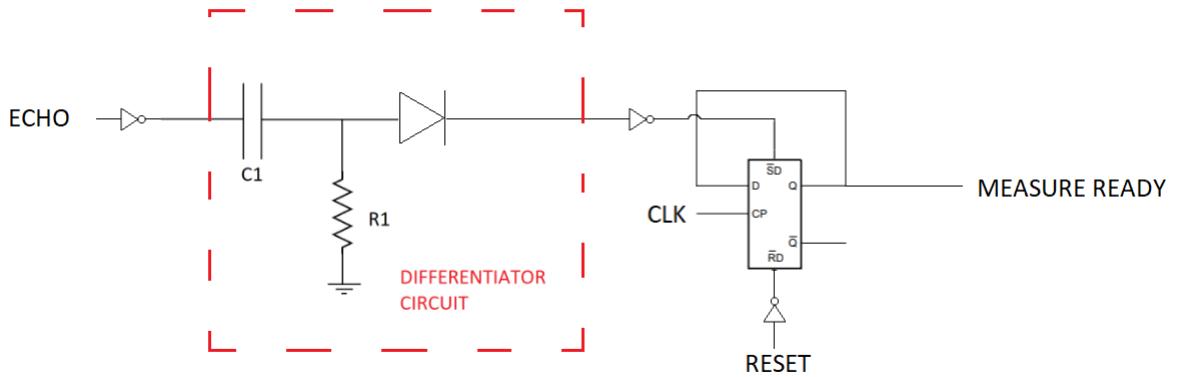


Figure 8.6: Measure Ready Logic

8.3.4 COUNTER

This circuit was relatively easy since we used a 74HC4040 Counter that was really intuitive to use, it was connected as shown in Figure 8.7

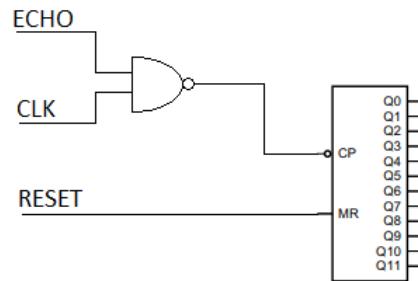


Figure 8.7: Counter

We implemented the NAND before the CP pin to count only when the Echo is on, and when it becomes off, the counter will stop counting.

8.3.5 CLOCK

The clock was performed also with a NE555 and by following the equation

$$f = \frac{1}{T} = \frac{1.44}{(R2 + 2.R1).C3}$$

we made a clock of the period needed. However, due to the resistor and capacitor values we had on the university, we only achieved a T of roughly of $80\mu S$ instead of the $100\mu S$ we wanted. Since it made no such big difference, we left it that way.

VISUAL OUTPUT Finally for this module, we decided to insert a simple array of LEDs displaying in binary code the measurement made by the sensor.

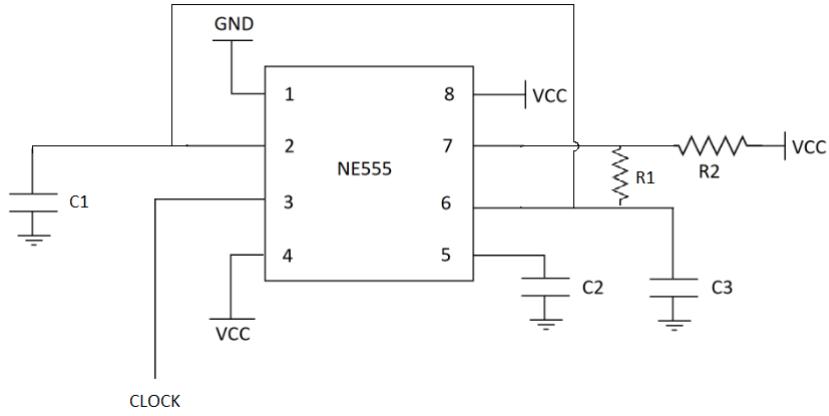


Figure 8.8: Clock

8.4 PCB FABRICATION

To fabricate the design explained before, we used Altium 18 to create the schematic and design the PCB. Because of the amount of things taken into account explained before, we decided to implement a double layer PCB, to make this solution fit in an respectable size. Using the default library provided by Altium and the LIBEBAL library, we created the design shown on Figure 8.9

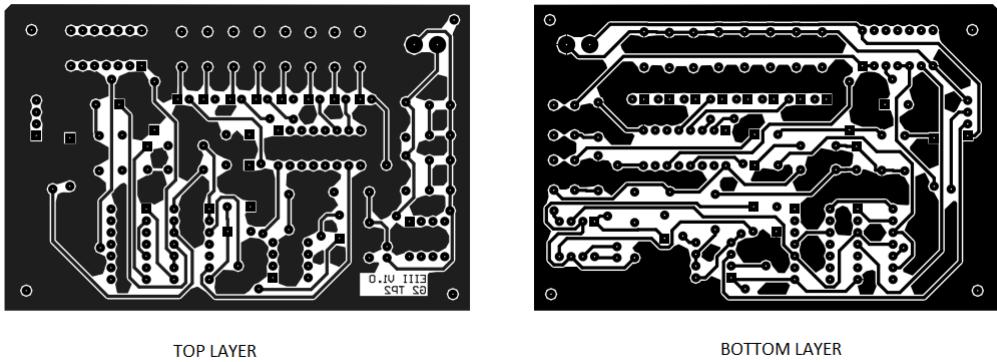


Figure 8.9: PCB Design

8.5 USAGE

To use this solution one simply has to connect the Board to 5V voltage tension, and press the reset button. Once you are ready to measure, press the Input Button and a measurement in binary code will be displayed in the LEDs placed in the PCB. If we call n the number in decimal obtained by the LEDs, we obtain the measurement by following the next equation

$$Distance = \frac{n \cdot 80}{58} (cm)$$

Where the number 80 comes from the clock speed and the 58 from the formula given from the sensor.

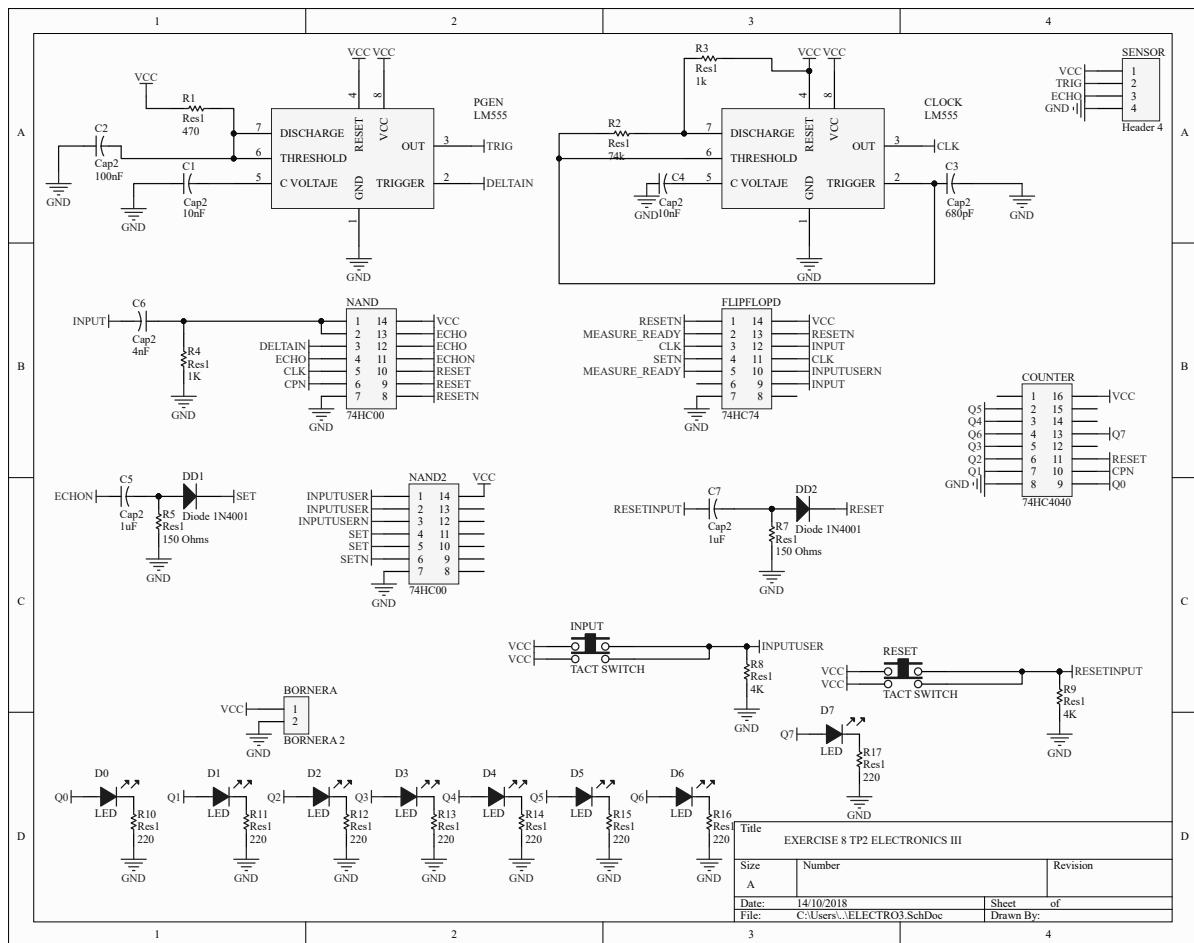


Figure 8.10: PCB Schematic

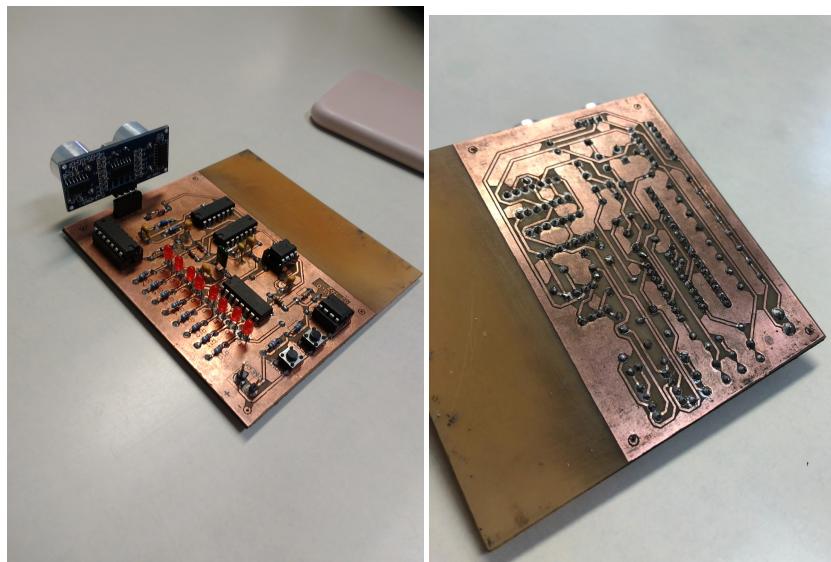


Figure 8.11: PCB Top and Bottom Layer

8.6 SIMULATION

For the simulation a counter with the logic shown on Figure 8.7 and the clock of Figure 8.8 was made. This was accomplished by writing hardware descriptive code on verilo and simulated on GTK wave. The results were as shown on Figure 8.12.

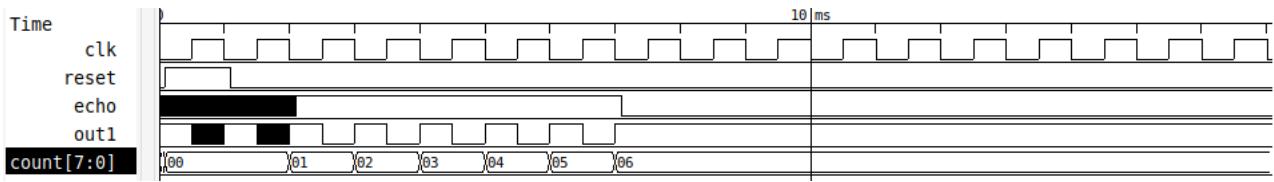


Figure 8.12: [Verilog Simulation](#)

As we've seen, the circuits make what we were expecting, so we conclude that everything should work ok on the real implementation.

8.7 CONCLUSIONS

We conclude that the Board behaves as expected, and by adjusting the formula with 80, we can obtain a relatively great measurement of the distance. Because fabrication and design limitations, we decided not to add the measure ready LED to display that. This was because to human perspective, the measurement is practically instant and adding 2 more components to the PCB was not enough gain to make the trouble. However, the Board to our perspective works perfectly.