1 Implementation of Flip-Flop D and SR Latch with discrete logic gates

Using the schematic on Figure 1 the logic gates were implemented on a PCB.

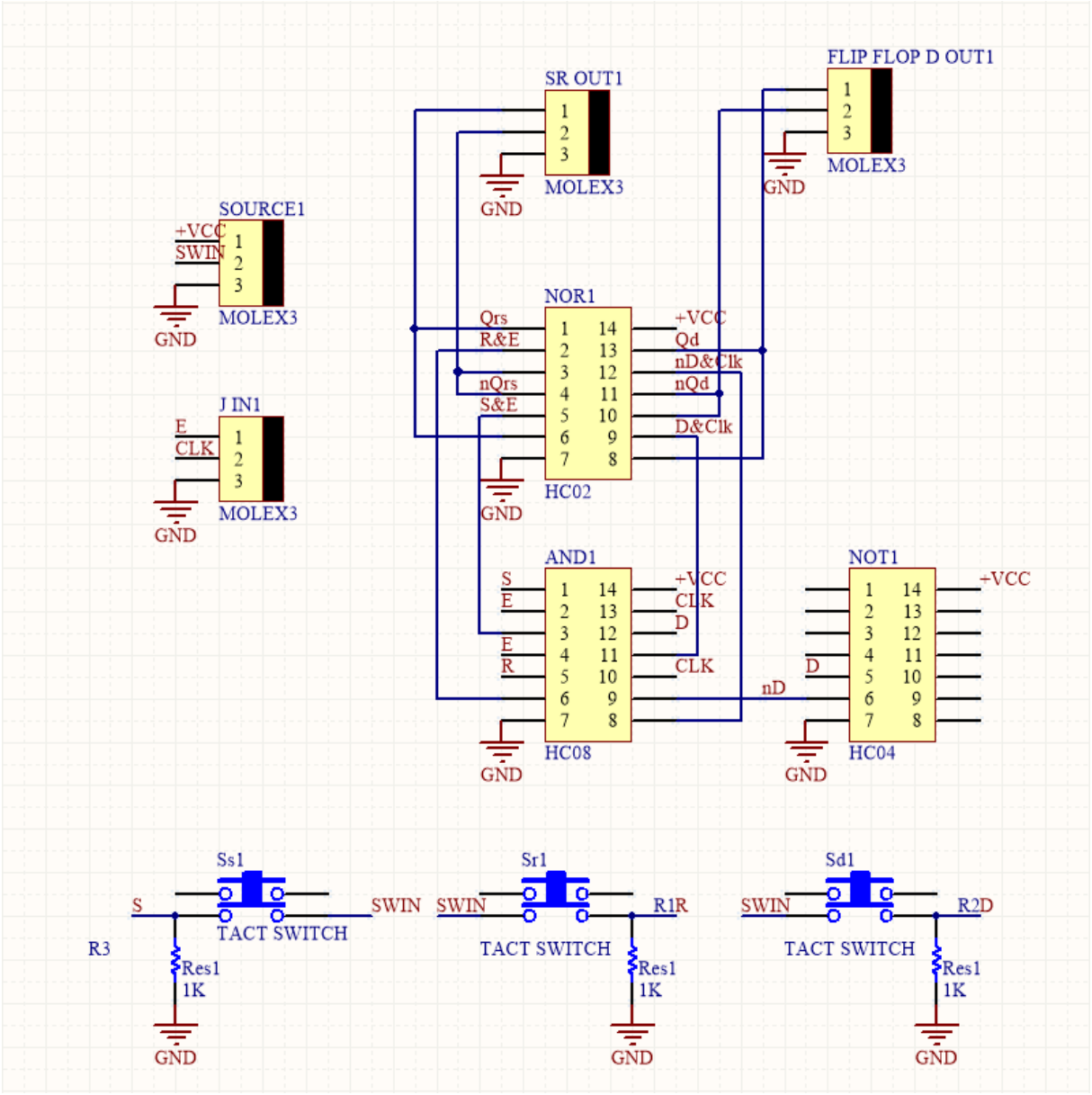

Figure 1: Schematic of the SR Latch (on the left) and Flip-Flop D (on the right)

The resulting circuits were tested and compared to their resulting counterparts as shown in Table 1.

Symbol	Parameter	74HC74			Experimental			Unit
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	2	5	6				V
V_{IH}	High-level input voltage	3.15	–	–		–	–	V
V_{IL}	Low-level input voltage	–	–	1.35	–	–		V
V_I	Input voltage	0	–	V_{CC}		–		V
V_O	Output voltage	0	–	V_{CC}		–		V
$\Delta t/\Delta v$	Input transitionrise and fall time	–	–	500	–	–		ns

Table 1: Operating Conditions comparison