1 Exercise 2: The Effect of the Noise Margin

Having three different technology integrated circuits, 74HC02, 74HCT02 and 74LS02, we compare the noise margin between them and analyze the possible results when loading them with each other us follow:

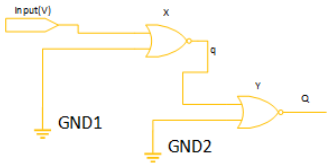

Figure 1.1: Loaded Circuit

Input(V): Input voltage X: First component name Y: Second component name q: First result voltage Q: Final result

1.1 Theoretically

From the datasheet of the components we obtain the following data:

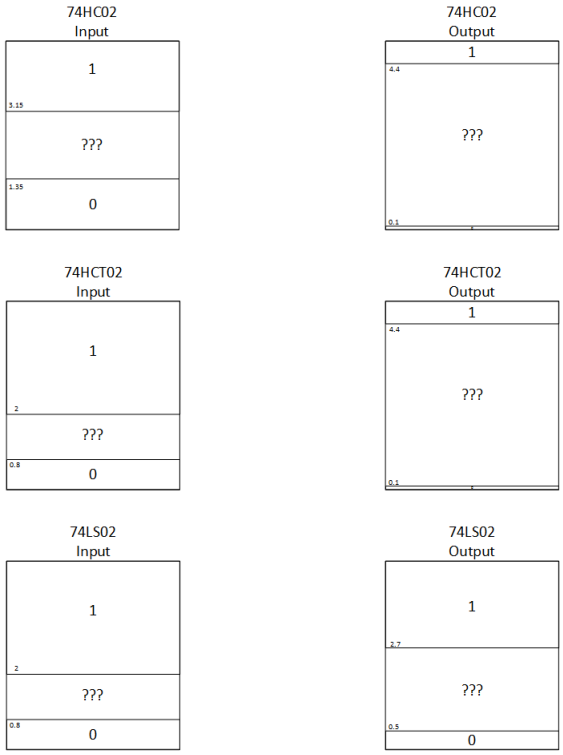

Figure 1.2: Theoretical Noise Margin in Input and Output

Connecting the circuit like the figure 1.1 being X:74HC02 and Y:74LS02, analyzing the possible results we obtain:

	74HC02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<1.35	0	1	4.4<V<5	1	0	0<V<0.5
1.35<V<3.15	?	?	0<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
3.15<V<5	1	0	0<V<0.1	0	1	2.7<V<5

Table 1.1: 74HC02 load to 74LS02

	74LS02		q	74HC02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<3.15	?	?	0.1<V<4.4
			3.15<V<5	1	0	0<V<0.1
0.8<V<2	?	?	0.5<V<1.35	0	1	4.4<V<5
			1.35<V<2.7	?	?	0.1<V<4.4
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 1.2: 74LS02 load to 74HC02

	74LS02		q	74HCT02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<5	1	0	4.4<V<5
0.8<V<2	?	?	0.5<V<0.8	0	1	4.4<V<5
			0.8<V<2	?	?	0.1<V<4.4
			2<V<2.7	1	0	0<V<0.1
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 1.3: 74LS02 load to 74HCT02

	74HCT02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	4.4<V<5	1	0	0<V<0.5
0.8<V<2	?	?	0.1<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
2<V<5	1	0	0<V<0.1	0	1	2.7<V<5

Table 1.4: 74HCT02 load to 74LS02