1 Exercise 2: The Effect of the Noise Margin

Having three different technology integrated circuits, 74HC02, 74HCT02 and 74LS02, we compare the noise margin between them and analyze the possible results when loading them with each other us follow:

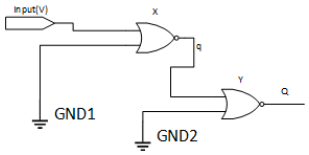

Figure 1.1: Logical circuit

-Input(V): Input voltage; -X: First component name; -Y: Second component name; -q: First result voltage; -Q: Final result

1.1 Theoretically

From the data-sheet of the components we obtain the following data when the power supply is $4.5V$ in the 74HC02 and 74HCT02 and around $5V$ for 74LS02:

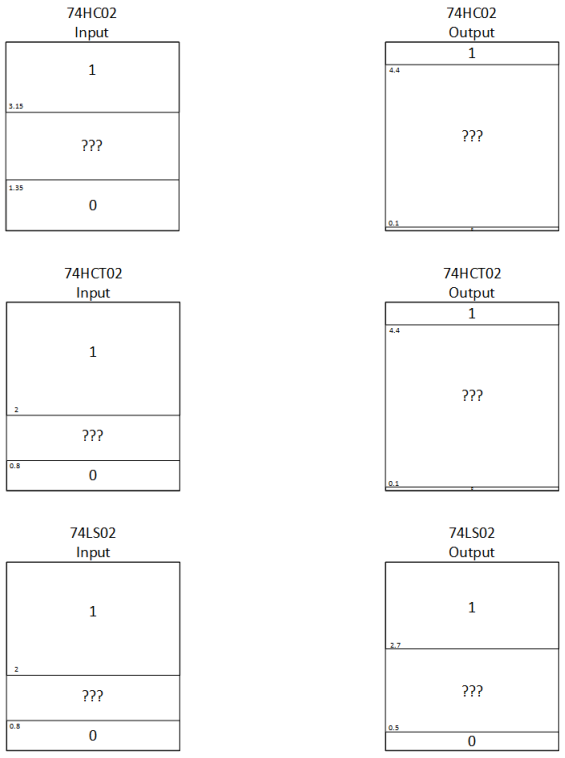

Figure 1.2: Theoretical Noise Margin in Input and Output

Within the mentioned values of power supply, the fanout of the components were: 74HC02 and 74HCT02 are 20, with $I_l = \pm 1\mu A$ and $I_o = -20\mu A$; and 74LS02 is 80, with $I_l = 0.1mA$ and $I_o = 8mA$. As we load the components together, to avoid hurting the circuit, the maximum fanout allow shall be the minimum of the components, this is to say 20 in this case when we load HC with LS or HCT with LS.
Connecting the circuit like the figure **??** being X the second column and Y the forth column, analyzing the possible results would be:

Input(V)	74HC02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<1.35	0	1	4.4<V<5	1	0	0<V<0.5
1.35<V<3.15	?	?	0<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
3.15<V<5	1	0	0<V<0.1	0	1	2.7<V<5

Table 1.1: 74HC02 load to 74LS02

Input(V)	74LS02		q	74HC02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<3.15	?	?	0.1<V<4.4
			3.15<V<5	1	0	0<V<0.1
0.8<V<2	?	?	0.5<V<1.35	0	1	4.4<V<5
			1.35<V<2.7	?	?	0.1<V<4.4
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 1.2: 74LS02 load to 74HC02

Input(V)	74LS02		q	74HCT02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	2.7<V<5	1	0	4.4<V<5
0.8<V<2	?	?	0.5<V<0.8	0	1	4.4<V<5
			0.8<V<2	?	?	0.1<V<4.4
			2<V<2.7	1	0	0<V<0.1
2<V<5	1	0	0<V<0.5	0	1	4.4<V<5

Table 1.3: 74LS02 load to 74HCT02

Input(V)	74HCT02		q	74LS02		Q
	Logic Input	Logic Output		Logic Input	Logic Output	
0<V<0.8	0	1	4.4<V<5	1	0	0<V<0.5
0.8<V<2	?	?	0.1<V<0.8	0	1	2.7<V<5
			0.8<V<2	?	?	0.5<V<2.7
			2<V<4.4	1	0	0<V<0.5
2<V<5	1	0	0<V<0.1	0	1	2.7<V<5

Table 1.4: 74HCT02 load to 74LS02

Therefore we expect when loading the components there will be are some irregularities in the Q output value when the input value aren't the recommended in the data-sheet.

1.2 EXPERIMENTALLY

Building the circuit in the figure **??** with the power supply to the integrated circuits equal to 5V with a square signal, altering its maximum value. The measured result were:

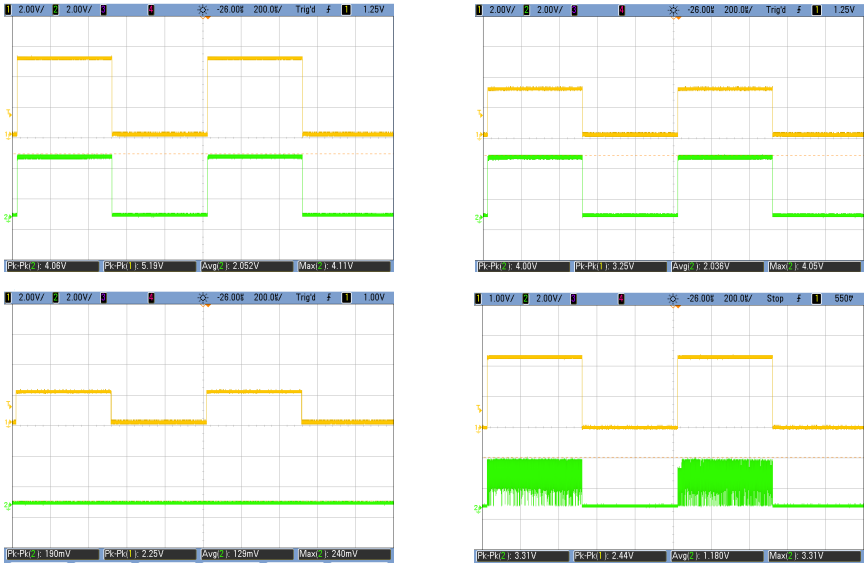

Figure 1.3: 74HC02 load to 74LS02

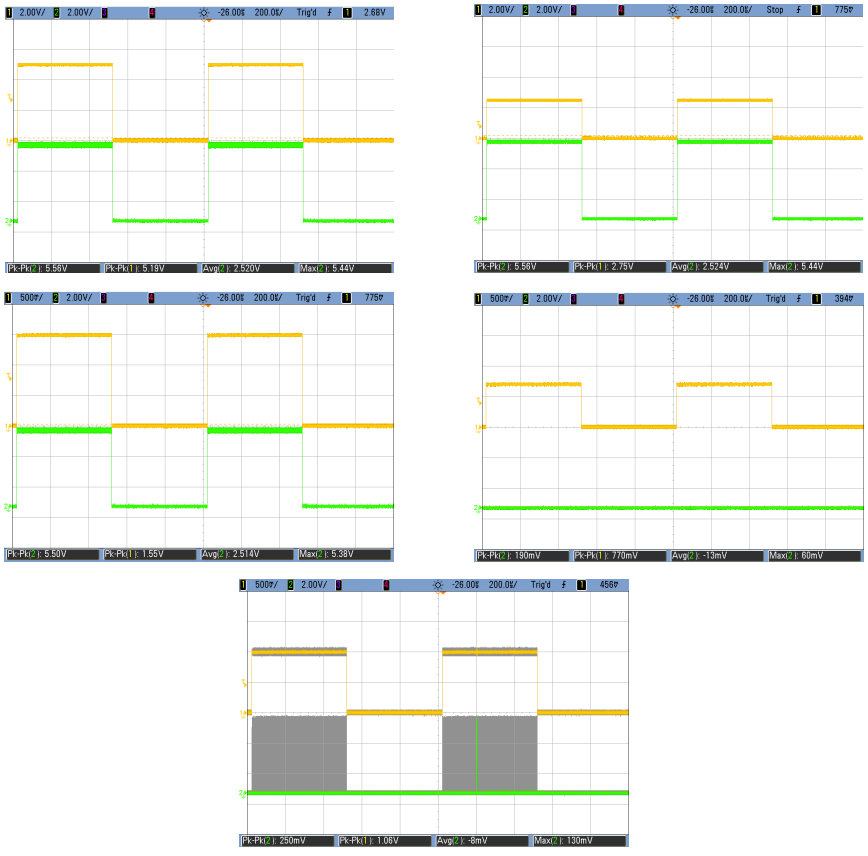

Figure 1.4: 74LS02 load to 74HC02

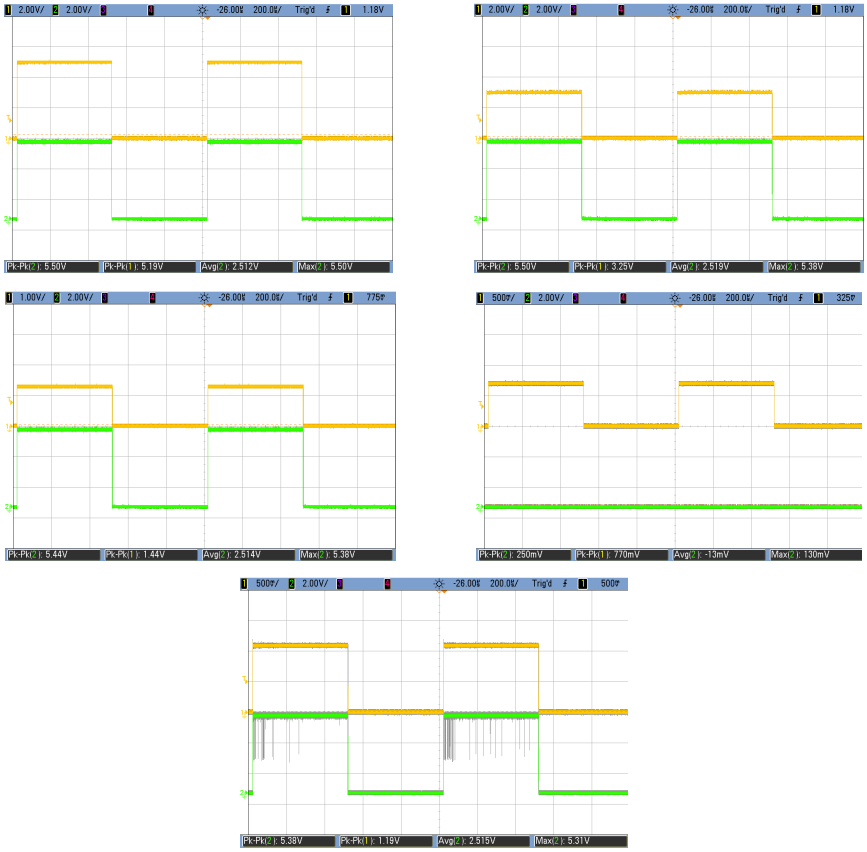

Figure 1.5: 74LS02 load to 74HCT02

Figure 1.6: 74HCT02 load to 74LS02

Analyzing the results in Q it is clear that the irregularities are odd to find, this could be because the manufacturer always leaves a bigger margin to ovoid conflicts within each unique component. Moreover as mention in the theoretical table when the input voltage isn't a logical input, in other words the supply voltage is in the prohibited zone because the circuit cannot decide if the the value of the voltage is low or high, the output value q could mean something in the second component leading to misunderstandings or errors in the logical function. In the other hand, we can notice that using the HCT with the LS integrated circuits, their irregularity is lower in amplitude and not so define as HC with LS, cause their input noise margin are similar.