1 Implementation of Flip-Flop D and SR Latch with discrete logic gates

Using the schematic on Figure 1 the logic gates were implemented on a PCB.

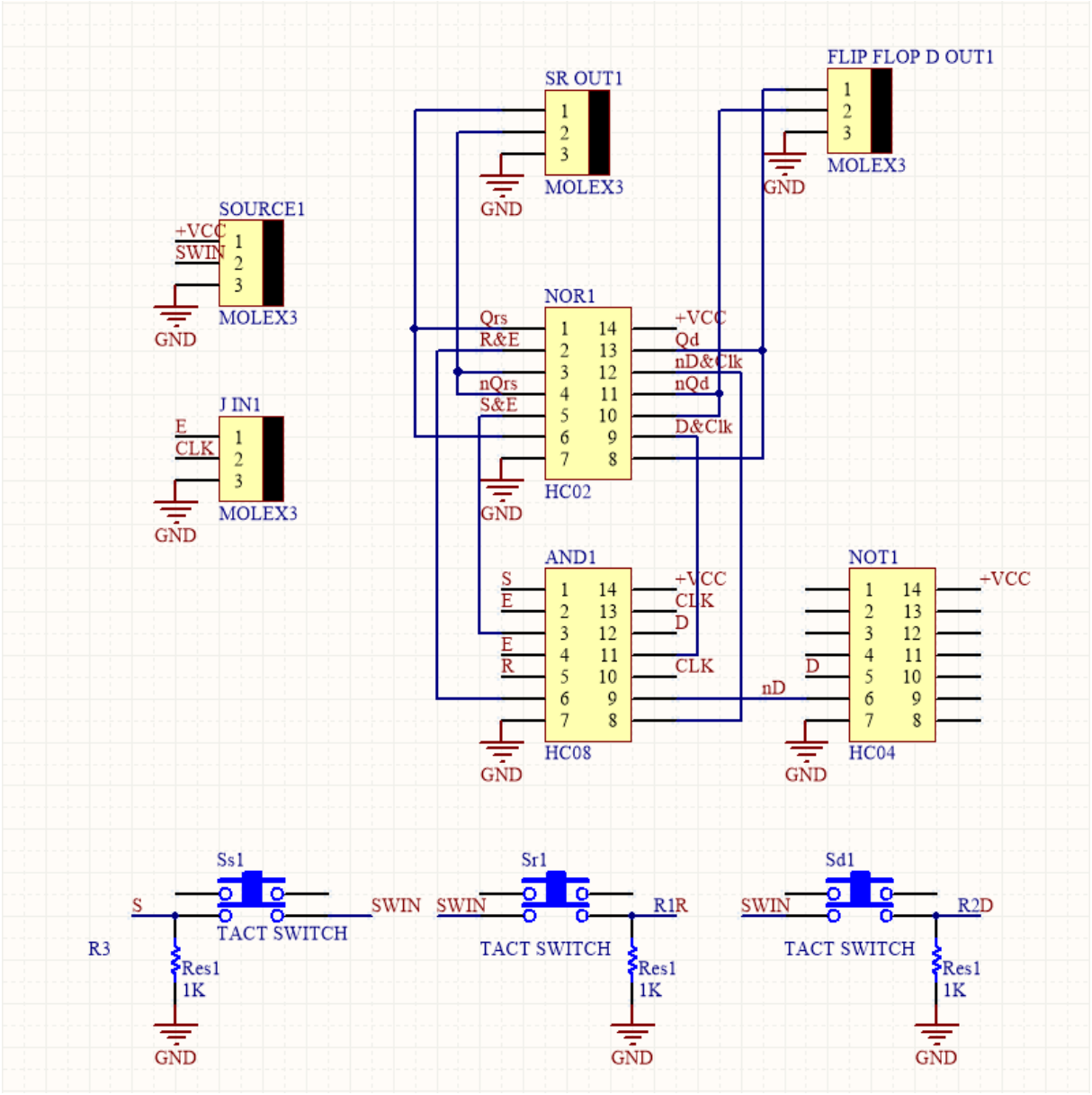

Figure 1: Schematic of the SR Latch (on the left) and Flip-Flop D (on the right)

The resulting circuits were tested and compared to their resulting counterparts as shown in Tables 1, 1, 1 and 1.

Symbol	Parameter	74HC74			Experimental			Unit
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	2	5	6				V
V_{IH}	High-level input voltage	3.15	–	–		–	–	V
V_{IL}	Low-level input voltage	–	–	1.35	–	–		V
V_I	Input voltage	0	–	V_{CC}		–		V
V_O	Output voltage	0	–	V_{CC}		–		V
$\Delta t/\Delta v$	Input rise and fall time	–	–	500	–	–		ns

Table 1: Operating Conditions comparison

Symbol	Parameter	74HC74			Experimental			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	3.84	4.3	–			–	V
V_{OL}	Low-level output voltage	–	0.17	0.4	–			V

Table 2: Electrical Characteristics comparison at V_{CC}=4.5V

Symbol	Parameter		74HC74		Experimental		Unit
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		–	21	–		MHz
t_w	Pulse Duration	$\overline{PRE}$ or $\overline{CLK}$ low	100	–		–	ns
		CLK high or low	100	–		–	
t_{su}	Setup time before CLK ↑	Data	100	–		–	
		$\overline{PRE}$ or $\overline{CLK}$ inactive	100	–		–	

Table 3: Timing Requirements comparison at V_{CC}=4.5V

Symbol	Input	Output	74HC74			Experimental			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			25	50	–			–	V
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	–	20	58	–			ns
	CLK	Q or $\overline{Q}$	–	20	44	–			ns
t_t		Q or $\overline{Q}$	–	8	19	–			ns

Table 4: Switching Characteristics comparison at V_{CC}=4.5V