0.1 Exercise 4: Behaviour Analysis of Circuits Including a 74HC02 Gate

The 74HC02 is an integrated circuit of NOR gates. Firstly, the propagation delays and the transition times are measured for this gate in a no-load output condition. Then these parameters are measured in the case in which the gate is connected in the circuit in Figure. In the following table, the results of the mentioned measures are shown.

Propagation and Transition Times' Measurements

	No-load	Loaded with circuit
t_{pHL}	1,5ns	1,05ns
t_{pLH}	12,5ns	14,4ns
t_f	32ns	30,7ns
t_r	41,4ns	43,2ns

In the previous table it can be seen that the four parameters remain practically the same while being the 74HC02 in the no-load situation and incorporated in the circuit. However, the small differences have opposite behaviours depending on the input signal's edge. In the case of a rising edge in the input signal, the propagation delay t_{pLH} and the transition time t_r are bigger if the 74HC02 forms part of the circuit, than if the 74HC02 is in a no-load situation. But the opposite occurs with the falling edge of the input. This is probably caused by the bigger capacitance in the wires and in the components of the circuit.

Circuit's Response to Frequency Increment

No significable temperature changes were noticed in the integrated circuits nor in any component of the entire circuit. The power discipated by the integrated circuit depends of the input signal's frequency as $P_D = fCV_{DD}^2$, and therefore, a temperature augmentation should be perceived by increasing the frequency from 1Hz to 100kHz. However, no significable temperature changes were noticed in the integrated circuits nor in any component of the entire circuit. Only a small temperature increase was perceived.

Alimentation Voltage of the IC

It is seen in the osciloscope that the alimentation voltage of the circuit in Figure has a ripple when there is an edge of the square input signal. This is due to the big ammount of current that the integrated circuit of NOR gates demands from the voltage source when the input signal rises from 0V to 5V or when it falls from 5V to 0V. In order to reduce this "ripple-shape" response of the circuits to such edges, a capacitor has to be added

between the +Vcc and the GND terminals of the integrated circuit. The goal is to add a capacitor in a way that the less inductance is added to the circuit. This capacitor has to be the nearest possible to such terminals, to avoid adding long wires that add inductance. Moreover, the best capacitors' technology for this case is the multilayer capacitor as it doesn't add as much inductance as other types of capacitors. As it is preffered to use a multilayer capacitor between 10nF and 100nF for this situation, we decided to use a 100nF capacitor and the ripple decreased, as it can be seen in Figure