Task 6

In this section, a D Flip-Flop and a SR Latch are implemented, based on logic gates.

SR Latch

For the SR Latch, it is implemented using NOR gates of 74HC02 integrated circuit. The resulting schematic is shown below.

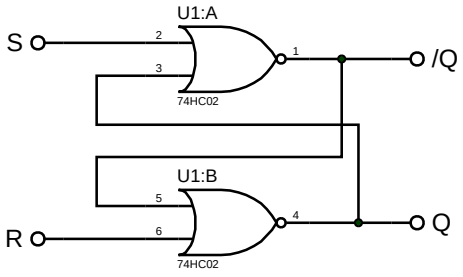

Figure 1: SR Latch circuit - Made in Proteus 7.8

PARAMETROS IMPORTANTES: PROPAGACION DE SET O RESET A LAS SALIDAS. MEDIR. COMPARAR CON UNO COMERCIAL CUALQUIERA

PARAMETER		FROM	TO	VALUE
t_{pd}	Circuit	S	Q	
	74HC279	S	Q	30ns o 26ns
t_{pd}	Circuit	R	Q	
	74HC279	R	Q	31ns o 36ns

Table 1: Measured values

D Flip-Flop

For the D flip-flop, it is implemented using the SR Latch designed before, adding the remaining parts as shown below.

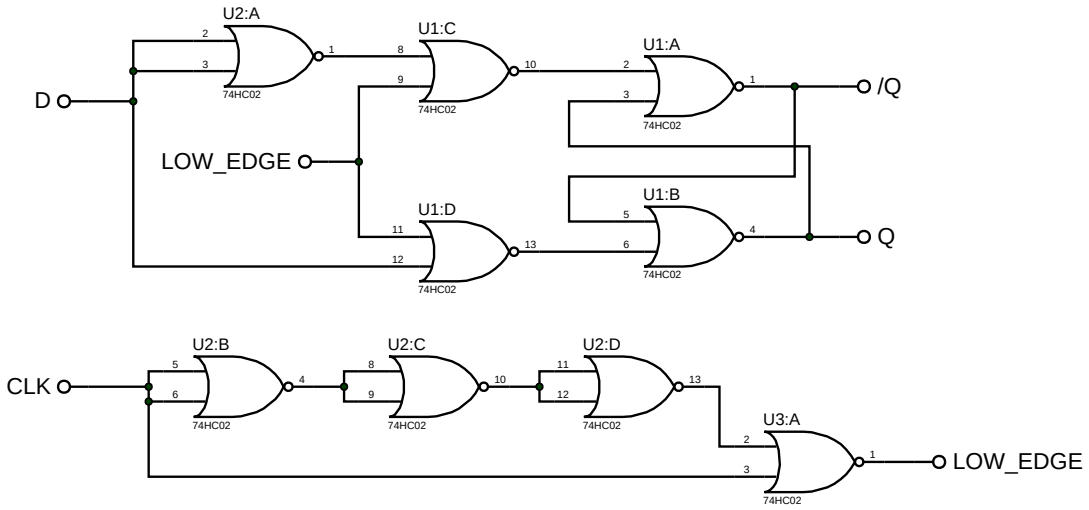

Figure 2: D Flip-Flop circuit - Made in Proteus 7.8

PARAMETROS IMPORTANTES: PROPAGACION DEL D A LA SALIDA LUEGO DEL CLK, TANTO PARA 0 COMO PARA 1. MEDIR. COMPARAR CON UNO COMERCIAL CUALQUIERA. The designed circuit will be compared with the 74HC74 D Flip-Flop, using the datasheet of Texas Instruments.

PARAMETER		FROM	TO	VALUE
t_{pd}	Circuit	CLK	Q or /Q	
	74HC74	CLK	Q or /Q	44ns o 37ns
t_t	Circuit		Q or /Q	
	74HC74		Q or /Q	19ns o 16ns

Table 2: Measured values