Task 4

In this section, there are measured the propagation delay, rise time and fall time of a 74HC02 logic gate (CMOS tecnology) in several configurations: without load, and with a circuit load as shown below.

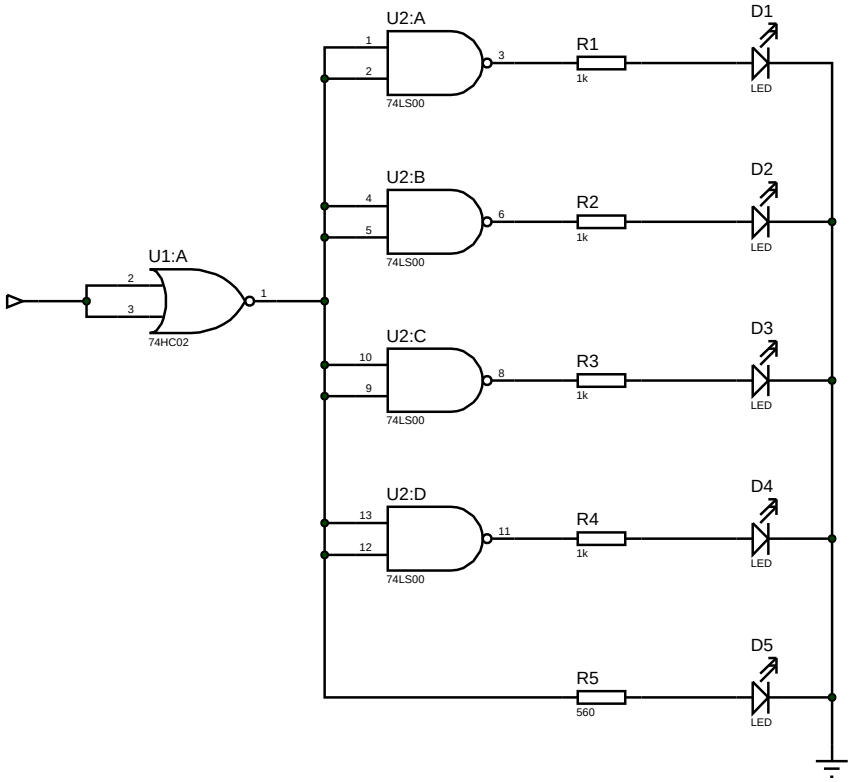

Figure 1: Circuit load schematic - Made in Proteus 7.8

In the following table are the measured times for the diferent configurations.

CASE	tpd_{L-H}	tpd_{H-L}	t_r	t_f
Without LOAD				
Circuit LOAD				
Circuit LOAD (100KHz)				
Circuit LOAD (100KHz with Capacitors)				

Table 1: Measured times

CONCLUSIONES DE TEMPERATURA, TIEMPOS Y EL PORQUE DE USAR 100nF.