

Task 6

In this section, a D Flip-Flop and a SR Latch are implemented, based on logic gates.

SR Latch

For the SR Latch, it is implemented using NOR gates of 74HC02 integrated circuit. The resulting schematic is shown below.

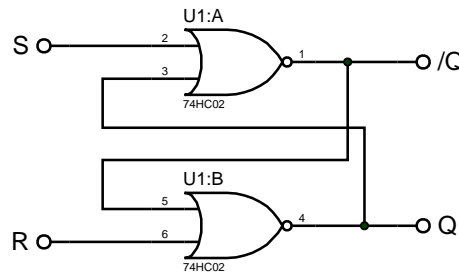


Figure 1: SR Latch circuit - Made in Proteus 7.8

PARAMETROS IMPORTANTES: PROPAGACION DE SET O RESET A LAS SALIDAS. MEDIR. COMPARAR CON UNO COMERCIAL CUALQUIERA

D Flip-Flop

For the D flip-flop, it is implemented using the SR Latch designed before, adding the remaining parts as shown below.

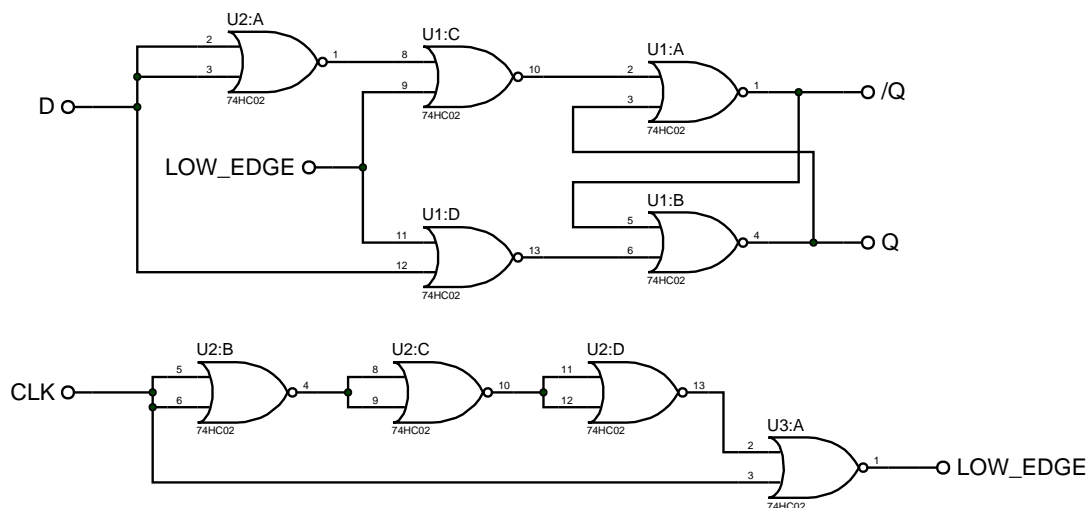


Figure 2: D Flip-Flop circuit - Made in Proteus 7.8

PARAMETROS IMPORTANTES: PROPAGACION DEL D A LA SALIDA LUEGO DEL CLK, TANTO PARA 0 COMO PARA 1. MEDIR. COMPARAR CON UNO COMERCIAL CUALQUIERA.