

Task 3: Issues at minimal cost implementation

Given a truth table, it was requested to see what happens when we implement it with the smallest number of logic gates. To perform this task, ICs that either have NOR or NAND logic gates will be used.

Low cost approach

		ab			
		00	01	11	10
c	0	0	1	0	0
	1	1	1	0	1

Figure 1: Karnaugh Map of the given truth table

We can get the minimal cost output expressed either in groups of max-terms (orange and red groups) or minterms (blue and green groups). Let Z be the output label, its maxterms expression is:

$$Z = (\bar{A}.B) + (C.\bar{B}) \quad (1)$$

Also, its minterms expression is:

$$Z = (\bar{A} + \bar{B}).(C + B) \quad (2)$$

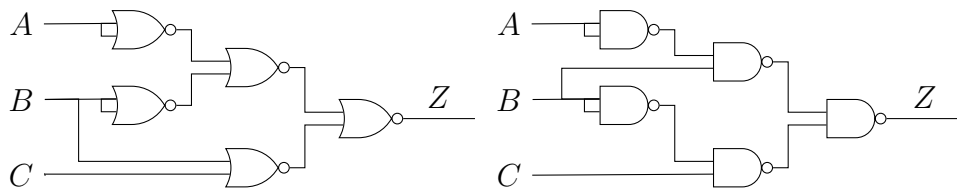


Figure 2: Implementation with NOR gates and NAND gates respectively

1 Introduction

Here is the text out your introduction.

$$\alpha = \sqrt{\beta} \tag{3}$$

1.1 Subsection Heading Here

Write your subsection text here.

2 Conclusion

Write your conclusion here.