Instituto Tecnológico de Buenos Aires

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Trabajo de Laboratorio N° 2

Electrónica III

Grupo 7

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Task 1

In this section are implemented NOT gates with BJT transistors (NPN), in two different configurations, as shown below.

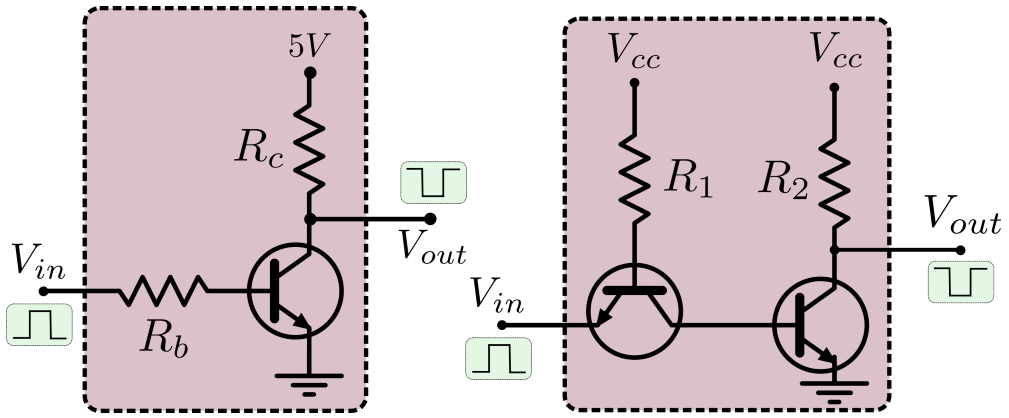

Figure 1: RTL and TTL respectively

Measures

Figure 2:

Where V_{IH}: minimum HIGH input voltage, V_{IL}: maximum LOW input voltage, V_{OH}: minimum HIGH output voltage, V_{OL}: maximum LOW output voltage.

To measure these values we use the ramp waveform and the oscilloscope in xy mode so we can see something like this:

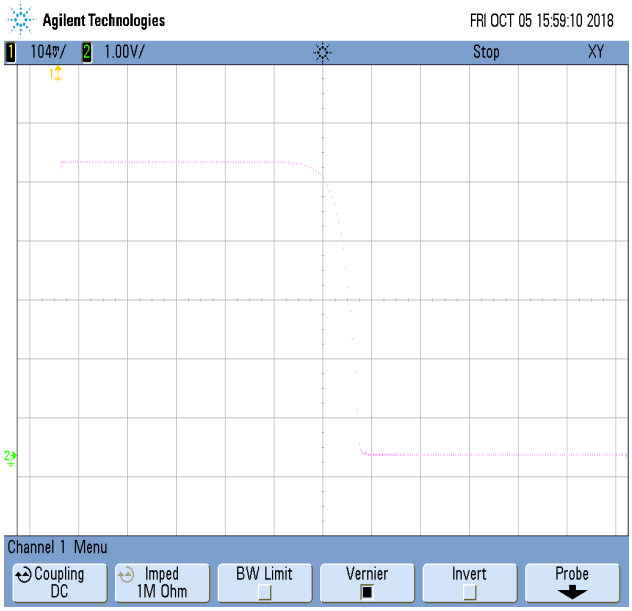

Figure 3:

Where the values we are looking for are found when the derivative is -1.

Noise margin: It allows one to estimate the allowable noise voltage on the input of a gate so that the output will not be affected. Noise margin is specified in terms of two parameters: the low noise margin N_L, and the high noise margin N_H. N_L is defined as the difference in magnitude between the maximum LOW input voltage and the maximum LOW output voltage of the gate. That is, $N_L = |V_{IL} - V_{OL}|$. Similarly, the value of N_H is the difference in magnitude between the minimum HIGH output voltage of and the minimum HIGH input voltage recognizable by the gate. That is, $N_H = |V_{OH} - V_{IH}|$.

Propagation delay: is the difference in time (calculated at 50 % of input-output transition), when output switches, after application of input. It is different if the transition is from HIGH to LOW or form LOW to HIGH.

Rise time is the time, during transition, when output switches from 10% to 90% of the maximum value. *Fall time* is the time when output switches from 90% to 10% of the maximum value.

In order to get the maximum output current, knowing that the load is a 1nF capacitor, with the oscilloscope we find out the derivative of the output voltage:

$$i_c = C\frac{dV_{OUT}}{dt} \tag{1}$$

The maximum current is when the derivative is maximum.

Case A1: RTL without load

V_{OL}=244mV ; V_{OH}=4,85V ; V_{IL}=547mV ; V_{IH}=1,83V
Rise time = 1,26 us

Fall time = 410 ns
Propagation time (HIGH to LOW) = 2,86 us
Propagation time (LOW to HIGH) = 520 ns.
There is not a maximum output current because there is no load.

Case A2: RTL with capacitors load

V_{OL}=384mV ; V_{OH}=4,75V ; V_{IL}=584mV ; V_{IH}=1,76V
Rise time = 1,76 us
Fall time = 480 ns
Propagation time (HIGH to LOW) = 3,12 us
Propagation time (LOW to HIGH) = 656 ns
Max current when input goes from LOW to HIGH: -9,38 mA
Max current when input goes from HIGH to LOW: 2,66 mA

Case B1: TTL without load

V_{OL}=100mV ; V_{OH}=4,69V ; V_{IL}=570mV ; V_{IH}=680mV
Rise time = 156 ns
Fall time = 27 ns
Propagation time (HIGH to LOW) = 299 ns
Propagation time (LOW to HIGH) < 13ns
It was not possible to determine because of the signal generator limitations (the square wave rise/fall time is <13ns) there is not a maximum output current because there is no load.

Case B2: TTL with capacitors load

V_{OL}= 70mV ; V_{OH}= 4,68V ; V_{IL}= 550mV ; V_{IH}= 700mV
Rise time = 960 ns
Fall time = 28 ns
Propagation time (HIGH to LOW) = 1,11 us
Propagation time (LOW to HIGH) < 13 ns
Max current when input goes from LOW to HIGH: -128 mA
Max current when input goes from HIGH to LOW: 8,75 mA
There are 2 different currents because when the transistor is in saturation mode, the capacitor discharges on the NPN transistor that has no resistance. And in cut off mode the capacitor charges with the resistance.

Task 2

In this task we have three different types of nor gates:

LS family: gates made with TTL technology with Schottky transistors. HC family: made with CMOS technology, incompatible with TTL circuits. HCT family: similar to HC but they are compatible with TTL.

Searching for the logic levels of each gate we found that:

dibujo

We can notice that a TTL gate can be connected to the output of a HC gate, but not otherwise because the minimum output voltage level of the TTL (VOH min) is below the minimum input voltage level CMOS (VIH min) . In the case of the HCT, as we said before, the logic levels are compatible with TTL gate.

Fan out

Another fundamental aspect that must be taken into account is the maximum current that provides or absorbs a logic gate. These characteristics are especially important when the technology of the components is TTL, since bipolar transistors are used and it is necessary to ensure the saturation or cutting state of the them. Depending on the relationship between maximum output current and input current, we can connect more or less circuits to a certain logic gate. This maximum number of circuits that I can connect in parallel to the output of a gate is called Fan-Out. Here the CMOS families present a great advantage thanks to the little input current (1 uA), which causes the fan-out to be very high. On the other hand, if we want to connect TTL gates the output capacity will be lower due to the fact that the input current is much higher (1mA).

Results

LS to HC: from 0,75V to 0,8V there was an invalid output
HC to LS: from 2,05V to 2,17V there was an invalid output
LS to HCT: from 0,8V to 0,9V there was an invalid output
HCT to LS: form 0,85V to 0,91V there was an invalid output

Case a:
The input range where the output was invalid is inside the range of voltages allowed for the logic 0 of the LS gate, so the output should be a 0. Here we can see the incompatibility between the gates. Case b, c, d: all the input ranges where the output was invalid belong to the invalid input voltages of the gate that is connected first.

Task 3

Given a truth table, it was requested to see what happens when the truth table is implemented with the smallest quantity of logic gates. To perform this task, ICs that have NAND logic gates only will be used. This is because in most of ICs there are many logic gates so it's a waste of logic gates if we use for example just one of them. Note that this can also be implemented with NOR only ICs.

Low cost approach

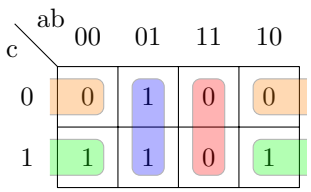

Figure 4: Karnaugh Map of the given truth table

Let Z be the output label, its reduced minterms expression is:

$$Z = (\bar{A}.B) + (C.\bar{B}) \tag{2}$$

Also, its reduced maxterms expression is:

$$Z = (\bar{A} + \bar{B}).(C + B) \tag{3}$$

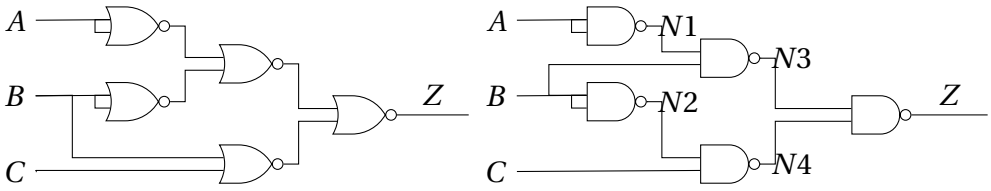

Figure 5: Implementation with NOR gates and NAND gates respectively

Note that the quantity of logic gates in both cases are the same.

Hazards

Sometimes propagation delays cause unexpected and unwanted transitions in the ouput. Depending on what we see in the output is how this issue is called. If there is a transition from 1 to

0 and the output was supposed to stay at 1 it is said that the circuit has a static 1-hazard. If the output must go from 0 to 1(or 1 to 0) and before establishing at 1 (or 0), it changes its value it is said that the circuit has a dynamic hazard.

Hazards can always be found at the Karnaugh map. An input that follows multiple paths to an output can create a glitch (due to the hazards in the circuit) if, for example, one path has an inverter (in this case implemented with a NAND logic gate) and one does not. This issue is called "asymmetric path delay" and it can be seen in Figure 4 with the input B.

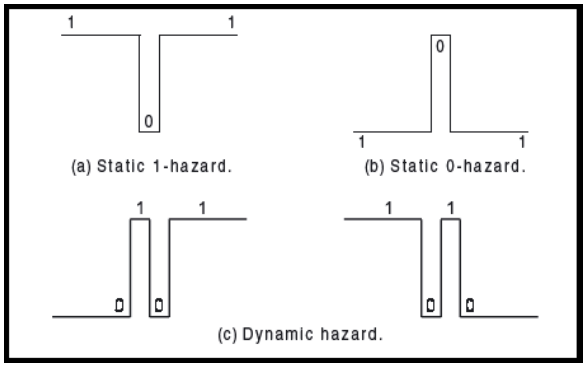

Figure 6: Different types of hazards

Static 1-Hazard example

Take the NAND implementation into account, assume all the propagation times equal and then observe transition of the states A,B,C from 011 to 001 respectively.

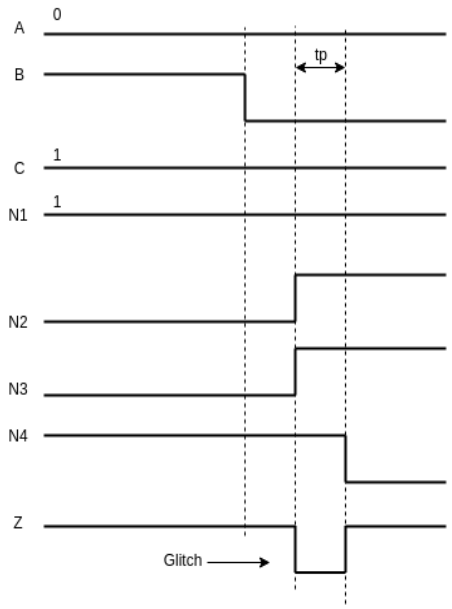

Figure 7: Propagation time analysis

Note that tp in Figure 7 denotes the propagation time.

It can be seen that there should be a glitch at the output.The different combination of delays that produce a glitch may or may not be likely to occur in the implementation of the circuit. In some instances it is very unlikely that such delays would occur.

Measures obtained from NAND implementation

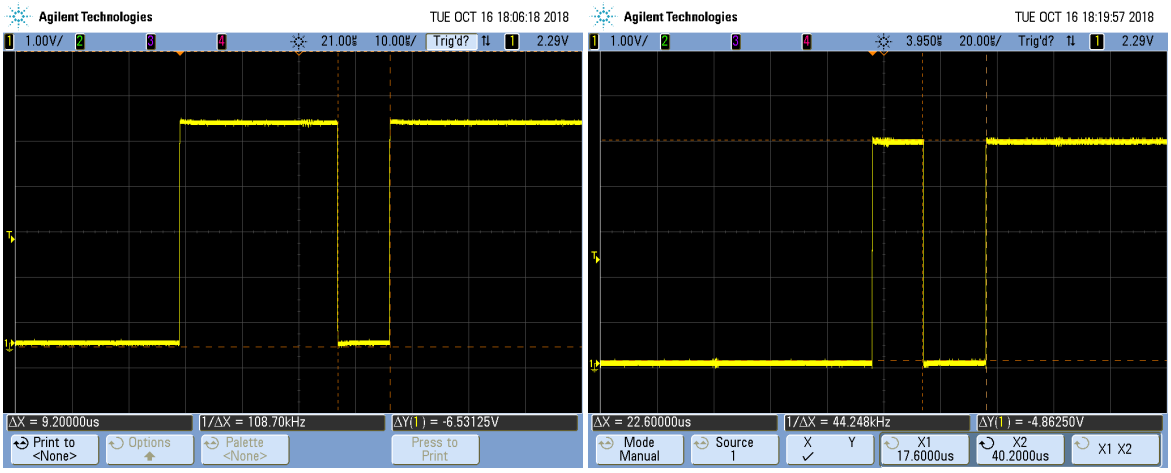

Figure 8: Dynamic hazards

In order to get the measures it was required to trigger many times until one of these glitches appear. It can be seen in Figure 8 that glitches caused by dynamic hazards doesn't share the same time interval in spite of being the same transition (from 000 to 001), this gives us some idea of delay propagation.

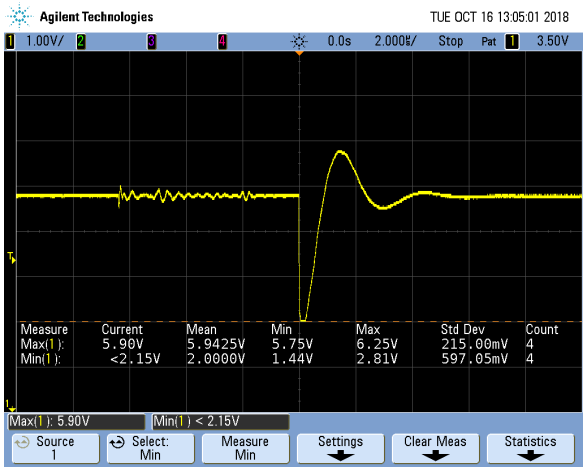

Figure 9: Static 1-hazard

The measure in Figure 9 was made with the transition 001 to 011 and the trigger configured to get the negative-edge so these glitches can be found.

Conclusion

In order to remove glitches it is needed to add redundant groups in the Karnaugh Map so that disjoint groups overlap.

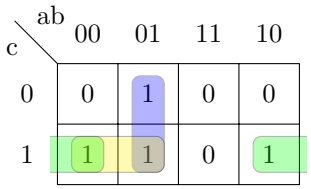

Figure 10: Karnaugh with redundant logic

In this case the output is given by:

$$Z = (\bar{A} + \bar{B}).(C + B) + (\bar{A}.C)$$

Note that the new term term of the expression is not dependent of B so regardless of the variation of B there won't be glitches in the output.

Task 4

In this section, there are measured the propagation delay, rise time and fall time of a 74HC02 logic gate (CMOS tecnology) in several configurations: without load, and with a circuit load as shown below.

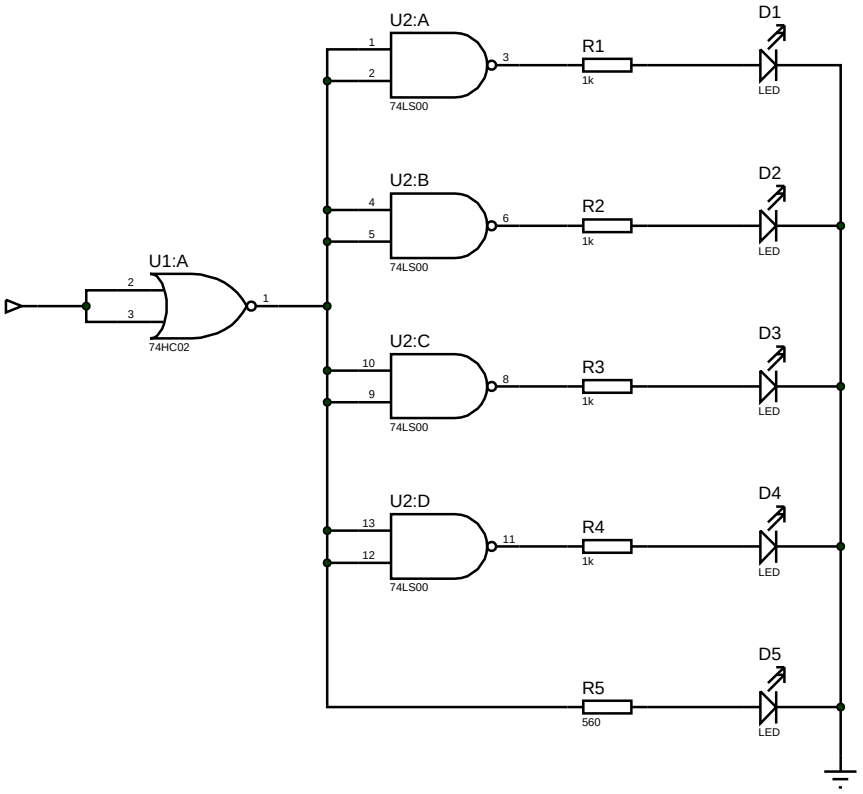

Figure 11: Circuit load schematic - Made in Proteus 7.8

In the following table are the measured times for the diferent configurations.

CASE	tpd_{L-H}	tpd_{H-L}	t_r	t_f
Without LOAD	15ns	5ns	42ns	45ns
Circuit LOAD	17ns	5ns	46ns	45ns
Circuit LOAD (100KHz)	18ns	4ns	45ns	52ns
Circuit LOAD (100KHz with Capacitors)	9ns	4ns	50ns	52ns

Table 1: Measured times

In the first two cases, it was observed that the measured times had no appreciable diferences when the gate is charged with the external circuit. In the case with the circuit, the IC raises its temperature a little. This is mainly due to the direct charge of the R5 and L5 componentes, requesting the IC a current that is near to the maximum value of $4mA$ per output.

Also the output voltage level decreases in the case with the circuit charge, compared to the case without load, as shown in the next figures.

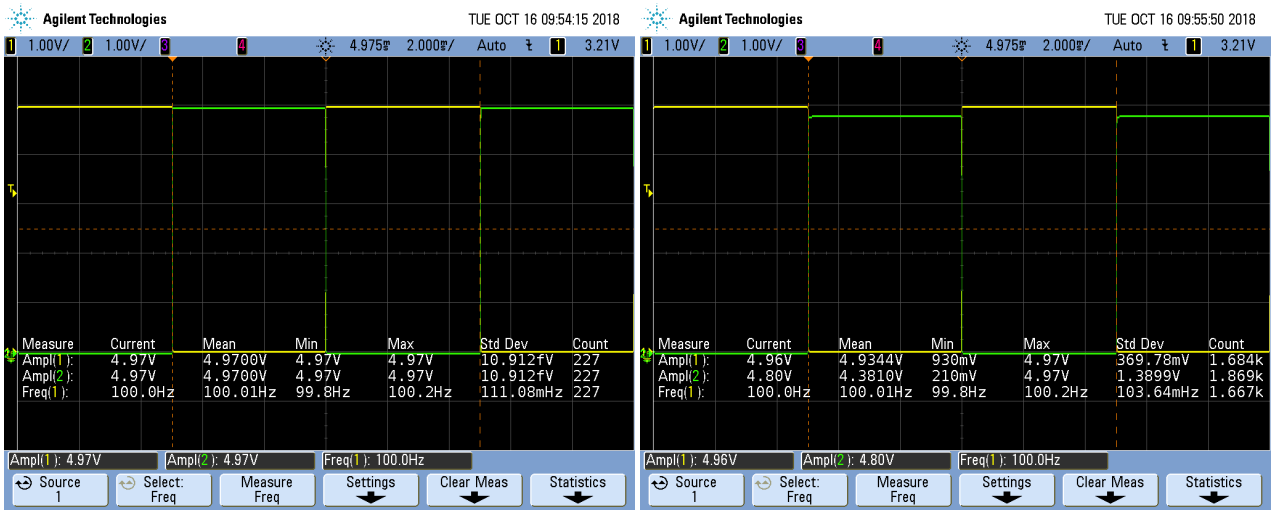

Figure 12: Voltage levels: CH1 - Gate input, CH2 - Gate output. On the left without load, and on the right with the circuit load.

In the same circuit, increasing the frecuency up to $100KHz$, a decrease was also observed in the output voltage level, with a little oscilation in the transition from low to high. This is because the external ciruit requires more current for turning the LED on, wich causes a voltage overshoot for a short period of time, until the circuit becomes stable. To absorve this overshoot, a decoupling capacitor is placed near the supply pins of the IC, with a value of $100nF$. This value is suggested by the datasheet of Texas Instruments. Below is shown the output change from low to high with the circuit at $100KHz$, without and with the capacitor.

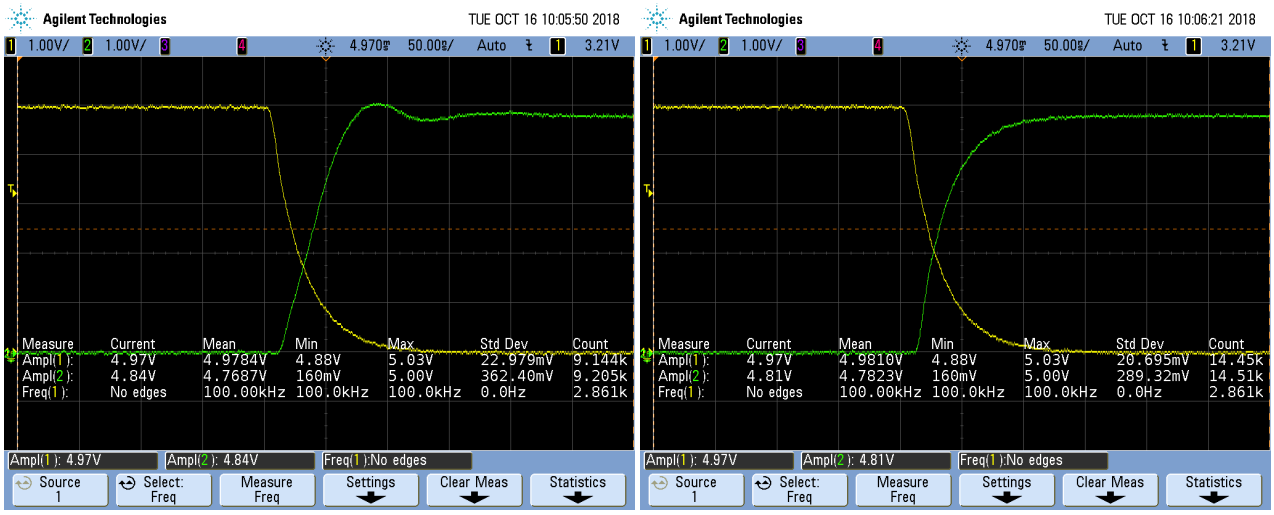

Figure 13: Transition L-H CH1 - Gate input, CH2 - Gate output. On the left without capacitor, and on the right with it.

Another fact observed is the high noise level (about 1V) at the supply voltage. This was also fixed with the decoupling capacitors, as shown below.

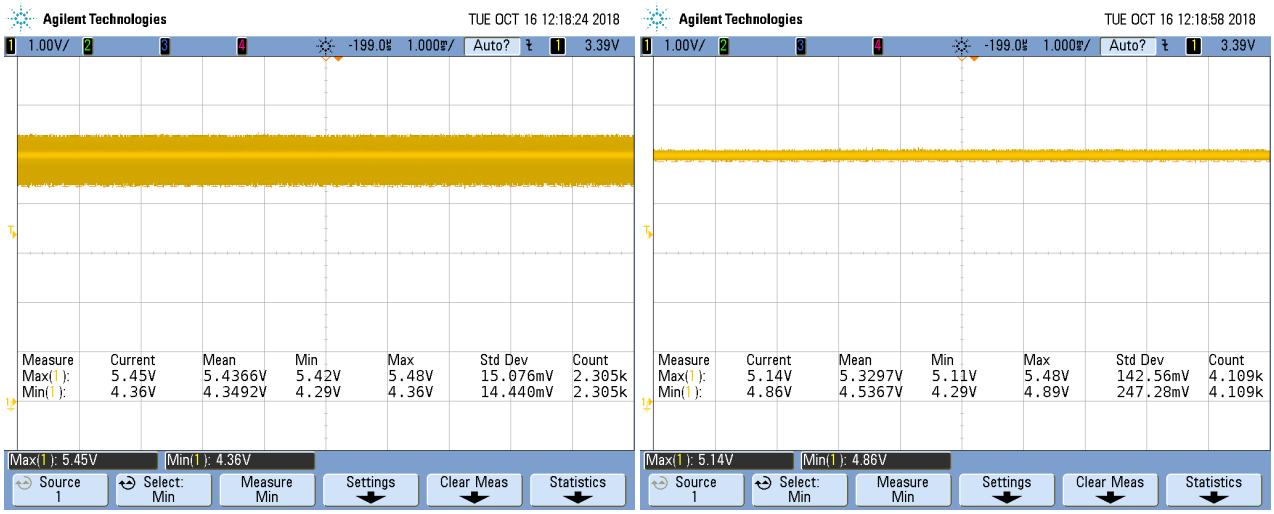

Figure 14: Supply voltage: CH1 - VCC. On the left without capacitor, and on the right with it.

Task 5

In this section it will be anayzed two particular cases of the TTL AND gate and the CMOS OR gate. The configurations to analyze are shown below.

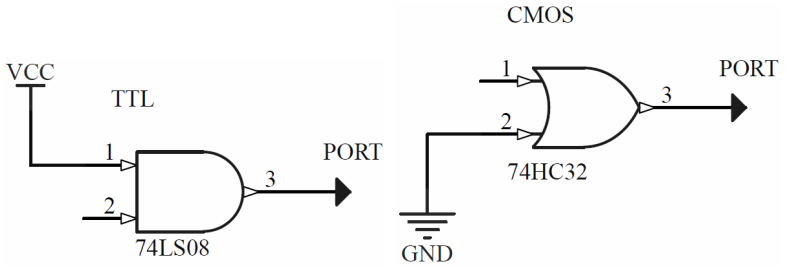

Figure 15: TTL AND gate and CMOS OR gate test circuits

In the case of the TTL AND gate, with one of the inputs not connected and the other to +VCC, the output results on HIGH level. That is because the emmiter terminal of the transistor for that input pin is floating without setting the potencial to a reference, so the transistor is in cut-off mode, causing that the output transistor to be in cut-off mode to, resulting a HIGH level voltage from its colector terminal.

In the case of the CMOS gate, with one of the inputs floating and the other to GND, the output results on HIGH level. That is because the gate terminal of the MOS transistor results floating, without setting the potencial to a reference, so its not fixed in saturation mode, similar to what happened in the previous case.

Then, both technologies are connected as follows.

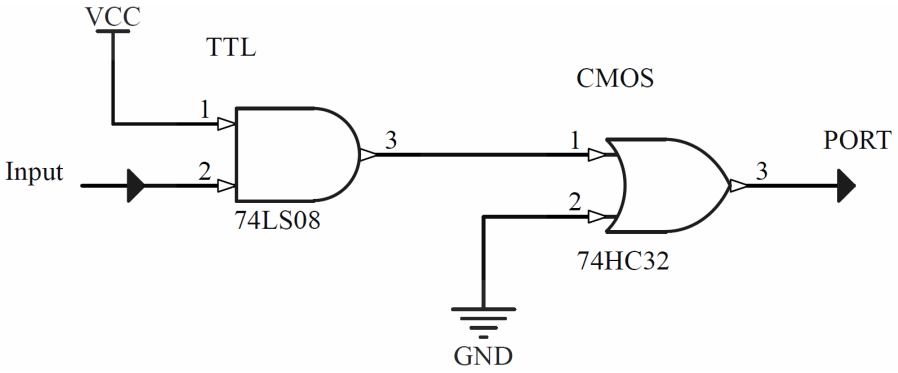

Figure 16: TTL AND gate and CMOS OR gate connected

The problem observed is the same as before: with the input pin floating, the output results on HIGH level voltage. But this connection has a problem regarding the voltage levels. From the examples used, according to Texas Instruments datasheets, in 74LS08 for the AND gate the $VOH_{MIN} = 2V$ in the worst case and for the 74HC32 (OR gate) the $VIH_{MIN} = 3.15V$. In the worst case, that can cause that although both inputs are in HIGH level, if the AND output is $2V$, it will be considered as a OV in the OR gate, showing $0V$ at the final output.

The simplest solution may be use both gates from the same technology, but it can be fixed with a level shifter circuit, implemented with a PNP transistor as shown below.

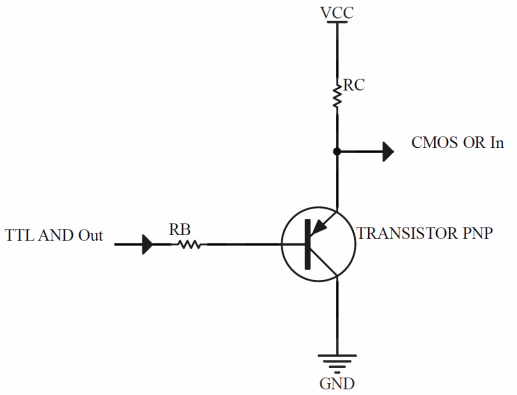

Figure 17: Level shifter with an PNP transistor

Task 6

In this section, a D Flip-Flop and a SR Latch are implemented, based on logic gates.

SR Latch

For the SR Latch, it is implemented using NOR gates of 74HC02 integrated circuit. The resulting schematic is shown below.

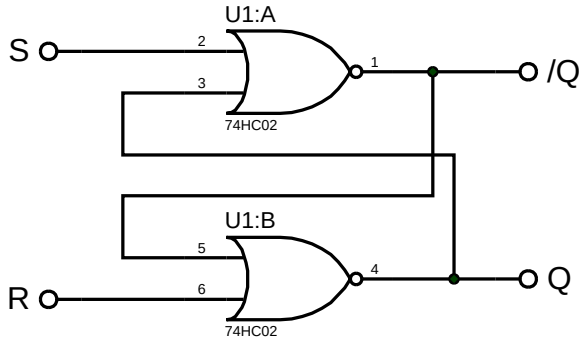

Figure 18: SR Latch circuit - Made in Proteus 7.8

The measured parameters are the same indicated by the reference IC 74HC279[1] (Quad-SR-Latch): time propagation delays (t_{pd}) from S to Q, and from R to Q, for comparative purposes.

PARAMETER		FROM	TO	VALUE
t_{pd}	Circuit	S	Q	13.2ns
	74HC279	S	Q	9ns
t_{pd}	Circuit	R	Q	18ns
	74HC279	R	Q	11ns

Table 2: Measured values

As shown, the IC times are faster than the discrete latch builded. This diferences are related to the fact that the logic gates are not identical to each other, son they may have diferent propagation delay times.
On the other side, with the Quad-NOT gate IC 74HC02 only two latches can be built, in comparison with the four latches included in the 74HC279 IC.

[1] "TC74HC279AP", Toshiba, 1997-08-07

D Flip-Flop

For the D flip-flop, it is implemented using the SR Latch designed before, adding the remaining parts as shown below.

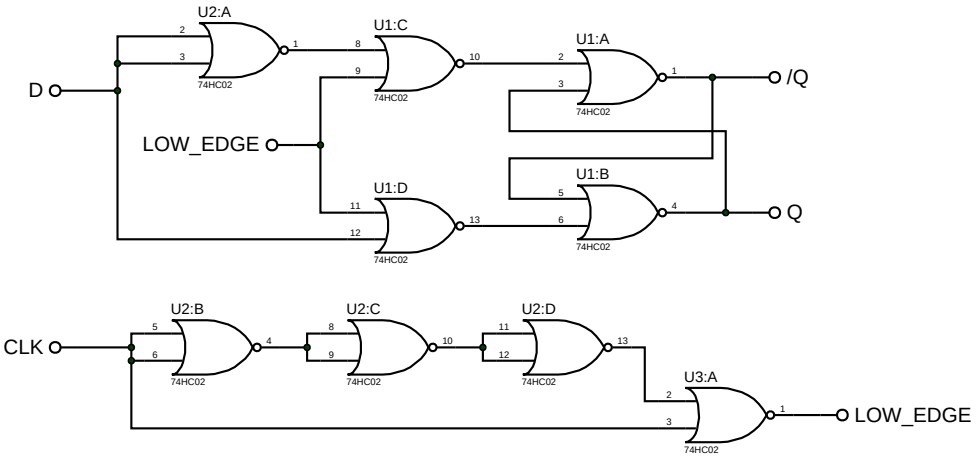

Figure 19: D Flip-Flop circuit - Made in Proteus 7.8

The designed circuit will be compared with the 74HC74[2] D Flip-Flop.

PARAMETER		FROM	TO	VALUE
t_{pd}	Circuit	CLK	Q or /Q	30ns
	74HC74	CLK	Q or /Q	14ns
t_t	Circuit		Q or /Q	18ns
	74HC74		Q or /Q	7ns

Table 3: Measured values

As shown, the measured times from the built circuit are slower than the IC 74HC74 times. Also, it required two NOR-Gates IC (74HC02) to build the flip flop with all discrete logic gates, and each gate has its own time propagation delay that needs to be considerated. On the other hand, the 74HC74 has two flip flops in one IC; to build them with logic gates, 4 IC 74HC02 would be needed.

[2] "74HC74 Dual D-type flip-flop with set and reset; positive edge-trigger", Nexperia, Rev.5 - 3 December 2015

Task 7

In this task we're asked to implement one syncronomous, and one asynchronous 3-bit counter, and contrast them.

Async. counter

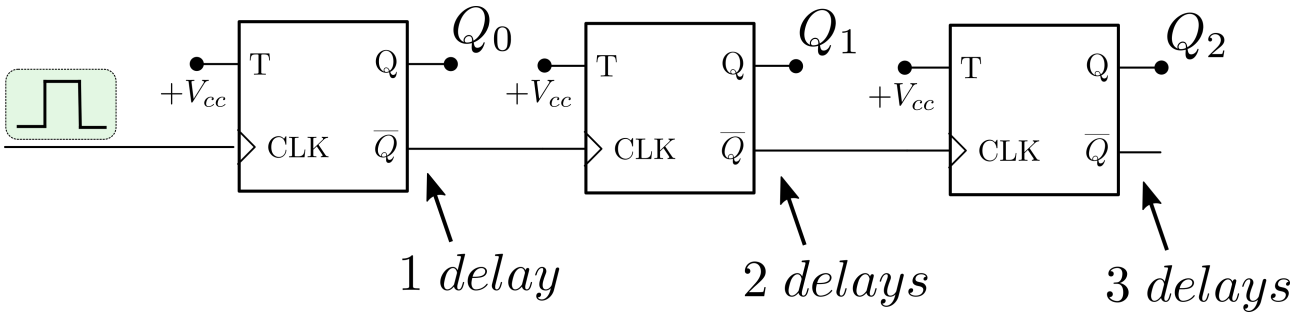

Figure 20: Async. counter - delays

This counter work with a casquade triggering flip flops clocks done by the not Q output.

The idea is that, everytime the left flip flop is clocked two times, not Q goes up one time, thus, right flip flop is clocked one time (the half) Propagating this logic to the general case, n-th flip flop has a period 2^n thus we made a binary counter.

The theorical problem of this system is the delay propagation. As there is a delay between clock rising edge and Q update, the total delay will be multiplied by the number of flip flops.

Sync. counter

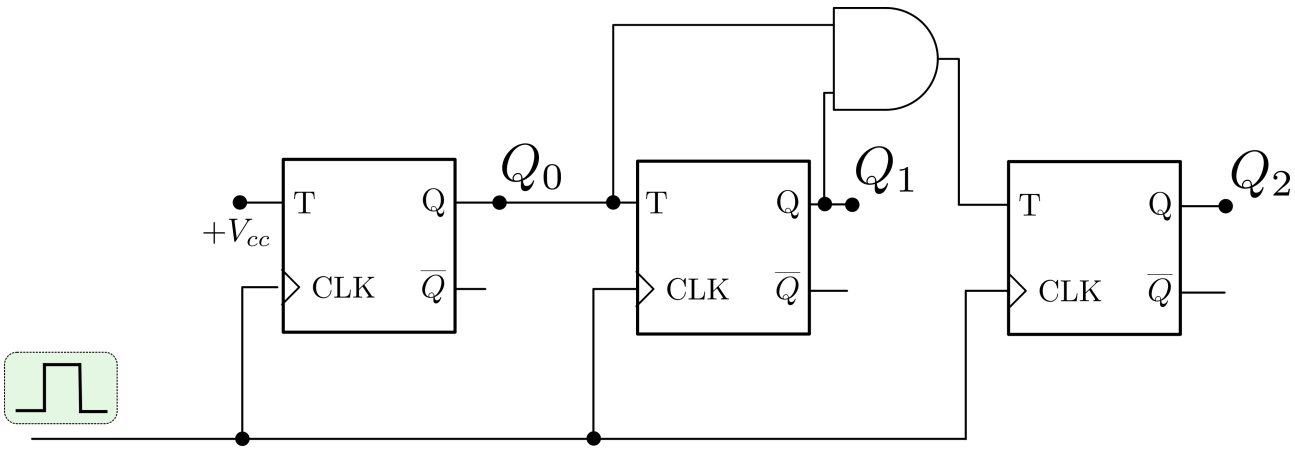

Figure 21: Sync. counter - delays

This counter is made to fix the problem of the previous counter. In this logic, all flip flops clocks are connected to the same trigger, thus, all of them are updated in the same instant, not, one after the other. We control if each flip flop switches by controlling the T input. Flip flop 2 needs flip flop 1 to be in 1 to switch (01->10). Flip flop 3 needs both previous two flip flops in 1 to switch. (011->100)

Measurements

We built the counters for both cases. As expected, in low frequencies diferences weren't noticed. But, when we increased frecuency to 1Mhz at clock input we were able to see a difference

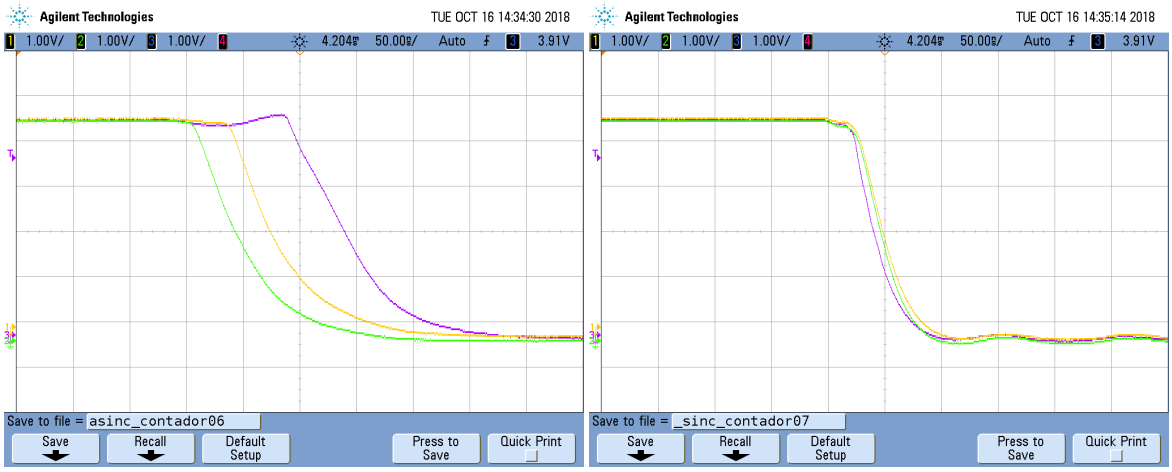

Figure 22: Comparison - 1Mhz clock - Q_0,Q_1,Q_2 signals - async, sync counters, left to right

From figure we can see that in async circuit bits are updated one after the other, while in sync circuit all of them are updated at the same time. Also we should note that updates are not instant, as it was assumed in previous analisis. There is countinous change, that creates an evident limitation to circuit. This limitation made both counters unusable with frecuencies slighty higher than 1Mhz (1Mhz was the higher frecuency with proper functioning found in both cases), cause the flip flops were switched before the output signal reached its corresponding logic level. So, with 3 bits in practice there is no difference between both circuits, as this limitation impacts both circuits in, apparently, the same way.

Task 8

In this section, a distance measurement system is implemented using discrete logic and the ultrasonic sensor HC - SR04. With it, distances between 1.7cm and 4.25m can be measured. The design is shown in the following block diagram.

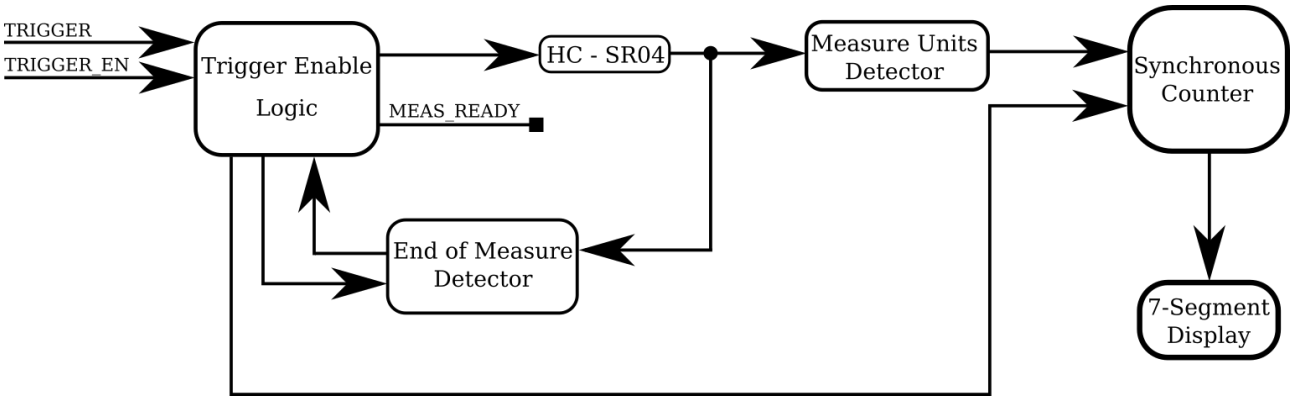

Figure 23: Distance measurement system - Block diagram

Trigger Enable Logic

For this part, a T flip-flop is used to define two states: (1) Measure enabled and (2) Measuring.

In state (1), with TRIGGER_EN on HIGH level, a measure can be made by sending a positive edge to the TRIGGER input, then the flip-flop changes to state (2), preventing a new retrigger while measuring if a new positive edge is detected in TRIGGER input. This two states and the MEASURE_READY bit are referenced from the $\overline{Q}$ output of the flip-flop. When the measure ends, an edge is sended to the CLR pin of the flip-flop, for returning to state (1), allowing to make a new measure. The previus performance is shown in the following time diagram.

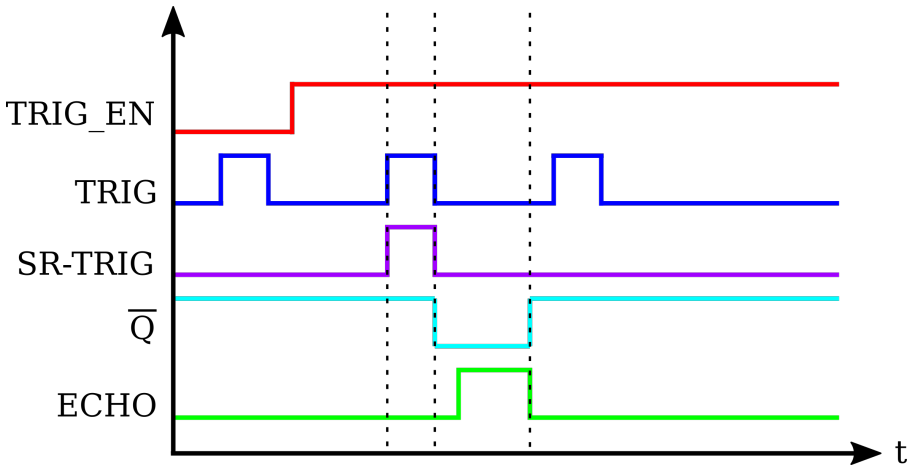

Figure 24: Trigger Enable Logic - Time diagram

The ultrasonic sensor needs a pulse of a period T > 10μSeg, so the edge of TRIGGER input is sended to a monostable circuit (implemented with a LM555 timer) to ensure that the condition is met. The final schematic of this section is shown below.

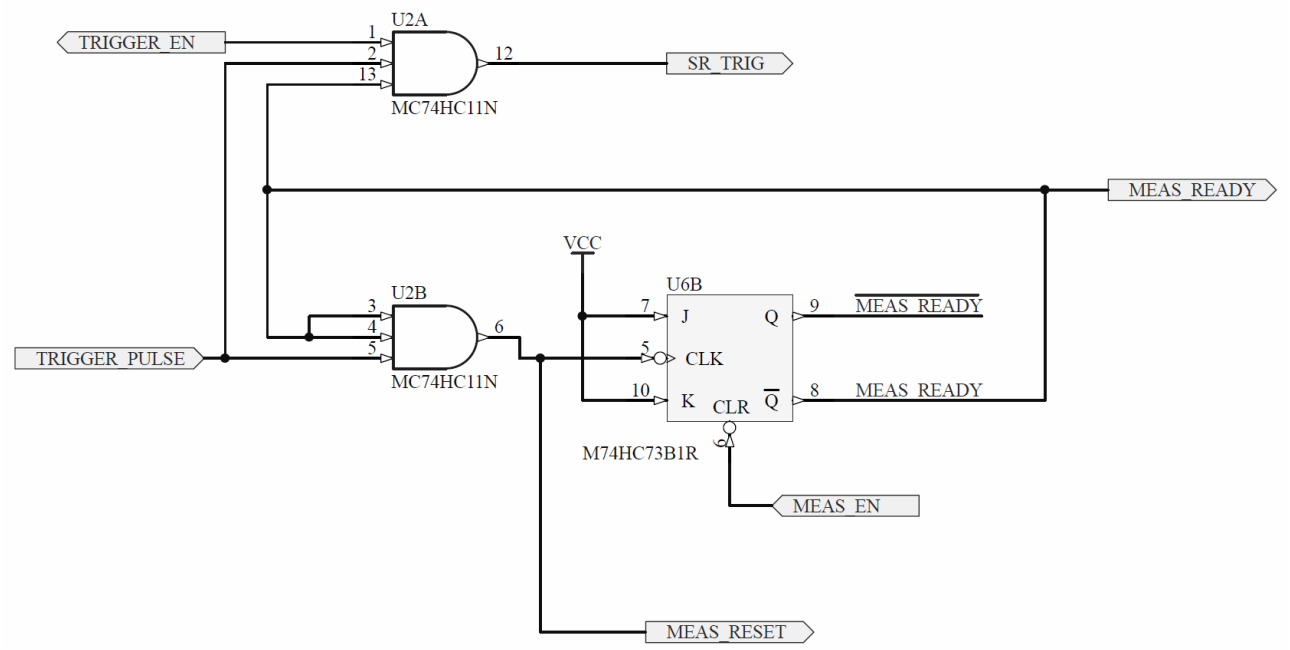

Figure 25: Trigger Enable Logic - Schematic circuit made in Altium 15

HC - SR04 Sensor

To make the measures in the mentioned interval, the HC - SR04 after receiving the TRIG input pulse, it answers at the ECHO out with a pulse of a period T > 100μSeg (1.7cm), up to 25000μSeg (4.25m). It will be fractioned in units of 100μSeg (to be counted).

To know the measure value, the obtained number N is processed in the following calculation:

$$Distance[m] = 170 \cdot 100 \cdot 10^{-6} \cdot N$$

By fractioning the ECHO pulse in discrete units, the resulting resolution is equivalent to 1.7cm, which is the smallest unit that can be counted (100μSeg).

Measure units detector

For fractioning the ECHO response into units of 100μSeg, it is connected to an AND gate with a clock source (CLK) whose period is 100μSeg.
In this way, while the ECHO out stays at HIGH level, the signal at the AND gate output is equal to the clock source. While not measuring, the output stays at LOW level. The previous performance is shown in the time diagram below.

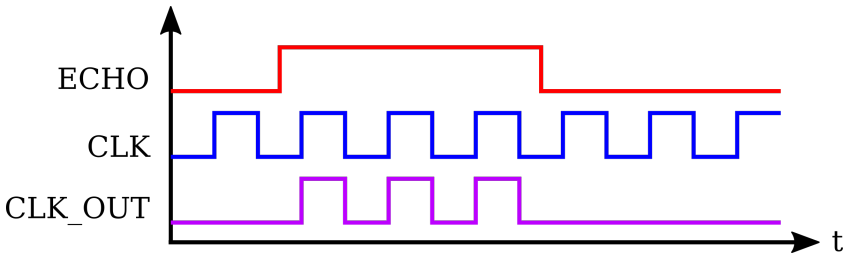

Figure 26: Measure units detector - Time diagram

The CLK signal was implemented with a LM555 timer in astable configuration. The schematic for this section is shown below.

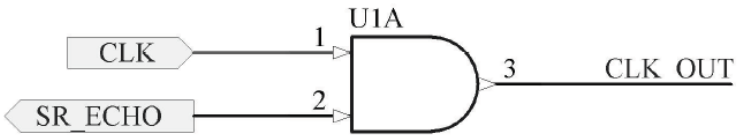

Figure 27: Measure units detector - Schematic circuit made in Altium 15

Synchronous counter

For counting the time units, an integrated synchronous counter is implemented (CD4040), whose CLK input is conected to the out signal of the measure units detector. It detects the positive edges of the CLK signal, in this case having one per 100μSeg. From the 12-bit output, only 8-bit are used, because for measuring the maximum distance, only 250 untis are needed (25000μSeg over 100μSeg results in 250 units), and if the binary out is converted to decimal, the maximun number is $2^8 = 256$ (which covers the 250 maximum).
The integrated circuit implementation is shown below.

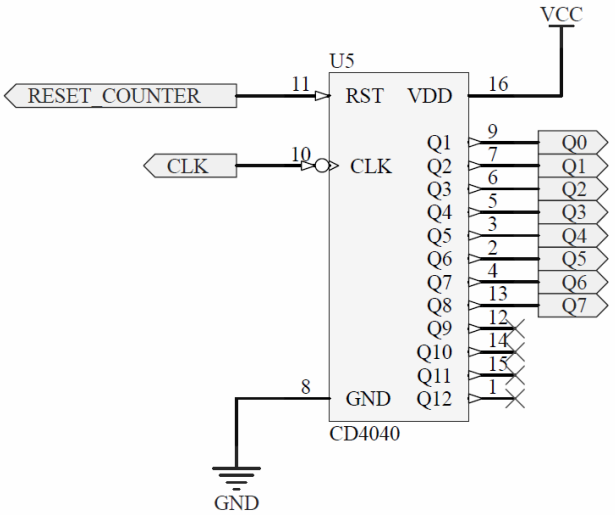

Figure 28: Synchronous counter - Schematic circuit made in Altium 15

End of measure detector

When the measure ends, the negative edge produced by the ECHO is used in a discrete edge detector to reset the flip-flop in the trigger enable logic, so a new measure can be started at any time. The circuit diagram of the implementation is shown below.

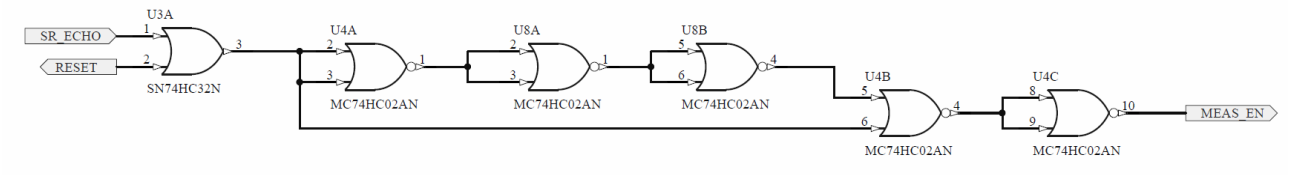

Figure 29: End of measure detector - Schematic circuit made in Altium 15

The binary output resulting from the measure stays on until a new positive edge from the trigger is received. Then, the pulse used to change the flip-flop state in a new measure is also used to reset the previous binary output from the synchronous counter.

Manual reset

If when connecting the power supply to the circuit, the counter is not in cero, or the flip-flop starts switched into the state (2), a manual switch for reset is added with a pull-down resistor, as shown below.

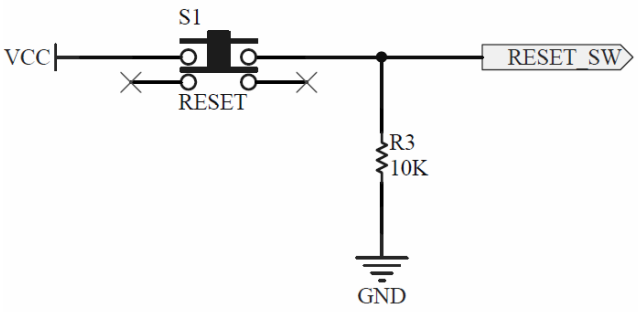

Figure 30: Manual reset with pull-down resistor - Made in Altium 15

Aditional settings

MEASURE_READY indicator

To know if the flip-flop starts in the correct state when connecting the power supply or if the last measure has finished, a bicolor LED was used through two transistors, using the Q and $\overline{Q}$ outputs of the flip-flop. When a measure ends (or when at the power supply connection the flip-flop starts at the correct state), the LED turns green as an OK indication. When measuring, the LED turns red until it ends. If when connecting the power supply (or in any moment) the flip-flop starts in

the wrong state, the LED will remain in red. This can be fixed by pressing the reset switch. The schematic circuit is shown below.

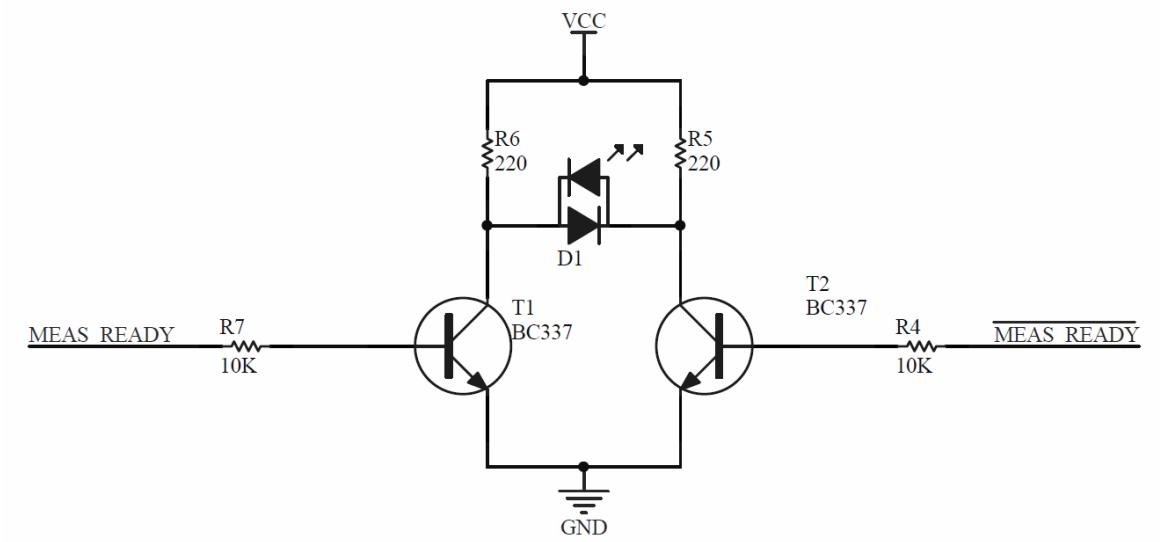

Figure 31: MEASURE_END indicator - Transistor logic made in Altium 15

The calculation of the resistors can be read from the Annex.

Measure counted units indicator

To obtain the amount of time units measured more easily, the CLK out of the measure units detector is used in decade counters implemented with CD4033, because their out pins are decoded for use in 7-segment displays. Since the maximum measure has 3 digits, there are 3 counters and displays implemented (their reset pin is connected to the reset signal of the end of measure detector, and to the reset switch through an OR gate). The implemented circuit schematic is shown below. It has been done in a separete PCB.

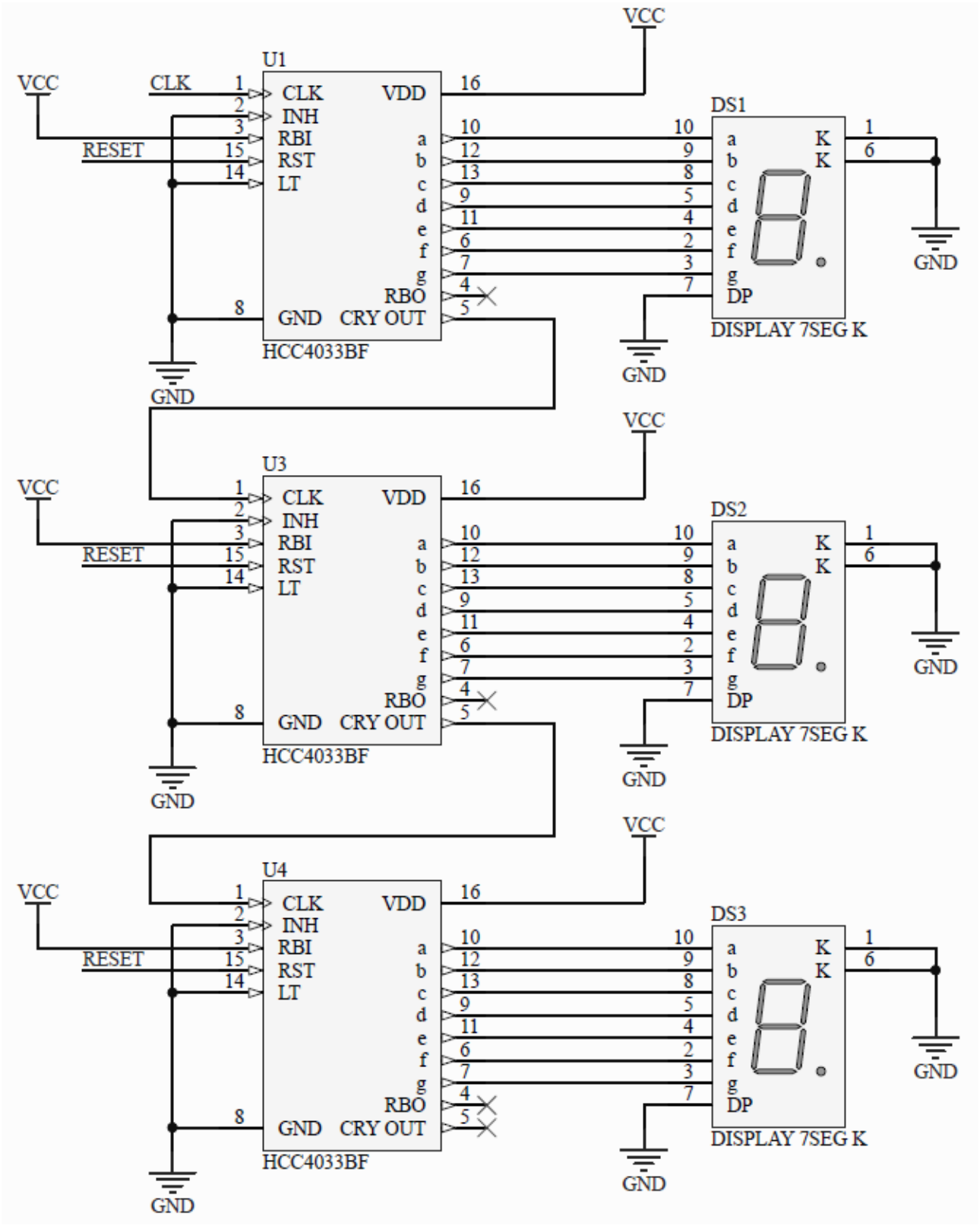

Figure 32: Measure display - Schematic circuit made in Altium 15

Appendix

MEASURE_READY indicator - Resistors calculation

For the circuit design, the transistors are used in saturation-cutt off mode. Considering a $15mA$ current for the LED, it will be the IC_{SAT}. Going through the out loop we have:

$$V_{CC} - IC_{SAT}R_C - V_{LED} - VCE_{SAT} = 0$$

Considering as $VCE_{SAT} = 0.2V$ and a $V_{LED} = 1.8V$, the value of R_C (collector resistor) can be obtained as follows:

$$\frac{V_{CC} - V_{LED} - VCE_{SAT}}{IC_{SAT}} = RC = 200\Omega$$

Normalizing the value, it remains as $R_C = 220\Omega$. Recalculating the new IC_{SAT}:

$$\frac{V_{CC} - V_{LED} - VCE_{SAT}}{R_C} = IC_{SAT} = 13.6mA$$

Using the BC337 transistors, according to ON Semiconductor datasheet, the minimum HFE is 100, which will be used to calculate the minimum IB_{SAT} (because its the worst case, to guarantee the saturation):

$$\frac{IC_{SAT}}{HFE_{MIN}} = IB_{SAT-MIN} = 136\mu A$$

With that value, the base resistors can be calculated, and then normalized down to get an IB_{SAT} over the previous limit. Going through the entry loop:

$$V_{Q-OUT} - VBE_{ON} - IB_{SAT}R_B = 0$$

Considerating that $VBE_{ON} = 0.7V$ and the output voltage of the flip-flop as $5V$ on HIGH level:

$$\frac{V_{Q-OUT} - VBE_{ON}}{IB_{SAT}} = RB_{MAX} = 31.6K\Omega$$

Normalizing the value, it results in $R_B = 10K\Omega$. Checking the resulting IB_{SAT}:

$$\frac{V_{Q-OUT} - VBE_{ON}}{R_B} = IB_{SAT} = 436\mu A$$

According to maximun ratings of Texas Instruments datasheet, the Q and $\overline{Q}$ outs can manage a current up to $25mA$, so the resulting IB_{SAT} is in range.