

1 EXERCISE 1:

1.1 MEALY STATE MACHINE

In the Mealy state machine, the output value not only depends on the state we are but also depends on the input values. This is to say the output could be represented as a function like $Z = f(X_1, \dots, X_n, Q_1, \dots, Q_n)$ where Z: output, Q: State and X: Input event as could be visualize:

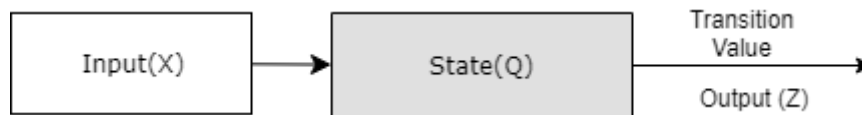


Figure 1.1: Mealy state machine simple representation

In this exercise, two sensors I and S function as input event to the state machine. Analyzing the possible states and event we obtain the following Mealy machine diagram:

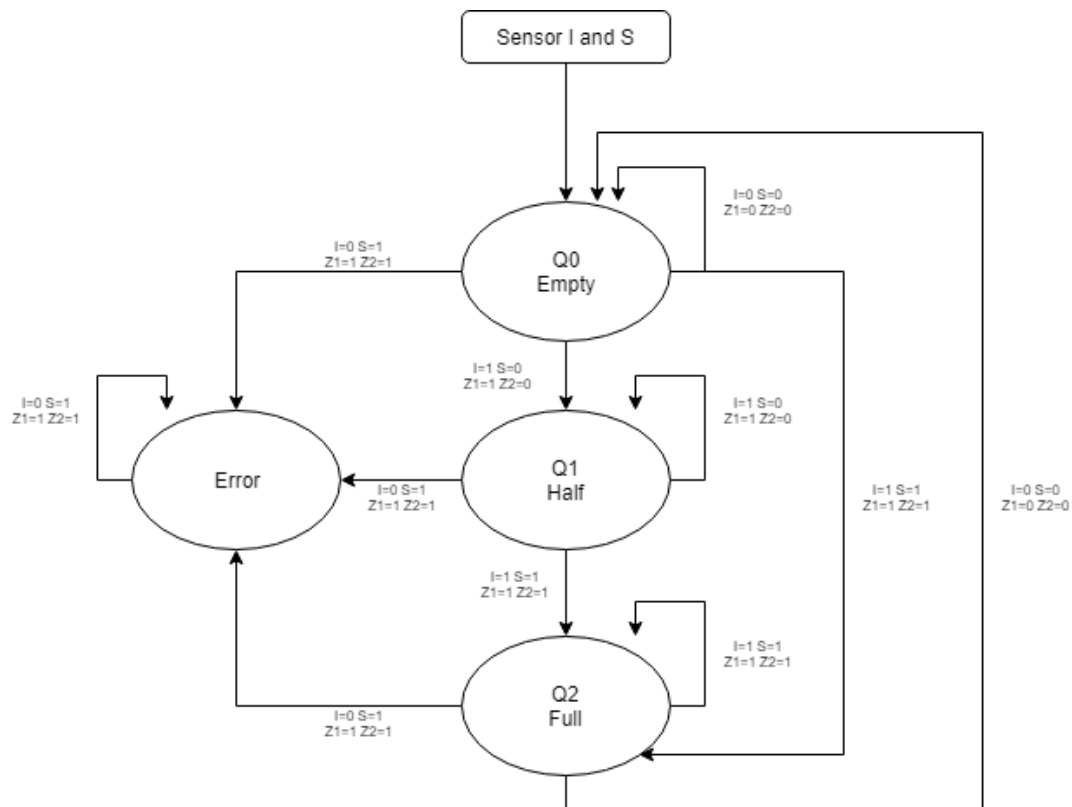


Figure 1.2: Exercise 1: Mealy state machine flow chart

Which is represented as follow:

State(Q)			Input(X)							
			I=0 S=0		I=0 S=1		I=1 S=0		I=1 S=1	
Representation	Q2	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2	Q1
Empty	0	0	0	0	0	1	1	0	1	1
Error	0	1	0	0	0	1	1	0	1	1
Half	1	0	0	0	0	1	1	0	1	1
Full	1	1	0	0	0	1	1	0	1	1
Output(Z)	Z1	Z2	0	0	1	1	1	0	1	1

Table 1.1: Exercise 1: Mealy state machine

So the logic circuit would be:

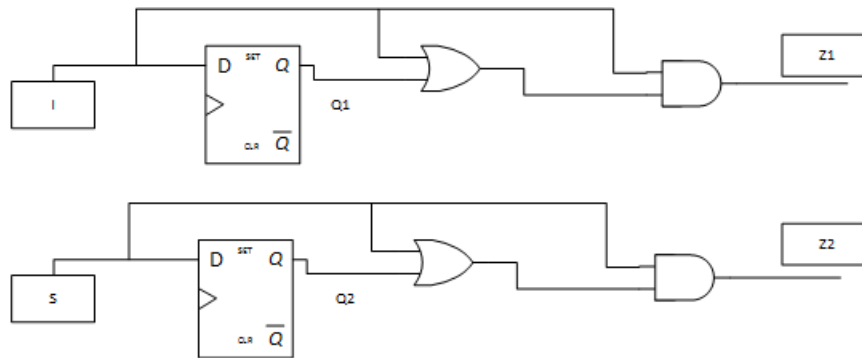


Figure 1.3: Exercise 1: Mealy logic circuit

We can notice that the input event and the output event are the same which could make the $Z_N = X_N$ with N: the output or input number, but as mention be in the Mealy state machine the output $Z = f(X_1, \dots, X_n, Q_1, \dots, Q_n)$, so we considered essential the use of state in the circuit is dependent with the state and the input to have a clear view of being a Mealy state machine.

1.1.1.1 SIMULATION

For the simulation of this stage machine, as the pump B1 and B2 alternate their function when $I = 1 \vee S = 0$ and for the activation of the pump that depends on output voltage is needed the following circuit is added:

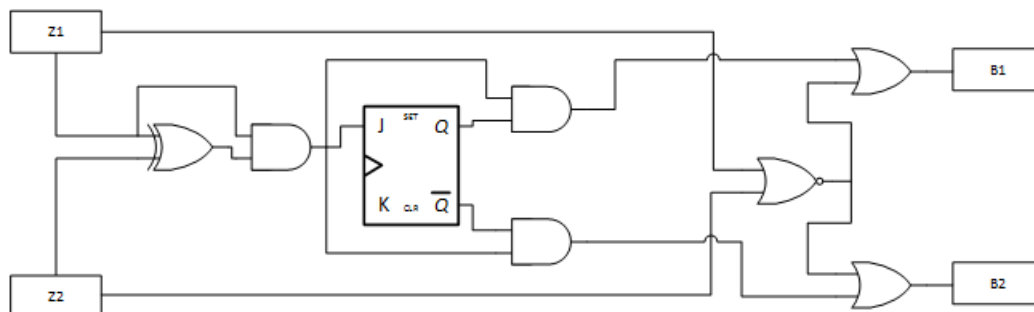


Figure 1.4: Exercise 1: Mealy additional logic circuit for the simulation

Simulation the complete circuit in Verilog and testing the possibles values of input in Gtkwave the result was:



Figure 1.5: [Exercise 1: Simulation results](#)

Esto es Y1

		AB			
		00	01	11	10
CD	00	0	0	0	1
	01	0	X	X	X
	11	0	X	X	X
	10	1	0	0	0

Y2

		AB			
		00	01	11	10
CD	00	0	0	0	1
	01	0	X	X	X
	11	1	X	X	X
	10	0	1	0	1

Y3

CD \ AB	AB			
	00	01	11	10
00	0	0	0	0
01	0	X	X	X
11	0	X	X	X
10	0	0	1	0

Z

C \ AB	AB			
	00	01	11	10
0	0	0	0	0
1	1	X	X	X