INSTITUTO TECNOLÓGICO DE BUENOS AIRES

Assignment N^o2

Electrónica 3 - 2018

Group 2:
Díaz Ian Cruz
Lin Benjamín
Müller Malena
Oh Victor

Professors:
Dewald Kevin
Wundes Pablo Enrique

November 14, 2018

1 Excercise 2: State Machines to Detect the sequence 1-1-0-1

In this exercise, the detection of the sequence 1-1-0-1 inside a longer sequence of bits, is done with a Moore's state machine and with a Mealy's state machine. The main difference between these two state machines is that in Moore's one, the output only depends on the present state of the machine, while in Mealy's one, the output depends on the present state as well as on the input. This causes a time displacement between the output of both state machines. Moore's output "answers" to the input one clock later after having reached the new state, while Mealy's output "answers" immediatly during the same clock that the input arrives. This is because Mealy's reacts not only according to the present state, but also depending on the input's value.
For the implementation of both state machines, five states are needed and they are represented with the letters from A to E:
- A (000): "IDLE", the state in which the first digit of the sequence has not yet been detected.
- B (001): The first digit of the sequence, "1", has arrived.
- C (010): The second digit of the sequence, "1", has arrived.
- D (011): The third digit of the sequence, "0", has arrived.
- E (100): The last digit of the sequence, "1", has arrived.

The states are digitally represented with three bits, as they allow to get five different combinations, so that the name of each state is represented with a binary number. Such representation is the one givin between parenthese, after the name of each state. It is important to mention that no matter which is the present state, whenever a "0" arrives from reset, the state changes to state A (IDLE).

1.1 Moore Type State Machine

In figure it is represented the sequence detection with the Moore's state machine.

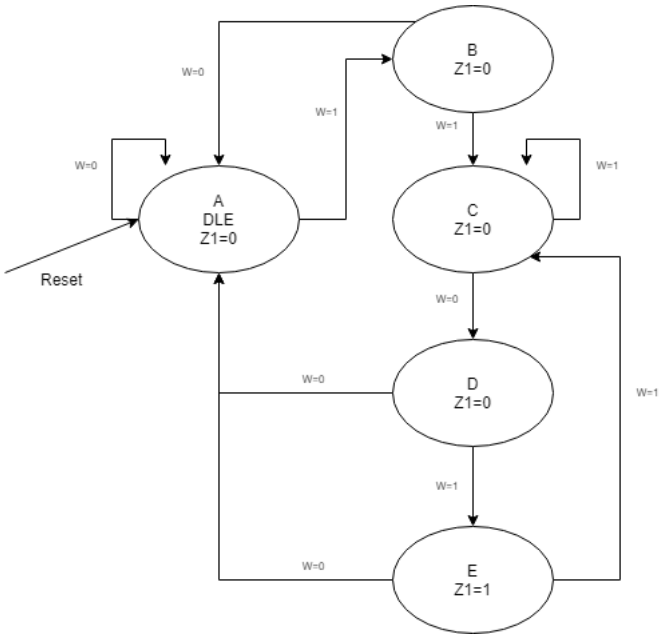

Figure 1.1: Moore's State Machine, for detecting the sequence 1-1-0-1.

From above's diagram (the one in figure 1.1), the following table 1.1 is obtained.

Present State	Next State		Output z
	w=0	w=1	
A	A	B	0
B	A	C	0
C	D	C	0
D	A	E	0
E	A	C	1

Table 1.1: Moore's Next States and Outputs.

The present state is represented as a 3 bit vector y: (y3,y2,y1) while the next state is represented as Y: (Y3,Y2,Y1). From the previous table 1.1 the following Karnaugh maps are used to get to simple logic expressions. The first Karnaugh map is to get Y1, the second one for Y2, the third one for Y3 and the last one for the output z.

w y3 \ y2 y1	00	01	11	10
00	0	0	0	1
01	0	X	X	X
11	0	X	X	X
10	1	0	0	0

w y3 \ y2 y1	00	01	11	10
00	0	0	0	1
01	0	X	X	X
11	1	X	X	X
10	0	1	0	1

w y3 \ y2 y1	00	01	11	10
00	0	0	0	0
01	0	X	X	X
11	0	X	X	X
10	0	0	1	0

y3 \ y2 y1	00	01	11	10
0	0	0	0	0
1	1	X	X	X

From the Karnaugh maps, we get to the following expressions:

$$Y1 = \overline{y1}(\overline{y2y3}w + y2\overline{w})$$

$$Y2 = y2\overline{y1} + w(y3 + \overline{y2}y1)$$

$$y3 = y1y2w$$

$$z = y3$$

1.2 Mealy Type State Machine

In figure 1.2 it is represented the sequence detection with the Mealy's state machine.

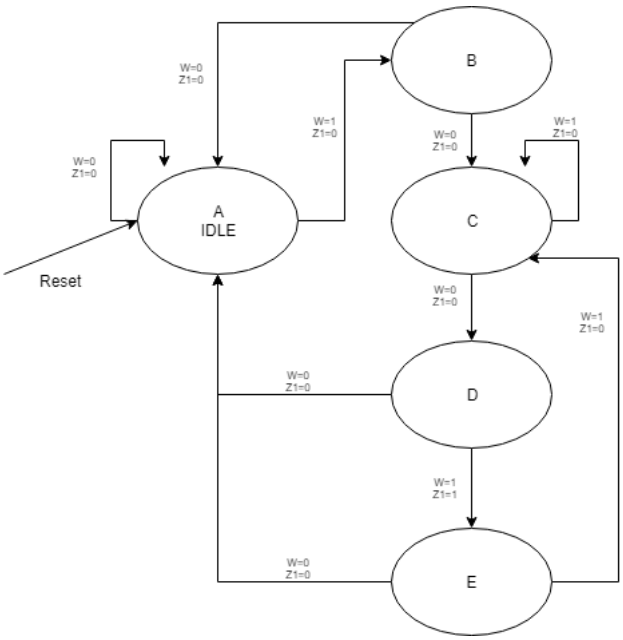

Figure 1.2: Mealy's State Machine, for detecting the sequence 1-1-0-1.

It can be seen how in this case, the transition between one state to another now also causes a change in the output. It doesn't wait to get to the new state in order to change it. The following table is obtained from above's diagram in figure 1.2 .

Present State	Next State		Output z depending on w	
	w=0	w=1	w=0	w=1
A	A	B	0	0
B	A	C	0	0
C	D	C	0	0
D	A	E	0	1
E	A	C	0	0

Table 1.2: Mealy's Next States and Outputs.

2 Exercise 3

For this exercise we were asked to implement the Moore machine shown on Figure 2.1, but with one condition, everything inside our machine should work on 3.3v and inputs and outputs should work on 5v logic.

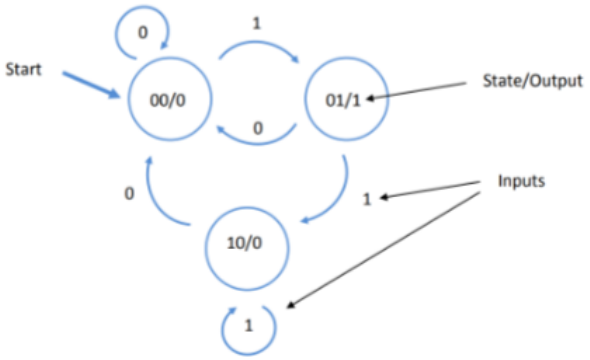

Figure 2.1: Moore Machine

2.1 State Machine Implementation

We proceeded to convert the diagram to a table that represents it, and we got Table 2.1, and by transforming each bit (Output, and next states bits) into a truth table, we could create our logic implementation for each bit. The Truth Tables are shown on Tables 2.2.

State	W=0	W=1	Output
00	00	01	0
01	00	10	1
10	00	10	0

Table 2.1: Moore Machine Table

S1 S0	Output
00	0
01	1
10	0
11	x

S1	S0	W	S1'	S0'
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	x	x
1	1	1	x	x

Table 2.2: Truth Tables

So by re-writing those truth tables we have got the following equations:

$$Output = S_1 . \bar{S_0} \tag{2.1}$$

$$S_1^{'} = \bar{S_1} S_0 w + S_1 \bar{S_0} w$$

$$S_0^{'} = \bar{S_1} \bar{S_0} w$$

So, by implementing those formulas into a synchronized logic circuit, we have got the Moore machine.

2.2 Level Converter Implementation

To convert the voltage levels on the PCB for compatibility, we decided to use 2N7000 Mosfet Transistor. We used it to implement an inverter with Open-Collector. By connecting the output to a pull-up network with the voltage we want, we can convert the level with no problems, form 5(v) to 3.3(v), and vice versa.
For the Pull-Up network, we decided to use a resistor $R = 1\,(k\Omega)$ so that when it's conected to ground, te current flowing through the inverter is less than $10\,(mA)$, and when the inverter produces a High Z, the resistor its not enough big to produce a High Z to the output, and set the output to a logic 1.

2.3 PCB Implementation

We proceeded to implement the PCB using Altium Designer, the Schematic for this Finite State Machine is shown on Figure 2.2. The Top and Bottom Layers are shown on Figure 2.3.

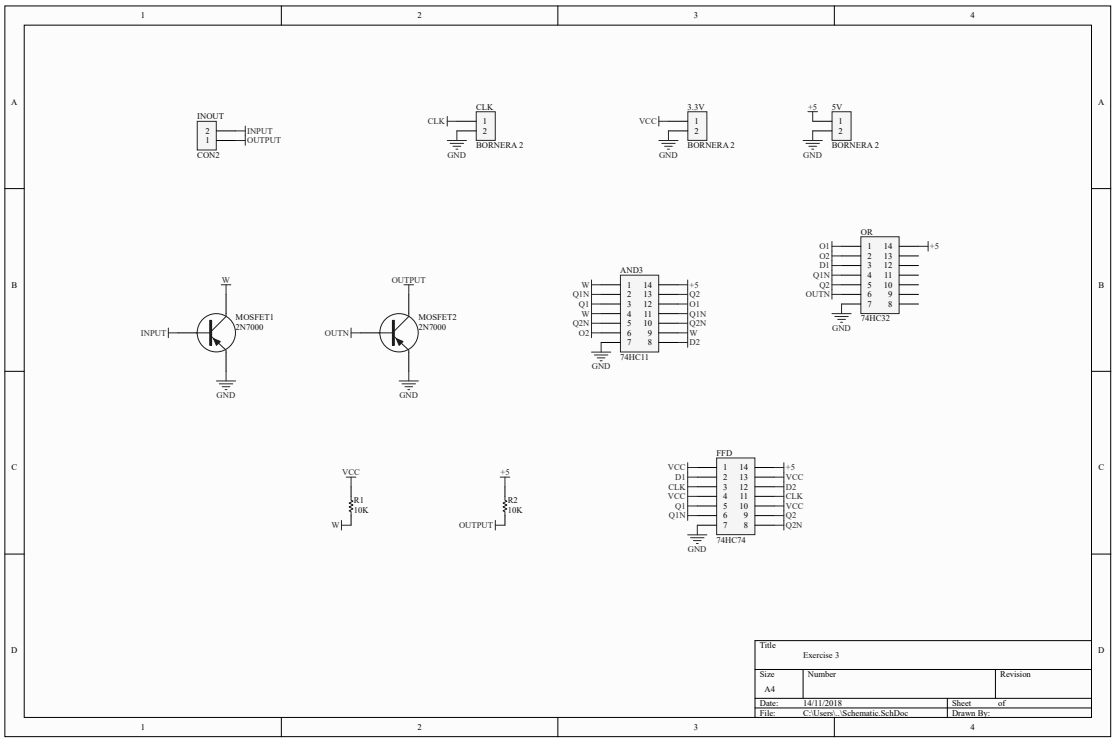

Figure 2.2: Schematic

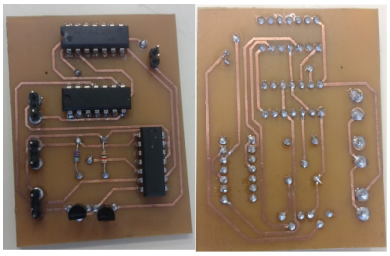

Figure 2.3: Printed Board

2.4 Mealy State Machine Re-Implementation

Finally, we were asked to re-implement the Moore State machine described in the previous Subsections, into a Mealy State Machine. As we know, Mealy Machines Outputs depend on states and inputs, different from Moore that only depends on states. So the truth tables for the next state, mantains its form and formula as the moore state machine, however, the output truth table, and by consequence, its formula , change ash shown on Table 2.5.

State	W=0	W=1
00	00/0	01/1
01	00/0	10/0
10	00/0	10/0

Table 2.3: Mealy State Machine

We can now easily see that in Table 2.3, states 01 and 10 are equal, so we can simplify those states into only one state. The final Table is shown on Table 2.4.

State	W=0	W=1
0	0/0	1/1
1	0/0	1/0

Table 2.4: Mealy Machine simplified

State	W	Output
0	0	0
0	1	1
1	0	0
1	1	0

Table 2.5: Output Truth Table

Finally, the formulas for the output and the next states are the following:

$$Output = \bar{St}.W$$

$$State = W$$

Implementing this would become someting like shown on Figure 2.4.

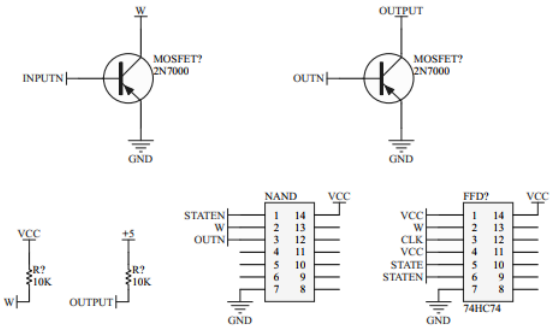

Figure 2.4: Schematic Mealy Machine

We builded this schematic in a breadboard, as shon on Figure 2.5.

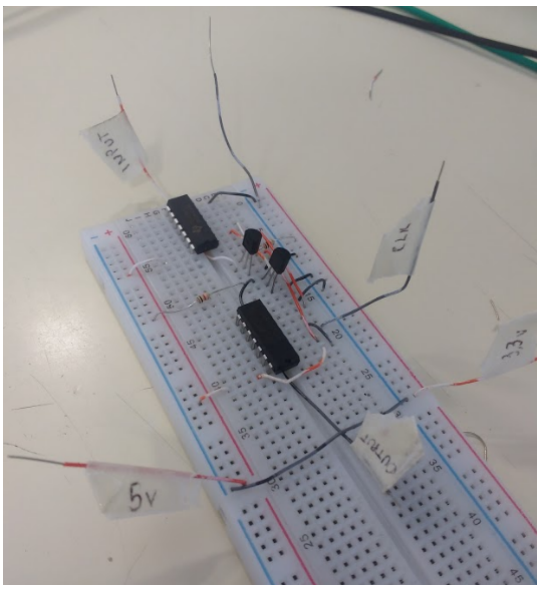

Figure 2.5: Mealy Implementation

2.5 Conclusions

By analizing the behaviour of both circuits, how they behave in the same test conditions, and comparing the amount of components used in both PCBs, we conclude that in this case, Mealy's implementation is more efficient because it utilizes less components and realizes the same operation. However, we need to clarify that not always Mealy's implementation is more efficient than Moore's, this depends on each state machine to implement.