

Task 3

In this section, is implemented a Moore's state machine already defined, as shown below.

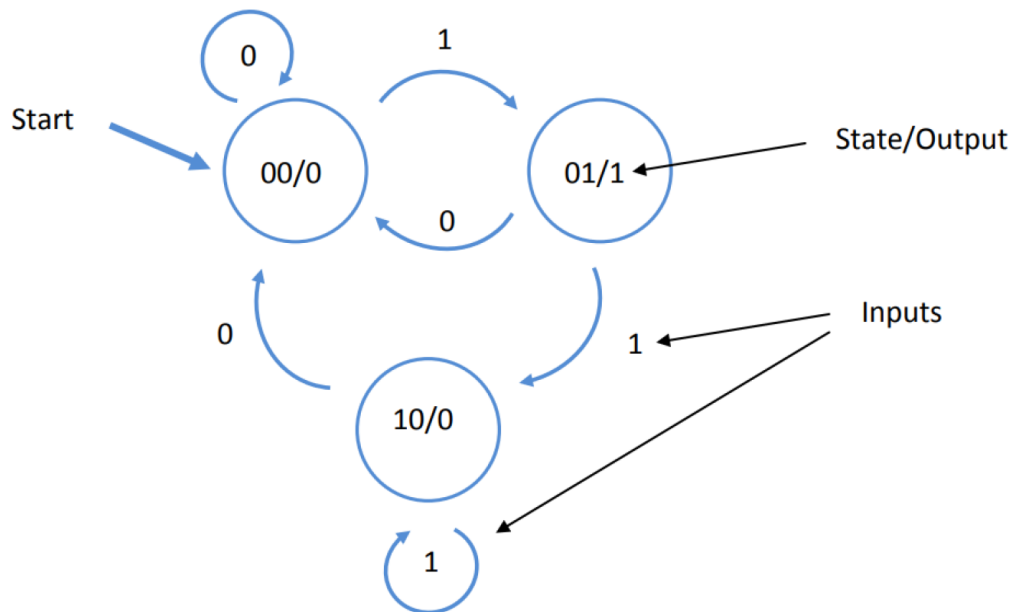


Figure 1: Moore state machine diagram

Using the diagram, the following table of transitions is made.

Estado Actual		Estado Siguiente		Salidas
	y2 - y1	W		Z
		0	1	
A	00	A	B	0
B	01	A	C	1
C	10	A	C	0

Figure 2: Moore state machine - Transitions

With the transitions, using Karnaugh's maps (see resolution in *Annex*), the functions for the states and the output result as follows: $Y_2 = W \cdot y_1 + W \cdot y_2$, and $Y_1 = W \cdot \overline{y_2} \cdot \overline{y_1}$.

From the transitions table, it is simple to see that $Z = y_1$. With the functions, the state machine is implemented using two D Flip Flops as follows.

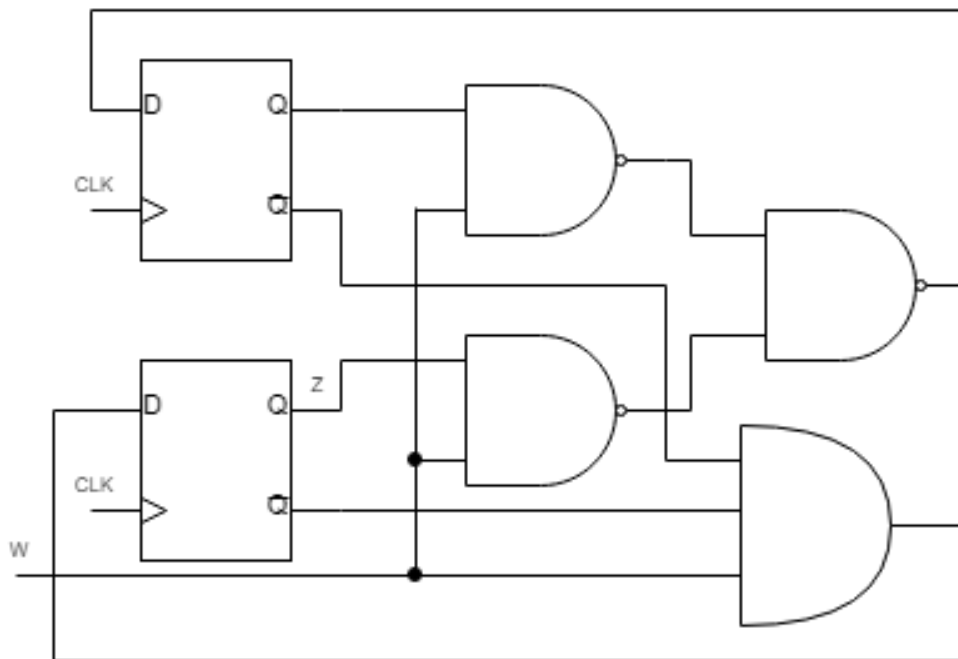


Figure 3: Moore state machine - Circuit implementation

Now the same system is implemented using a Mealy's state machine, with resulting diagram is shown below.

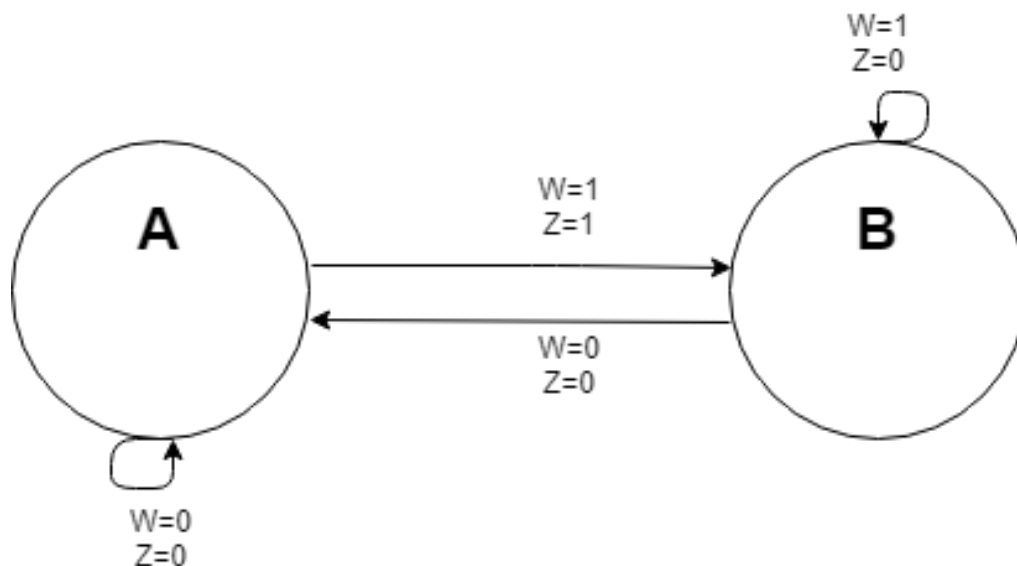


Figure 4: Mealy state machine diagram

Notice that it requires one less state than Moore's machine because of the direct connection of the from the input to the output.

The following transition table is made using the diagram.

Estado Actual		Estado Siguiente		Salidas	
	y	W		Z	
		0	1	W=0	W=1
A	0	A	B	0	1
B	1	A	B	0	0

Figure 5: Mealy state machine - Transitions

With the table, using Karnaugh's maps (see resolution in *Annex*), are made the functions for the states and the output as follows: $Y = W$, and $Z = \bar{y} \cdot W$. With the defined functions, the state machine is implemented using one D Flip Flop as shown below.

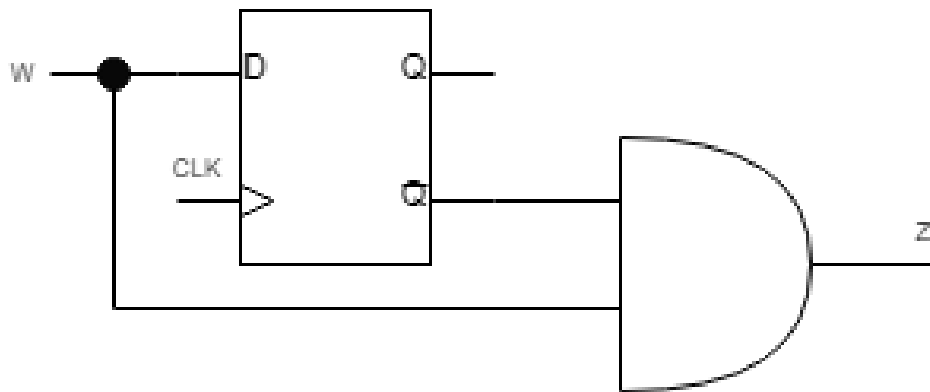


Figure 6: Mealy state machine - Circuit implementation

Since the internal logic works with 3.3V power supply, and the external signals work with 5V, level shifters are implemented using BJT transistors. For adapting the inputs of CLK and W, the circuits are shown below.

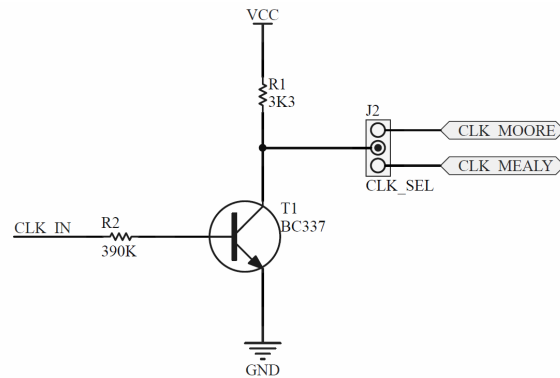


Figure 7: Level shifter for CLK from 5V to 3.3V (VCC)

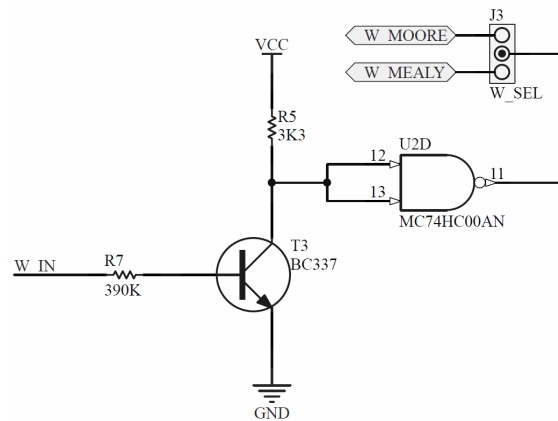


Figure 8: Level shifter for W from 5V to 3.3V (VCC). The inverting gate is to compensate the transistor logic inversion.

And for the outputs (Moore and Mealy machines) the driver circuit is as shown below.

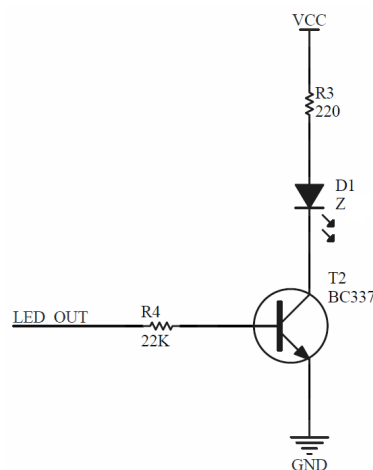


Figure 9: Driver for LED output.

Level shifter for inputs

From the implemented circuit:

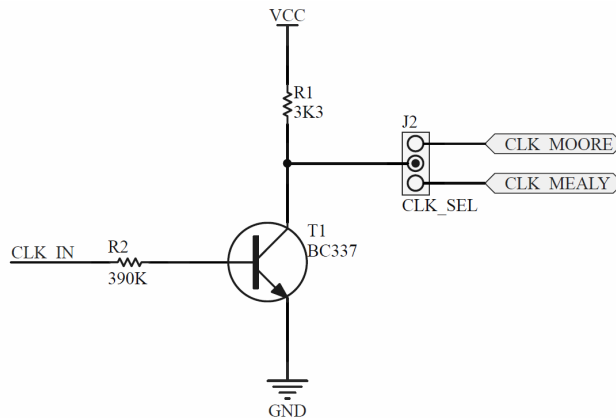


Figure 10: Level shifter for CLK from 5V to 3.3V (VCC)

Usign for $I_{SAT} = 1\text{mA}$, considering $VCE_{SAT} = 0.2\text{V}$, the equation from the out mesh:

$$3.3\text{V} - VCE_{SAT} - I_{SAT}R_1 = 0$$

$$\frac{3.3\text{V} - VCE_{SAT}}{I_{SAT}} = R_1 = 3.1\text{K}\Omega$$

Normalizing we have $R_1 = 3.3\text{K}\Omega$. Considering $HFE_{MIN} = 100$, from the input mesh:

$$5\text{V} - VBE_{ON} - \frac{I_C}{HFE_{MIN}}R_2 = 0$$

$$\frac{5\text{V} - VBE_{ON}}{I_C}HFE_{MIN} = R_2 = 430\text{K}\Omega$$

Normalizing we have $R_2 = 390\text{K}\Omega$.

Driver for output led

Taking the implemented circuit:

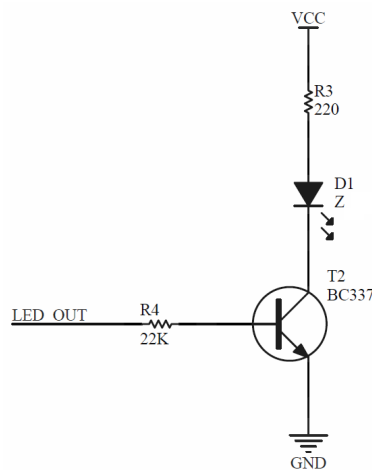


Figure 11: Driver for LED output.

Usign for $I_{LED} = 10mA$, considering $VCE_{SAT} = 0.2V$ and $V_{LED} = 2V$, the equation from the out mesh:

$$3.3V - V_{LED} - VCE_{SAT} - I_{LED}R_3 = 0$$

$$\frac{3.3V - V_{LED} - VCE_{SAT}}{I_{LED}} = R_3 = 110\Omega$$

Normalizing we have $R_3 = 220\Omega$. Considering $HFE_{MIN} = 100$, from the input mesh:

$$3.3V - VBE_{ON} - \frac{I_C}{HFE_{MIN}}R_4 = 0$$

$$\frac{3.3V - VBE_{ON}}{I_C}HFE_{MIN} = R_4 = 26K\Omega$$

Normalizing we have $R_4 = 22K\Omega$, to guarantee saturation.