

# Trabajo Práctico Final: Cronómetro en VGA

Electrónica III – 2018

Grupo 2:

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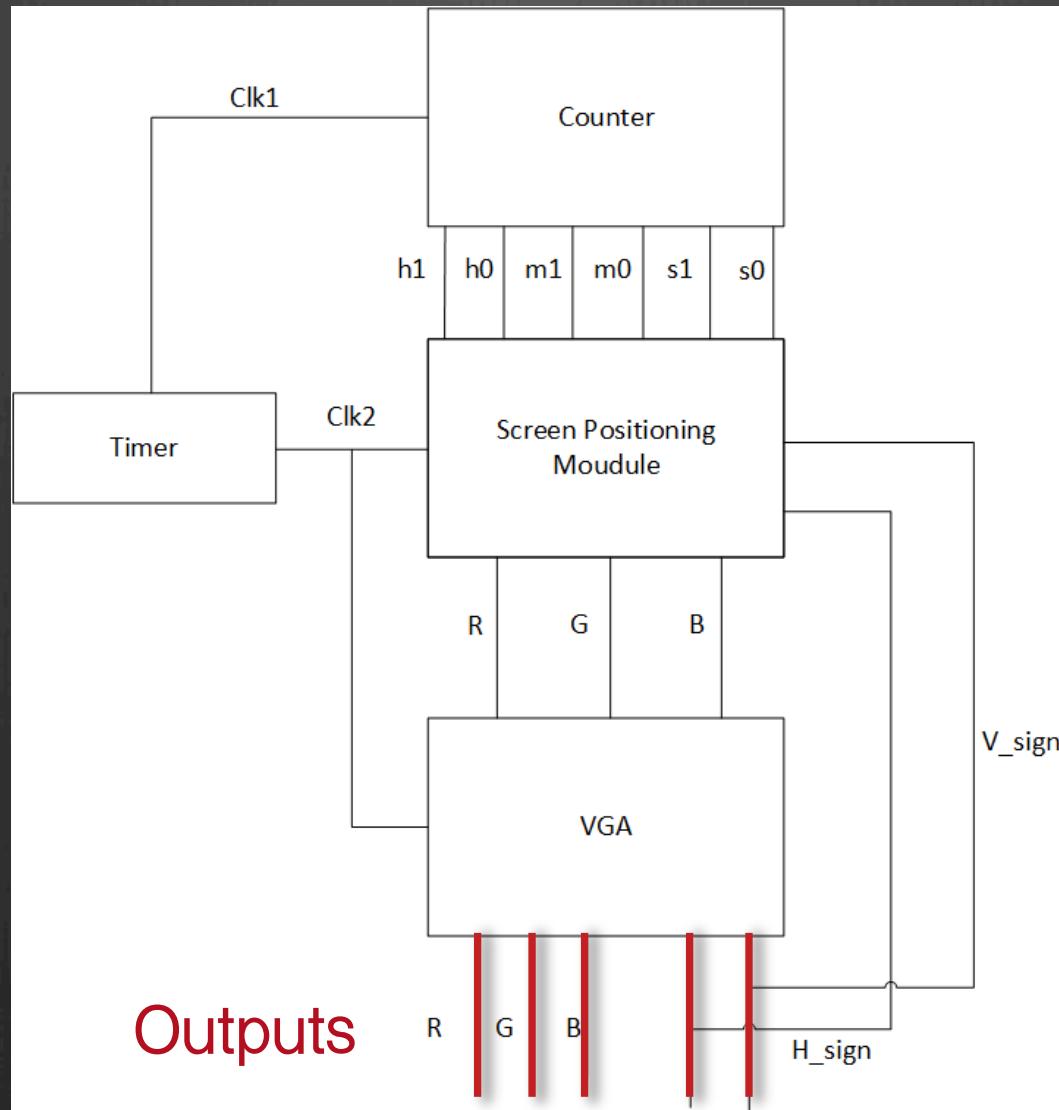
Oh Victor

Profesores:

Kevin Dewald

Pablo Wundes

# Modularización del proyecto



# Módulos en Verilog

- Clock\_50M\_to\_1k
- ScreenPositioningModule
- NumTo7Seg
- Contador\_final
- VGA
- ContadorN
- Vsync
- Count2watch
- Hsync
- Bin2bcd
- RGB

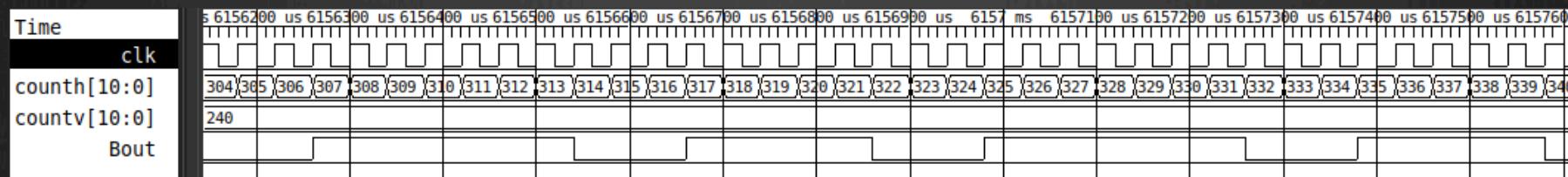
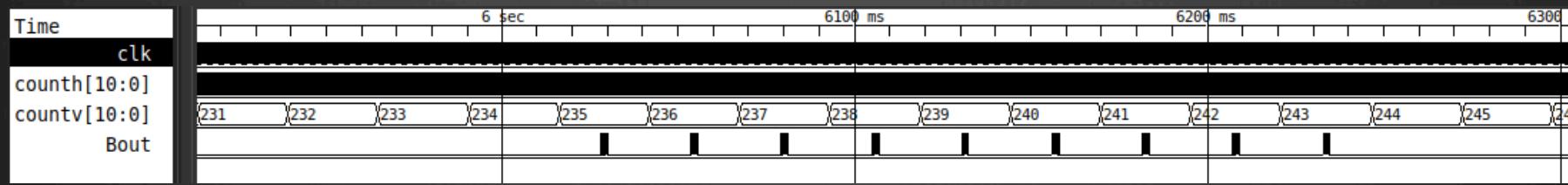
# Counter

## Simulación

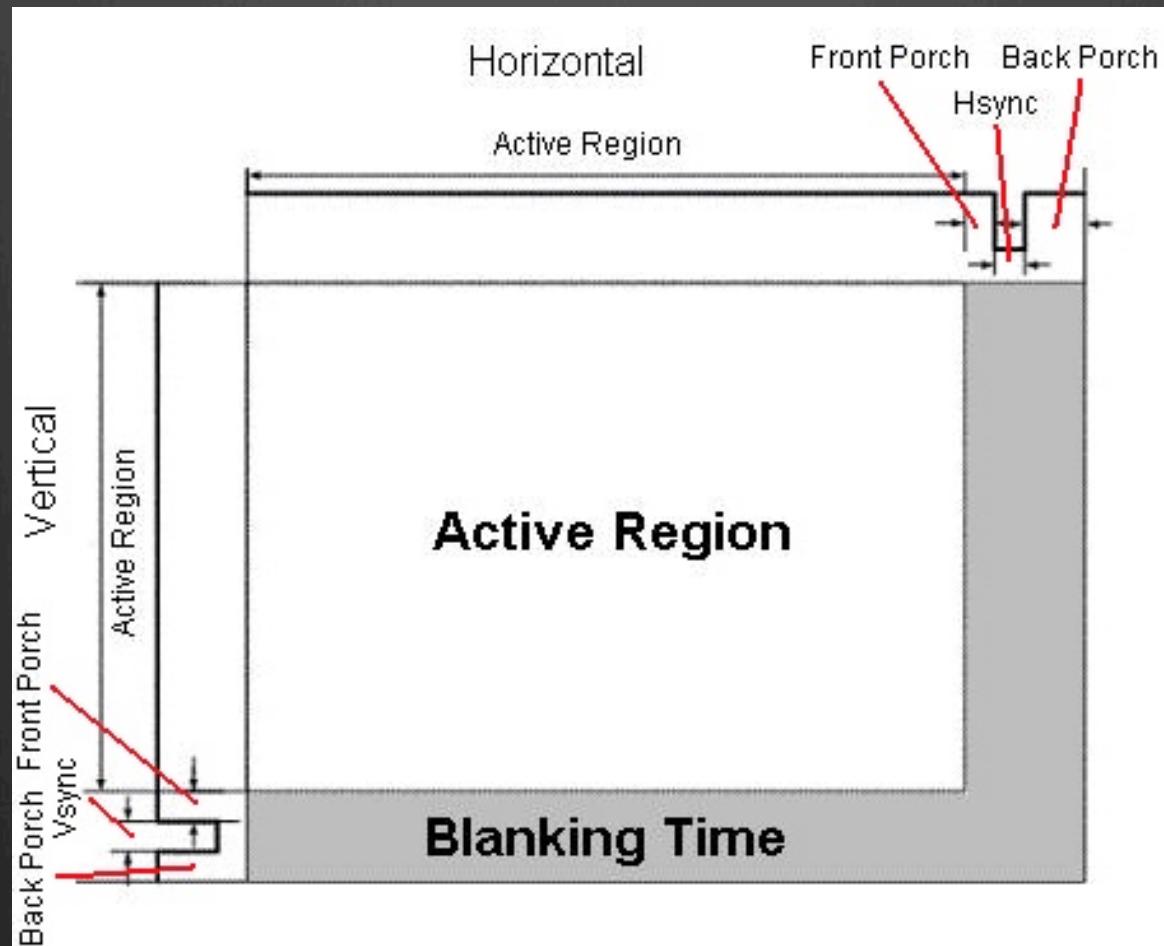
count	Bin_Out	BCD_Out
0	0: 0: 0:( 0)	0 0: 0 0: 0 0( 0 0 0)
1100	0: 0: 1:( 100)	0 0: 0 0: 0 1( 1 0 0)
7200000	2: 0: 0:( 0)	0 2: 0 0: 0 0( 0 0 0)
123548	0: 2: 3:( 548)	0 0: 0 2: 0 3( 5 4 8)
33954604	9:25:54:( 604)	0 9: 2 5: 5 4( 6 0 4)
963783	0:16: 3:( 783)	0 0: 1 6: 0 3( 7 8 3)
1368644	0:22:48:( 644)	0 0: 2 2: 4 8( 6 4 4)
53154214	14:45:54:( 214)	1 4: 4 5: 5 4( 2 1 4)

# Screen Positioning Module

## Simulaciones



# VGA



# VGA

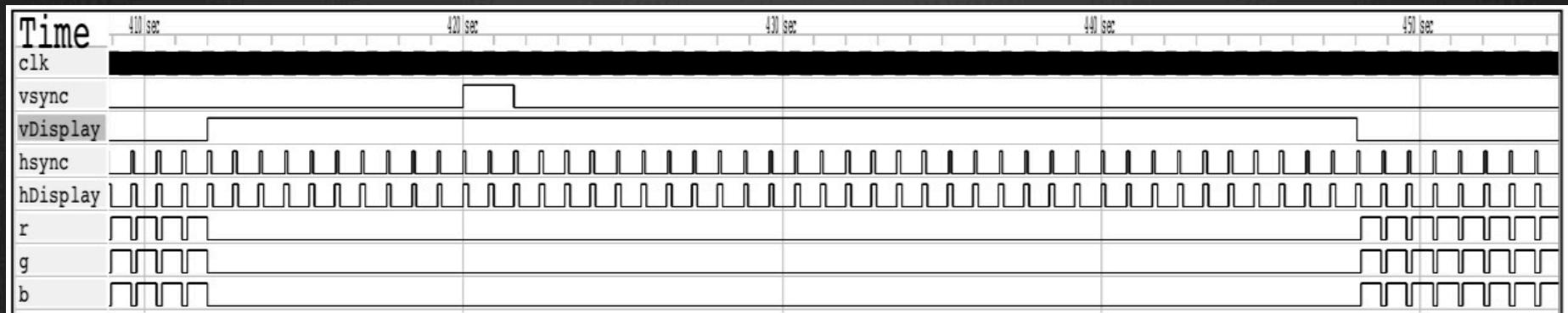
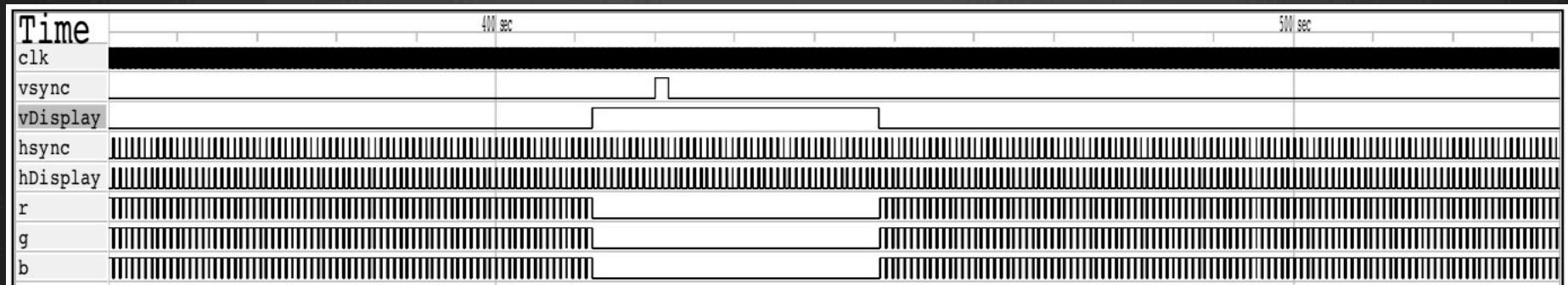
- Resolución: 640x480.
- Frecuencia de refresco de pantalla: 60 Hz.

VERTICAL	Pixels
Sync Pulse	2
Back Porch	33
Display	480
Front Porch	10
Whole Frame	525

HORIZONTAL	Pixels
Sync Pulse	96
Back Porch	48
Display	640
Front Porch	16
Whole Line	800

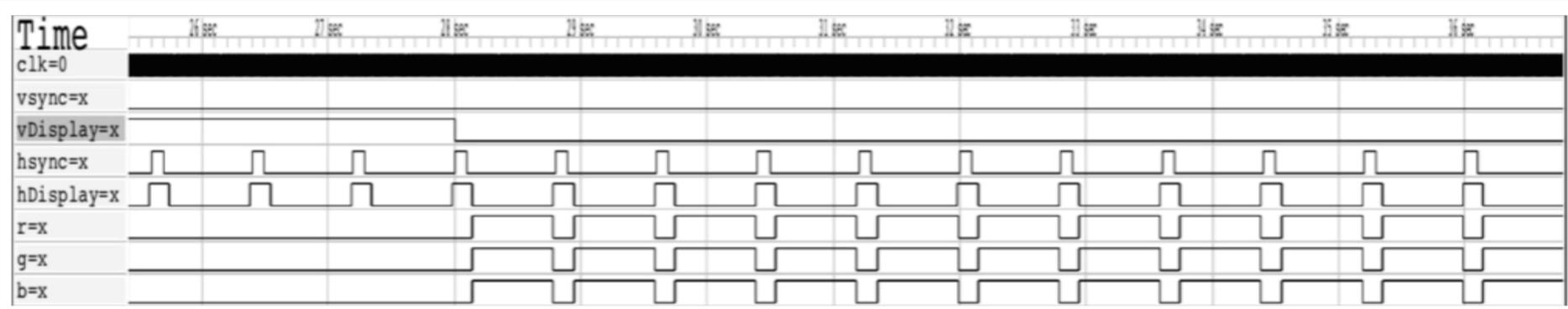
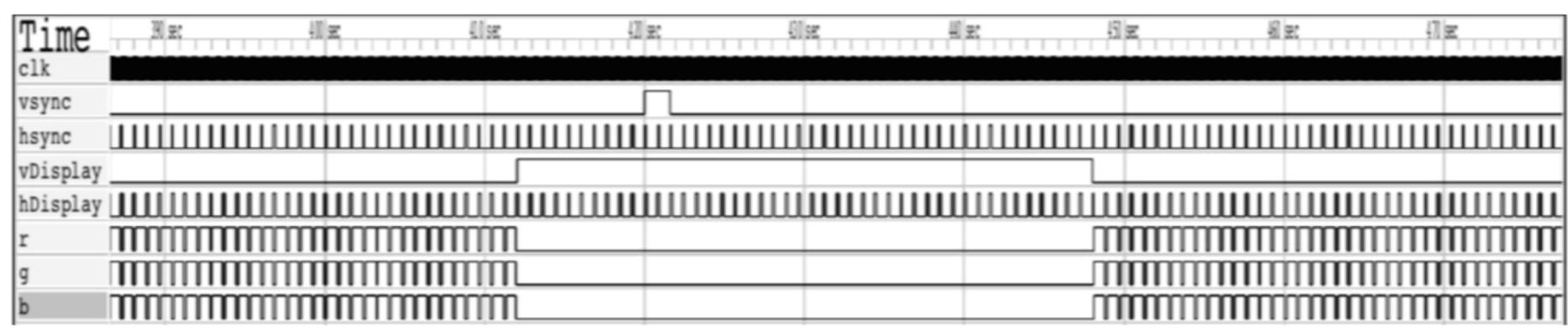
# VGA

## Simulaciones



# VGA

## Simulaciones



# Resultado Final

000021

000019