INSTITUTO TECNOLÓGICO DE BUENOS AIRES

Trabajo Práctico Final

NOWIK, Ariel 58309
MASPERO, Martina 57120
MESTANZA, Joaquin 58288
REGUEIRA, Marcelo 58300
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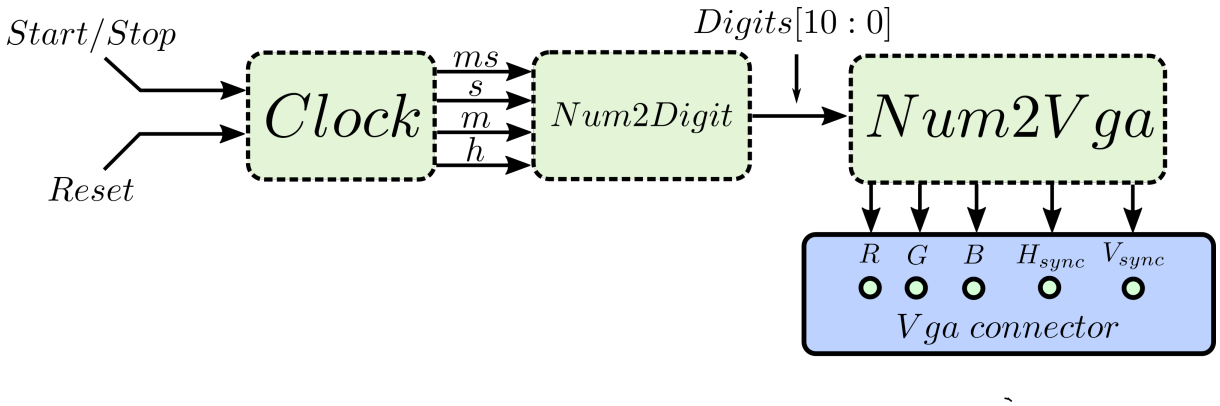
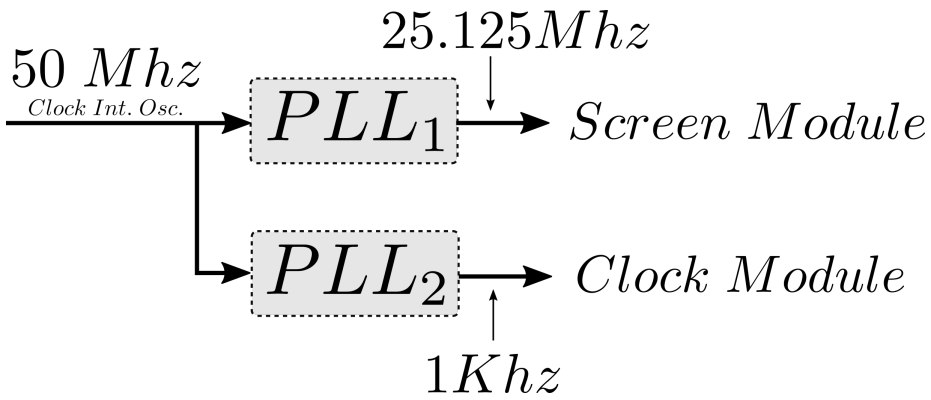
Module structure



The project is organized in three modules:

1. Clock module: handles the clock reset/start/stop actions (via Buttons), and counts milisecconds, seconds, minutes and hours.
2. Number to digit module: Receives the numbers from the clock and converts them to digit codes.
3. Digit to Screen module: Gets the numbers and handles the Vga protocol.

Clock syncronization



The project uses FPGA internal 50Mhz oscillator. Using two PLLs, the different frequencies needed for each module is generated

Clock Module

This module gets as input