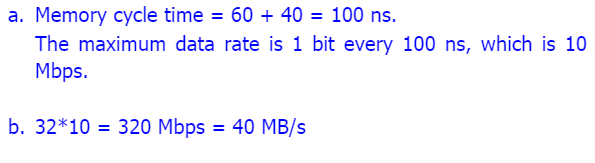
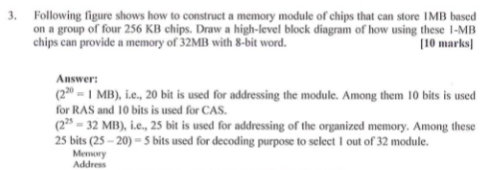
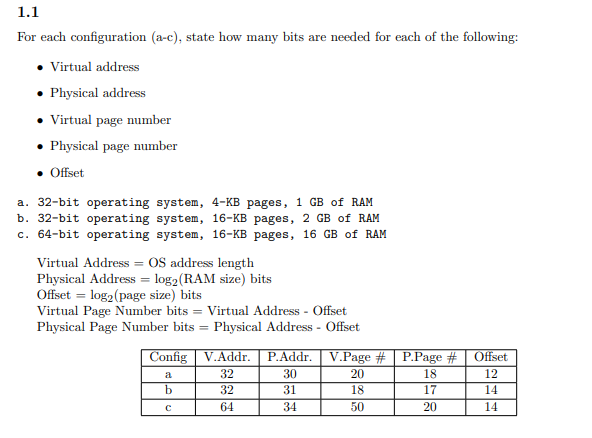
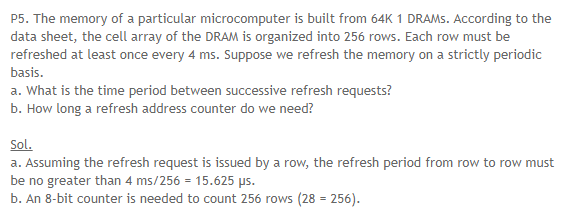


2. Figure 5.16 shows a simplified timing diagram for a DRAM read operation over a bus. The  
access time is considered to last from t1 to t2. Then there is a recharge time, lasting from  
t2 to t3, during which the DRAM chips will have to recharge before the  
processor can access them again.  
a. Assume that the access time is 60 ns and the recharge time is 40 ns. What is the  
memory cycle time? What is the maximum data rate this DRAM can sustain,  
assuming a 1-bit output?  
b. Constructing a 32-bit wide memory system using these chips yields what data  
transfer rate?





Design a 16-bit memory of total capacity 8192 bits using SRAM chips of size 64 1 bit. Give  
the array configuration of the chips on the memory board showing all required input and  
output signals for assigning this memory to the lowest address space. The design should  
allow for both byte and 16-bit word accesses.

answer

