1) Consider a system including a CPU with 20 lines of address (A0-A19) and 8 lines of data (D0-D7). Draw schematics for memory mapping and CPU connections in "Fully-Decoding" method with given memory chips below.

- **a.** 512K8 (all of memory)
- **b.** 64K8 (all of memory)
- **c.** 128K4 (all of memory)
- **d.** First half 128K8 – Second half 256K8

2) Consider a system including a CPU with 20 lines of address (A0-A19) and 16 lines of data (D0-D15). Draw schematics for memory mapping and CPU connections in "Fully-Decoding" method with given memory chips below.

- **a.** 1M8 (all of memory)
- **b.** First half 1M8 – Second half 1M4
- **c.** First quarter 64K16 – Second half 256K8
- **d.** First quarter 128K8 – Third quarter 64K8

3) Calculate "speed up" in a 5 stage pipeline CPU which every stage has different time. Stage durations: 20, 15, 25, 20, 20.

4) Consider a system with 2 levels of cache memory. CPU has 20 address lines (A0-A19) and 8 data lines(D0-D7). Main memory is 1M8 and cache memories in both levels are 4K8. Main memory has an access time of 100ns. L1 cache memory access time is 10ns and it has a hit rate of 90%. L2 cache memory access time is 20ns and has a hit rate of 80%. Memory controller has a delay of 30ns.

- **a.** Draw the schematic (including memory controller)
- **b.** Calculate effective Time.
- **c.** The L1 memory is swapped with another cache memory (still 4K8) which has an access time of 5ns with 95% hit rate. But we also change main memory to a new one with 110ns access time. Calculate new access time. Will it be faster or slower?

5) Let's compare a CISC machine versus a RISC machine on a benchmark. Assume the following characteristics of the two machines:

- CISC: CPI of 4 for load/store, 3 for ALU/branch and 10 for call/return, CPU clock rate of 3.5 GHz.
- RISC: CPI of 1.3 (the machine is pipelined, the ideal CPI is 1.0, but overhead and stalls make it 1.3) and a CPU clock rate of 1.75 GHz.

Since the CISC machine has more complex instructions, the IC for the CISC machine is 30% smaller than the IC for the RISC machine. The benchmark has a breakdown of 38% loads, 10% stores, 35% ALU operations, 3% calls, 3% returns and 11% branches. Which machine will run the benchmark in less time and by how much?

(Hint: CPU time = IC * CPI * Clock cycle time)

6) Assume a program with 820,000,000 instructions is needed for spell checking of a very large file. There are 4 types of instructions in this program and each type needs N clock cycle for execution.

Instruction Class	Clock cycles per Instructions	Number of Instructions
Branch	3	150,000,000
Store	4	185,000,000
Load	5	260,000,000
ALU/R-type	4	225,000,000

Duration of complete run of the program is 1.57 seconds. Find out clock cycles time of execution in this computer.

7) In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

`alu`	`beq`	`lw`	`sw`
45%	20%	20%	15%

a. What is the clock cycle time in a pipelined and non-pipelined processor?
b. What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
c. Assuming there are no stalls or hazards, what is the utilization of the data memory?

If you have any questions regarding this assignment, feel free to contact us.

Please submit your homework, simulations and projects in the following format:

Name_StudentNumber_HW2 (BillGates_12345678_HW2)

Good Luck!