DOCUMENTATION

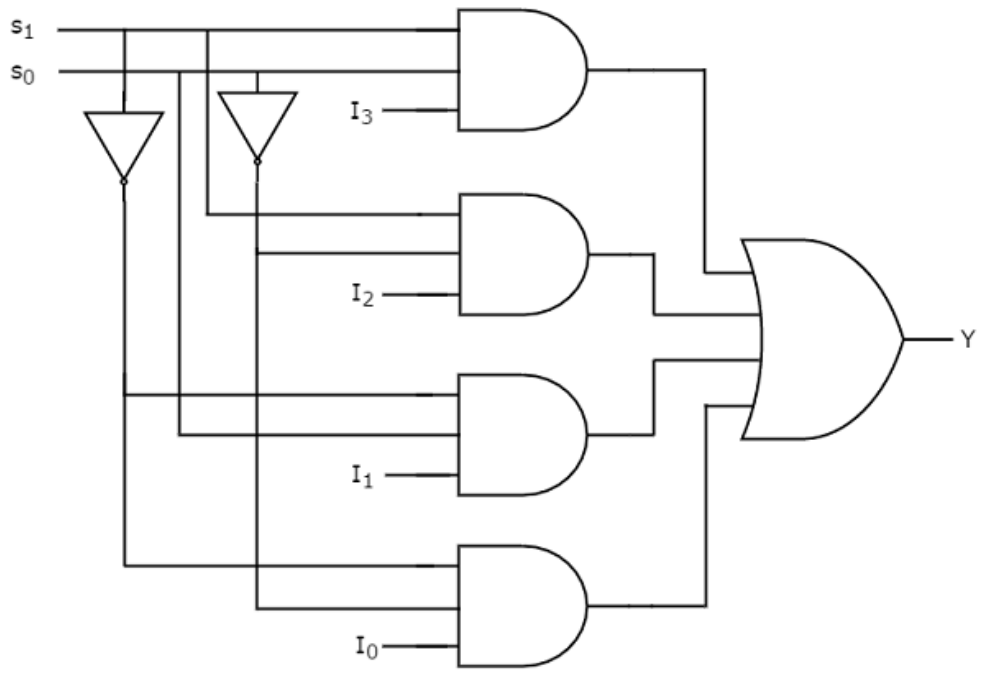
AIM

To Construct a 4*1 Multiplexer that consists of 4 parallel inputs and a single output, that is then connected to a D-Flip Flop as a clock input.

SHORT DESCRIPTION

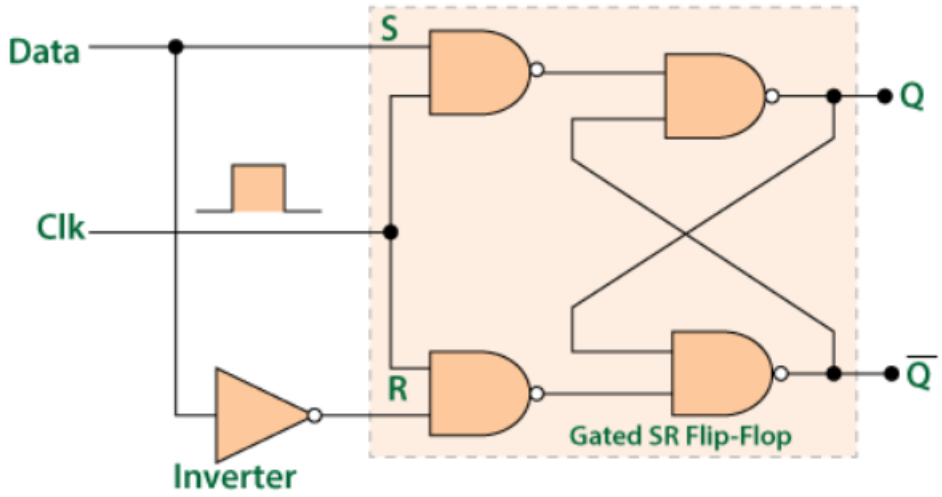
Implementation of this multiplexer and D- Flip Flop is done Using Multiple quantum Gates. The input for this circuit is 4 bits. The following code is a generalized one.

CLASSICAL MULTIPLEXER

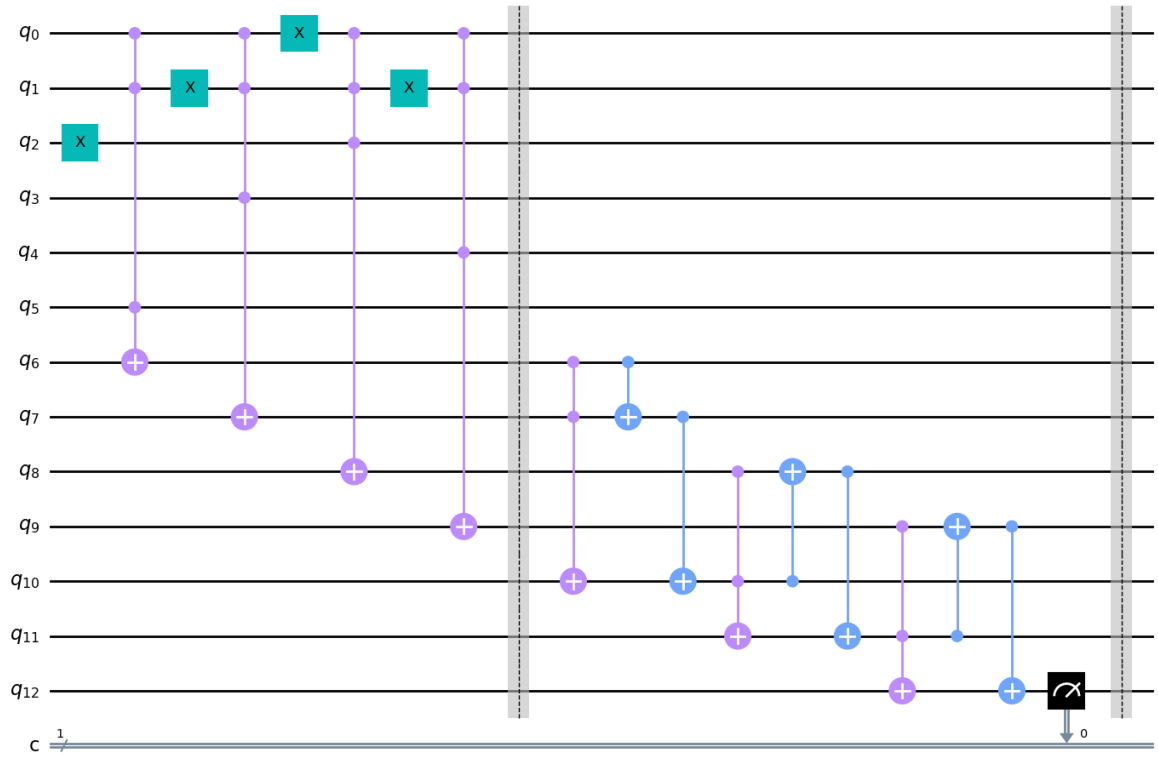


Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

CLASSICAL D FLIP FLOP

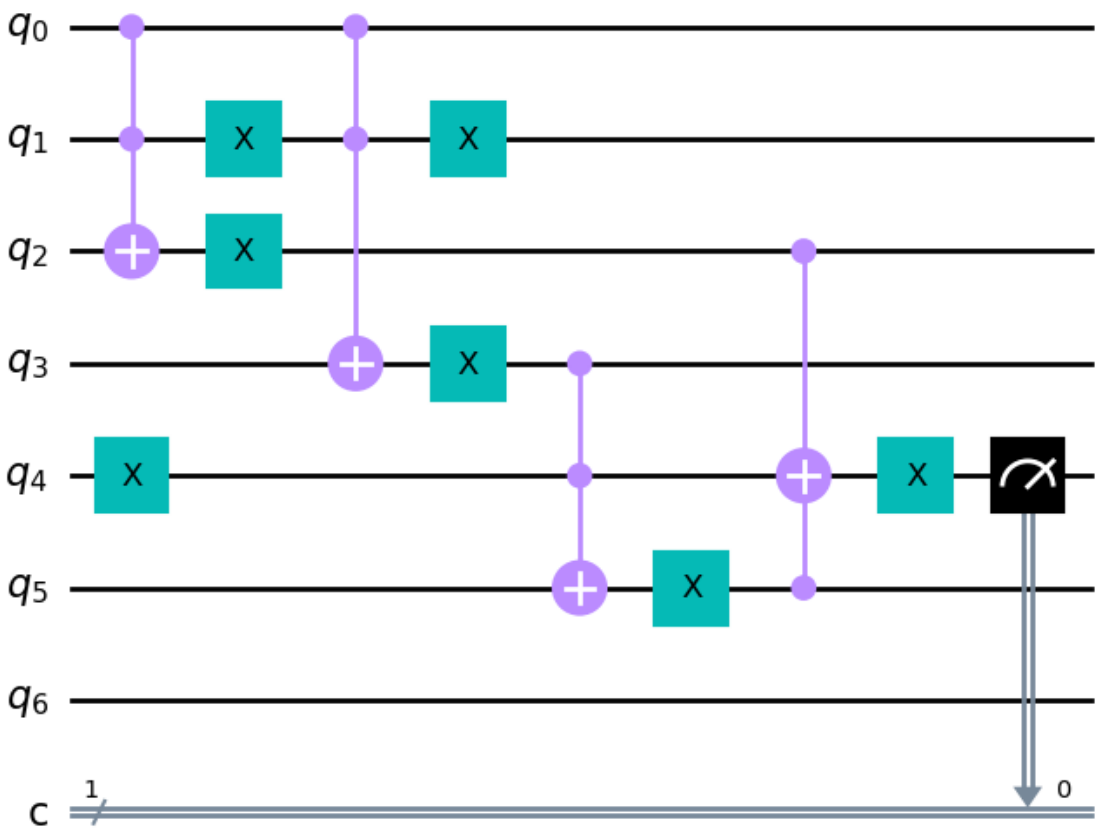


Clock	D	Q	Q′
↓ » 0	0	0	1
↑ » 1	0	0	1
↓ » 0	1	0	1
↑ » 1	1	1	0



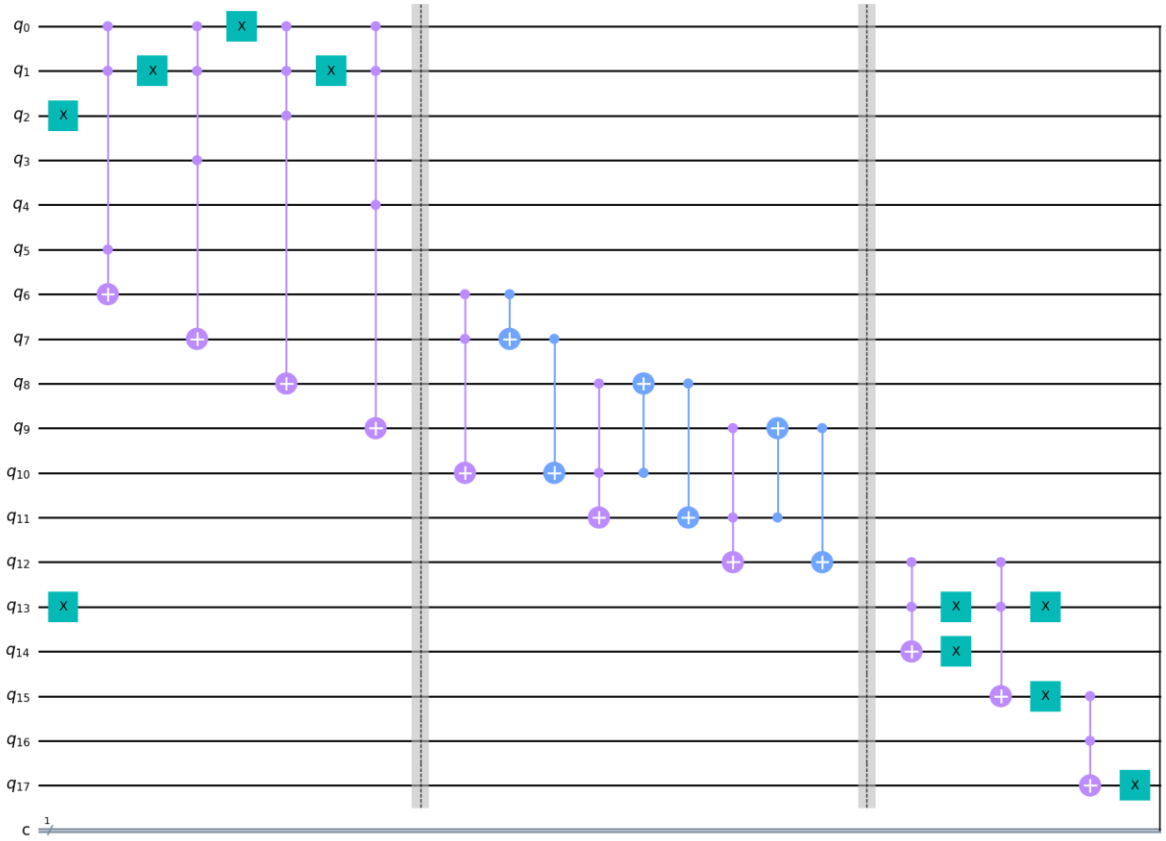
OUTPUT:1

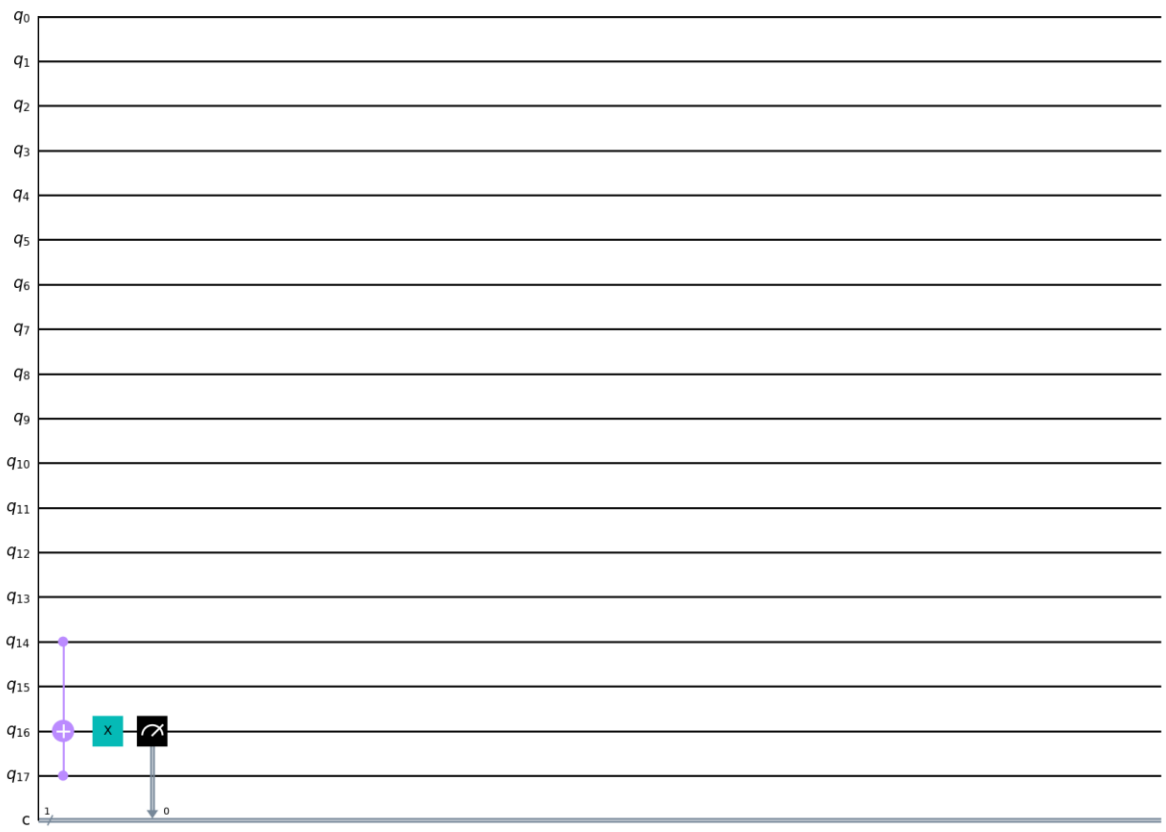
D Flip Flop



OUTPUT: 0

COMPLETE CIRCUIT:





SAMPLE TESTCASES

INPUT:

S0,S1,I0,I1,I2,13,D,Q

0010000000000100100

OUTPUT:

1

THINGS LEARNED

- To reduce the depth of circuit.
- Tried a new experiment of connecting two different classical circuits and producing a single output.

REFERENCES

- **https://www.tutorialspoint.com/digital_circuits/digital_circuits_multiplexers.htm**
- **https://www.electronicsforu.com/technology-trends/learn-electronics/flip-flop-rs-jk-t-d**
- **https://arxiv.org/abs/1807.02940#:~:text=Distributing%20entangled%20pairs%20is%20a,pair%20of%20remote%20quantum%20memories.**
- **https://www.irjmets.com/uploadedfiles/paper//issue_5_may_2022/22088/final/fin_irjmets1651928209.pdf**