Started on Wednesday, 9 December 2020, 9:00 AM

State Finished

Completed on Wednesday, 9 December 2020, 9:28 AM

Time taken 28 mins 44 secs **Marks** 13.00/20.90

Grade 6.22 out of 10.00 (62.2%)

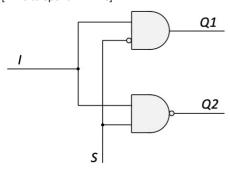
Question **1**

Incorrect

Mark 0.00 out of 1.50

Consider a logic circuit depicted below. *I* denotes an input pin, *S* - a selector pin, and *Q1* and *Q2* - output pins. Which digital device from the list below corresponds to a depicted logic circuit?

[Time to spend: 2 mins]



Select one:

- Multiplexer
- Demultiplexer X
- Encoder
- Decoder
- None of the listed

Your answer is incorrect.

The correct answer is: None of the listed

Question 2

Correct

Mark 0.80 out of 0.80

Do you agree that some special-purpose MIPS processor registers are not directly addressable?

[Time to spend: 1 min]

Select one:

■ True

False

The correct answer is 'True'.

Question 3
Correct
Mark 1.00 out of 1.00
Northbridge/Couthbridge computer expliteature love at identifies the major chipsets, pamed as Couth Bridge and North Bridge De Vou
Northbridge/Southbridge computer architecture layout identifies two major chipsets, named as South Bridge and North Bridge. Do you agree that South Bridge, unlike North Bridge, is the one directly connected to the CPU, as it should provide a fast communication between
the CPU and peripheral computer devices?
[Time to spend: 1 min]
[Time to opend. 2 min]
Select one:
○ Agree
Totally disagree ✓
Your answer is correct.
The correct answer is: Totally disagree
Question 4
Correct
Mark 1.00 out of 1.00
Do you agree that all modern processor exhitectures, such as Intel vOC ADM, and MIDC assume Van Noumann computer Architecture?
Do you agree that all modern processor architectures, such as Intel x86, ARM, and MIPS, assume Von Neumann computer Architecture?
[Time to spend: 1.5 min]
Select one:
True ✓
○ False
⊎ i disc
The correct answer is 'True'.

Question **5**

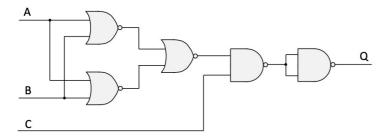
Correct

Mark 1.50 out of 1.50

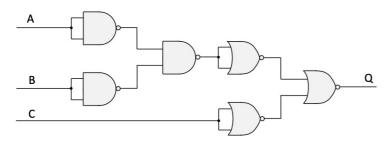
Are two logical circuits depicted below equivalent?

[Time to spend: 3 mins]

Circuit 1



Circuit 2



Select one:

- Yes

 ✓
- O No

Your answer is correct.

The correct answer is: Yes

Question 6

Correct

Mark 1.00 out of 1.00

Do you agree that, as opposed to a sequential digital circuit, the output of a combinational digital circuit depends only on its current inputs, but not on its past inputs?

[Time to spend: 2 mins]

Select one:

- True
- False

The correct answer is 'True'.

Correct Mark 1.00 out of 1.00 Do you agree that a processor register with a storage capacity of 8 bits consists of 16 flip-flops? [Time to spend: 1 min] Select one: True False ✓ The correct answer is 'False'. Question 8 Correct Mark 1.00 out of 1.00
Do you agree that a processor register with a storage capacity of 8 bits consists of 16 flip-flops? [Time to spend: 1 min] Select one: True False ✓ The correct answer is 'False'. Question 8 Correct
[Time to spend: 1 min] Select one:
[Time to spend: 1 min] Select one:
Select one: ○ True ○ False ✓ The correct answer is 'False'. Question 8 Correct
True False ✓ The correct answer is 'False'. Question 8 Correct
 True False ✓ The correct answer is 'False'. Question 8 Correct
● False ✔ The correct answer is 'False'. Question 8 Correct
The correct answer is 'False'. Question 8 Correct
Question 8 Correct
Question 8 Correct
Correct
Correct
Correct
Recall MIPS32 R-type instructions. Why "rs", "rt", and "rd" R-type instruction fields are 5 bits long?
[Time to spend: 2 mins]
Select one:
 No choice is correct
Because every MIPS32 register has a storage capacity of 32 bits
Because MIPS32 processors have 32 registers ✓
Your answer is correct.
The correct answer is: Because MIPS32 processors have 32 registers
Ouestion 9
Question 9 Incorrect

Your answer is incorrect.

The correct answer is: No choice is correct

Exam Quiz: Attempt review

The correct answer is: Agree

Question 12
Partially correct
Mark 0.83 out of 1.25
Choose valid statements for a CPU cache: [Time to spend: 2 mins] Select one or more: □ Different cores of the same processor might share L2 or L3 cache □ CPU L1, L2, or L3 cache provides a faster access to data, as compared to the main system memory ✓
☑ CPU cache, depending on a cache level (L2, L3, etc.), can be implemented as a physically separate chip from a CPU chip ✓
□ No choice is correct
Your answer is partially correct. You have correctly selected 2. The correct answers are: CPU L1, L2, or L3 cache provides a faster access to data, as compared to the main system memory, Different cores of the same processor might share L2 or L3 cache, CPU cache, depending on a cache level (L2, L3, etc.), can be implemented as a physically separate chip from a CPU chip
Question 13
Correct
Mark 0.75 out of 0.75
Do you agree that ARM and MIPS are both the examples of complex instruction set computers (CISC)?
[Time to spend: 0.5 min]
Select one:
○ True
False ✓

The correct answer is 'False'.

1/23, 9:30 PM	Exam Quiz: Attempt review
Question 14	
Correct	
Mark 0.80 out of 0.80	
Choose a CPU component from the list below, which is responsib data, from an external memory unit, such as cache or the main sy	le for fetching instructions to be executed by a CPU, as well as any other stem memory.
[Time to spend: 0.5 min]	
Select one:	
Control Unit ✓	
Register File	
 Floating-Point Coprocessor 	
Arithmetic-Logical Unit	
Many an arrangia a arrang	
Your answer is correct.	
The correct answer is: Control Unit	
Question 15	
Correct	
Mark 0.90 out of 0.90	
What is a "register spilling" in the context of MIPS instruction set a	architecture?
[Time to spend: 0.5 min]	
Select one:	
 The transfer of some live variables from registers to other me 	emory, due to the lack of registers❤
The use of multiple registers to store double precision floating	
The use of registers for purposes they are not originally desi	gnea tor

Your answer is correct.

The correct answer is: The transfer of some live variables from registers to other memory, due to the lack of registers

Question 16				
Partially correct				
Mark 0.67 out of 1.00				
Choose valid statements for the main system memory of modern personal computers:				
[Time to spend: 1.5 min]				
Select one or more:				
It belongs to DRAM memory type				
☐ Its typical read/write access speed exceeds a CPU clock speed				
☐ Its typical storage capacity is a few megabytes				
■ No choice is correct				
☑ It provides a faster access speed as compared to a remote SSD disk				
☐ It supports direct addressing of data				
☐ It is non-volatile				
Your answer is partially correct.				
You have correctly selected 2.				
The correct answers are: It supports direct addressing of data, It belongs to DRAM memory type, It provides a faster access speed as				
compared to a remote SSD disk				
Question 17				
Correct				
Mark 0.75 out of 0.75				
Convert decimal number "144" into the octal numeric system:				
[Time to spend: 1 min]				
Answer: 220				
Answer: 220				

The correct answer is: 220

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Oı	restion	1	റ

Incorrect

Mark 0.00 out of 1.20

What is the primary goal of MESI coherence protocol?

[Time to spend: 2 mins]

Select one:

- To support data communication between CPU and GPU
- No choice is correct
- To speed-up data exchange between a CPU cache and the peripheral storage devices
- To maximise the overall hit cache ratio for a CPU

Your answer is incorrect.

The correct answer is: No choice is correct

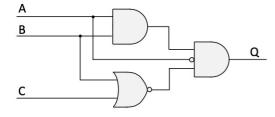
Question 19

Incorrect

Mark 0.00 out of 1.50

Consider the combinational logic circuit below having 3 input pins, A, B, and C. What is the value of output Q?

[Time to spend: 3.5 min]



Select one:

- (A+B)*(B+C)
- 0
- 0 1
- No choice is correct X

Your answer is incorrect.

The correct answer is: 0

Question 20
Correct
Mark 1.00 out of 1.00
Choose J-type MIPS instructions from the list below:

[Time to spend: 1.5 min]

Select one or more:

sb

- ☑ No choice is correct
 ✓
- addi
- sub
- div
- Ih
- add

Your answer is correct.

The correct answer is: No choice is correct