Started on	Tuesday, 15 September 2020, 4:30 PM
State	Finished
Completed on	Tuesday, 15 September 2020, 4:42 PM
Time taken	11 mins 54 secs
Grade	**4.25** out of 10.00 (**42.5**%)

Question **1**

Partially correct

Mark 0.50 out of 1.00

Choose the factors, which cannot not increase the execution time of a program:

Select one or more:

- [x] Decreasing the number of memory access operations (assume that the program functionality is not affected) ✔
- [ ] Increasing the storage capacity of an L1 CPU cache
- [ ] Increasing the CPU frequency
- [ ] Increasing the duration (length) of a CPU cycle
- [ ] No factors listed will affect the execution time of a program

The option "Increasing the storage capacity of an L1 CPU cache" is not considered in the grading (although is correct as well); the details will be discussed later in the course

You have correctly selected 1.
The correct answers are: Decreasing the number of memory access operations (assume that the program functionality is not affected), Increasing the CPU frequency

Question **2**

Incorrect

Mark 0.00 out of 1.00

Order the major stages of a translation hierarchy from a high-level language program into machine code:

Stage 1: loader ✖

Stage 2: linker ✖

Stage 3: assembler ✖

Stage 4: compiler ✖

Your answer is incorrect.

The correct answer is: Stage 1: → compiler, Stage 2: → assembler, Stage 3: → linker, Stage 4: → loader

Question 3

Incorrect

Mark 0.00 out of 1.00

What principle(s) do(es) not comply with Von Neumann computer architecture?

Select one or more:

- a. No choice is correct
- b. Programs and data are stored in different physical memory units
- c. Programs and data are stored in the same physical memory unit ✖
- d. Program instructions are executed sequentially ✖

Your answer is incorrect.

The correct answer is: Programs and data are stored in different physical memory units

Question 4

Incorrect

Mark 0.00 out of 1.00

Do you agree that all modern general-purpose CPUs have exactly 5 stages in a pipelined execution of CPU instructions?

Select one:

- a. Totally agree ✖
- b. Completely disagree!

Your answer is incorrect.

The correct answer is: Completely disagree!

Question 5

Correct

Mark 1.00 out of 1.00

Do you agree that, according to "a memory wall problem", the key performance bottleneck of modern computer platforms is a slow memory access speed, rather than a slow CPU speed?

Select one:

- True ✔
- False

The correct answer is 'True'.

Question 6

Partially correct

Mark 0.75 out of 1.00

Every CPU has several key components, including Control Unit (CU), Arithmetic Logic Unit (ALU), and registers. Match the functionalities below to the respective CPU components:

Stores the result of an arithmetic operation	Register(s) ✔
Stores the arguments for arithmetic operations	No choice is correct ✖
Performs arithmetic and logic operations	ALU ✔
Directs the CPU operation, such as determines the next instruction to be executed	CU ✔

Your answer is partially correct.

You have correctly selected 3.

The correct answer is: Stores the result of an arithmetic operation → Register(s), Stores the arguments for arithmetic operations → Register(s), Performs arithmetic and logic operations → ALU, Directs the CPU operation, such as determines the next instruction to be executed → CU

Question 7

Incorrect

Mark 0.00 out of 1.00

What is the primary goal for a pipelined execution of CPU instructions?

Select one or more:

- a. Increase of the CPU reliability ✖
- b. Optimisation of the CPU energy consumption ✖
- c. Optimisation of a program runtime ✔
- d. No choice is correct

Your answer is incorrect.

The correct answer is: Optimisation of a program runtime

Question 8

Correct

Mark 1.00 out of 1.00

There are several levels of caches in a memory hierarchy, such as L1, L2, and L3. What are the primary differences between them?

Select one or more:

- [x] an access speed
- [x] storage capacity
- [x] some cache levels are embedded into a CPU chip, while others - outside of a CPU chip
- [ ] No choice is correct

Your answer is correct.

The correct answers are: an access speed, storage capacity, some cache levels are embedded into a CPU chip, while others - outside of a CPU chip

Question 9

Incorrect

Mark 0.00 out of 1.00

Recall the key stages of a translation hierarchy from a high-level programming language into machine code.

Do you agree that there is a one-to-one correspondence between assembly and machine language instructions, that is one assembly instruction always corresponds to the same machine instruction, and vice versa, assuming that CPU and its instruction set remain unchanged.

Select one:

- ( ) Indeed, this is a case!
- (•) Completely disagree! Multiple optimisations are applied, to increase program performance, which lead to the violation of such a one-to-one correspondence ✖

Your answer is incorrect.

The correct answer is: Indeed, this is a case!

Question 10

Correct

Mark 1.00 out of 1.00

When a program is adapted to run on multiple processors in a multiprocessor system, the execution time on each processor is comprised of computing time and the overhead time required for locked critical sections and/or to send data from one processor to another. Assume a program requires t = 100 s of execution time on one processor. When run p processors, each processor requires t/p s, as well as an additional 4 s of overhead, irrespective of the number of processors. Compute the corresponding speedup of running a program on 4 processors relative to a single processor case. Round your answer to "X.XX" format.

Answer: 3.45

The correct answer is: 3.45