Started on	Thursday, 29 October 2020, 12:40 PM
State	Finished
Completed on	Thursday, 29 October 2020, 1:30 PM
Time taken	49 mins 53 secs
Marks	25.04/47.00
Grade	**5.33** out of 10.00 (**53.28**%)

Question **1**

Partially correct

Mark 1.50 out of 2.00

Recall several communication bus protocols used to support data exchange in computer platforms. Choose the most appropriate protocol for each use case below.

Complexity: average

Time to spend: 2 mins

Data exchange between CPU registers and its L1 cache	On-Chip Peripheral Bus protocol ✔
Data exchange between main system memory and SSD	Peripheral Component Interconnect Express ✔
To connect BIOS Flash ROM to Southbridge chipset	Peripheral Component Interconnect Express ✖
Data exchange between an external USB flash drive and a computer	Universal Serial Bus protocol ✔

Your answer is partially correct.

You have correctly selected 3.

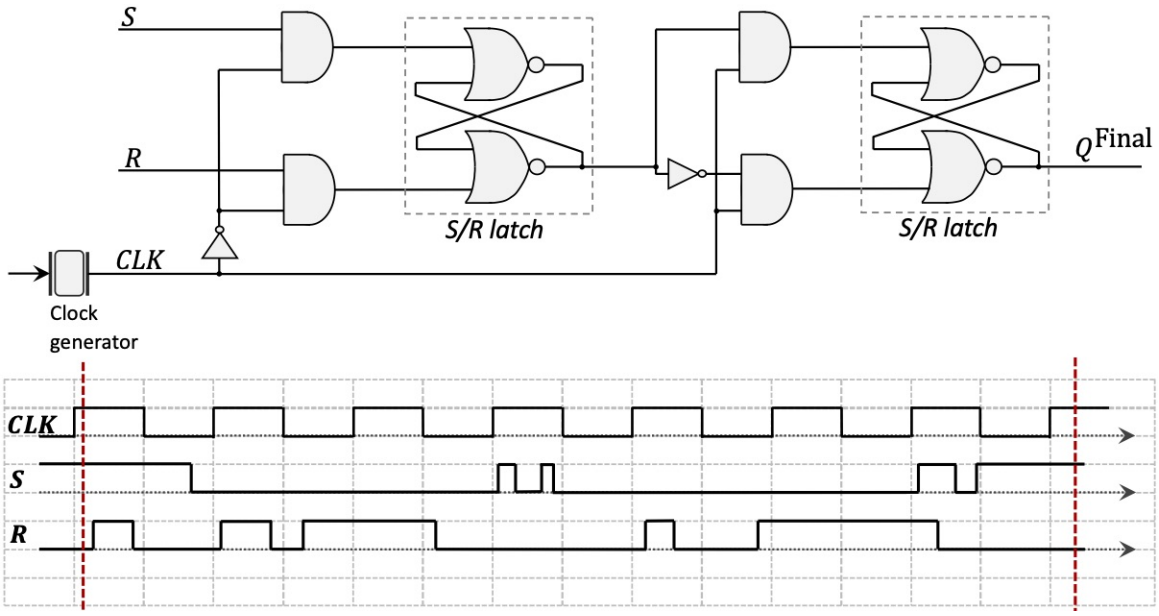
The correct answer is: Data exchange between CPU registers and its L1 cache → On-Chip Peripheral Bus protocol, Data exchange between main system memory and SSD → Peripheral Component Interconnect Express, To connect BIOS Flash ROM to Southbridge chipset → Low Pin Count bus protocol, Data exchange between an external USB flash drive and a computer → Universal Serial Bus protocol

Question 2

Incorrect

Mark 0.00 out of 4.00

Consider a digital circuit depicted below. Observe the presence of two S/R latches connected in a cascaded way. Assume that input signals denoted by S and R change over time according to the diagrams depicted below the digital circuit diagram. How many times the output Q^Final will change its value over a time interval marked with red boundaries?



Complexity: higher

Time to spend: 6 min

Answer: 7 ✖

The correct answer is: 2

Question 3

Correct

Mark 1.00 out of 1.00

What is/are the key differences between 32- and 64-bit processors?

Complexity: average

Time to spend: 1 min

Select one or more:

- a. No choice is correct
- b. The number of processor registers
- c. The storage capacities of processor registers ✔

Your answer is correct.

The correct answer is: The storage capacities of processor registers

Question 4

Correct

Mark 3.00 out of 3.00

What are the values stored in registers $t0 and $t1, respectively, after executing the code below:

```
# Pseudocode:
# if (a < b + 6)
# a = a + 2
# else
# a = a + 1
# b = b + a
# Register mappings:
# a: $t0, b: $t1


        addi $t2, $t1, 6
        blt $t0, $t2, then
        addi $t0, $t0, 2
        j end
then:   addi $t0, $t0, 1
end:    add $t1, $t1, $t0
```

Complexity: average

Time to spend: 5 min

Select one:

- The result of a program execution is unpredictable ✔
- 0x20000000 and 0x10000000
- No choice is correct
- 0x00000001 and 0x00000002
- 0x00000002 and 0x00000002

As studied during the classes, MIPS registers are reset to 0, before instructions execution, and the correct answer should be 0x00000001 and 0x00000001, meaning that "No choice is correct".

However, as an exception only, this time we give points for the option "The result of a program execution is unpredictable" as well; however, this option would be correct only if MIPS registers would have initial random values (what is not a case).

If you rely on the pseudocode, instead of the program code, the correct answer is 0x00000002 and 0x00000002. We consider this answer as correct as well.

The correct answers are: 0x00000002 and 0x00000002, No choice is correct, The result of a program execution is unpredictable

Question 5

Complete

Mark 1.00 out of 4.00

Compare the worst-case propagation delays for a X-to-Y multiplexor and X-to-Y encoder. Justify, either they must be the same, or different. Keep your answer clear and very short.

After you write down your answer, check it again, and try to make it shorted, by removing any unnecessary words. Grading will consider your writing style as well.

Complexity: higher

Time to spend: 6 mins

they will be the same because both of them are combinational logic and they are time-independent

Comment:

Question 6

Correct

Mark 1.50 out of 1.50

Do you agree that the number of CPU registers does not affect the CPU clock frequency?

Complexity: average

Time to spend: 2 min

Select one:

- Agree
- Totally disagree ✔

Your answer is correct.

The correct answer is: Totally disagree

Question 7

Correct

Mark 1.50 out of 1.50

What is the key idea behind a cache-oblivious programming?

Complexity: average

Time to spend: 2 mins

Select one:

- To optimise program code (e.g. by reordering program instructions) in such a way, that less energy is consumed by a CPU cache
- To parallelise a program execution upon multiple CPU cores, with each CPU having its own separate cache
- To optimise program code, aiming at reducing the total execution time of a program, by exploring the specifics of a CPU cache of a target hardware platform ✔
- No choice is correct

Your answer is correct.

The correct answer is: To optimise program code, aiming at reducing the total execution time of a program, by exploring the specifics of a CPU cache of a target hardware platform

Question 8

Correct

Mark 1.50 out of 1.50

Do you agree with the following statement?

An arithmetic-logic unit (ALU) of a typical general-purpose processor is usually implemented by means of a synchronous logic circuit, with a primary objection of increasing the overall CPU runtime performance?

Complexity: simpler

Time to spend: 1 min

Select one:

- True
- False ✔

The correct answer is 'False'.

Question 9

Partially correct

Mark 0.75 out of 1.50

Choose valid statements for a 32-bit MIPS processor from the list below.

Complexity: average

Time to spend: 1 min

Select one or more:

- [ ] No choice is correct
- [x] Each register is 32 bits in storage size ✔
- [x] Each register is reserved for a specific purpose, like storing return values from ALU, or the code of an instruction, etc. ✔
- [x] It has 32 registers in total, including the registers of its floating-point coprocessor ✖

Your answer is partially correct.

You have selected too many options.
The correct answers are: Each register is 32 bits in storage size, Each register is reserved for a specific purpose, like storing return values from ALU, or the code of an instruction, etc.

Question 10

Correct

Mark 1.50 out of 1.50

There are several levels of CPU caches available, including L1, L2, and L3. Choose the primary differences between them:

Complexity: average

Time to spend: 2 mins

Select one or more:

- [x] Storage capacity ✔
- [x] Physical implementation: some caches (e.g. L1) is embedded into the CPU chip, while other caches might be implemented as physically separate chips ✔
- [ ] Different memory types: L1 is SRAM, while others are DRAM
- [ ] Different volatility: L1 cache is always volatile, while other cache levels can be both, volatile or non-volatile
- [x] Access speed ✔

Your answer is correct.

The correct answers are: Storage capacity, Access speed, Physical implementation: some caches (e.g. L1) is embedded into the CPU chip, while other caches might be implemented as physically separate chips

Question 11

Incorrect

Mark 0.00 out of 1.50

Do you agree with the following statement regarding MIPS processor instructions?

All MIPS instructions are classified into 3 categories - R, I, and J - depending on a total instruction length in its corresponding binary representation.

Complexity: average

Time to spend: 1 min

Select one:

- True ✖
- False

The correct answer is 'False'.

Question 12

Partially correct

Mark 1.13 out of 1.50

Choose aspects, which affect directly the execution time of a single-threaded computer program. Assume that such a program executes in isolation, cannot be interrupted by any other program, and cannot be parallelised over multiple CPU cores.

Complexity: average

Time to spend: 1.5 mins

Select one or more:

- [ ] The number of CPU cores available
- [x] Communication bus protocols used to transfer data between memory levels ✔
- [x] The access speed of the main system memory ✔
- [ ] No choice is correct
- [ ] The CPU clock frequency
- [x] The storage capacity of CPU caches ✔

Your answer is partially correct.

You have correctly selected 3.
The correct answers are: The access speed of the main system memory, The CPU clock frequency, Communication bus protocols used to transfer data between memory levels, The storage capacity of CPU caches

Question 13

Correct

Mark 2.00 out of 2.00

Recall two major types of computer memory, which are SRAM and DRAM. Match each of the memory units below to its type.

Complexity: average

Time to spend: 1 min

CPU registers	SRAM ✔
Main system memory	DRAM ✔
CPU L2 cache	SRAM ✔
Hard Disk Drive (HDD)	Neither SRAM, nor DRAM ✔
CPU L1 cache	SRAM ✔

Your answer is correct.

The correct answer is: CPU registers → SRAM, Main system memory → DRAM, CPU L2 cache → SRAM, Hard Disk Drive (HDD) → Neither SRAM, nor DRAM, CPU L1 cache → SRAM

Question 14

Incorrect

Mark 0.00 out of 1.50

Do you agree with the following statement?

In order to overcome a "memory wall problem" for modern computer platforms, nowadays serial communication buses became obsolete, and are actively replaced by parallel communication buses.

Complexity: average

Time to spend: 1 min

Select one:

- True ✖
- False

The correct answer is 'False'.

Question **15**

Incorrect

Mark 0.00 out of 1.00

Do you agree that a CPU instruction for memory access (such as lw or sw for MIPS) might execute for more than one CPU clock cycle?

Complexity: average

Time to spend: 1 min

Select one:

- No, incorrect, as the length of a CPU clock period is computed by considering the execution time of the slowest CPU instruction ✖
- Yes, correct

Your answer is incorrect.

The correct answer is: Yes, correct

Question **16**

Incorrect

Mark 0.00 out of 2.50

Consider three processors, denoted by P1, P2, and P3. For each processor, below we list its respective clock rate (frequency) and the average number of clock cycles per instruction (CPI):

P1: 4.2 GHz and 1.5 CPI;

P2: 2.5 GHz and 1.1 CPI;

P3: 4.8 GHz and 2.4 CPI

Which processor executes a larger number of instructions per second, in an average case?

Complexity: average

Time to spend: 2.5 min

Select one:

- P1
- P2 ✖
- P3
- Both, P1 and P2

Your answer is incorrect.

The correct answer is: P1

Question 17

Not answered

Marked out of 1.50

Do you agree that modern general-purpose CPUs have at most two cache levels, which are typically denoted by L1 and L2?

Complexity: average

Time to spend: 1 min

Select one:

- True
- False

The correct answer is 'False'.

Question 18

Incorrect

Mark 0.00 out of 1.00

Choose valid differences between an S/R latch and a D flip-flop.

Complexity: average

Time to spend: 1 min

Select one or more:

- Consumed power for data storage
- No choice is correct ✖
- Storage capacity: different numbers of bits stored
- Synchronicity: an S/R latch is synchronous, while a D flip-flop is asynchronous

Your answer is incorrect.

The correct answer is: Consumed power for data storage

Question **19**

Correct

Mark 1.50 out of 1.50

For each memory unit, which is listed below, specify, either it is volatile, or not.

Complexity: simpler

Time to spend: 1 min

An external USB flash drive	Non-volatile ✔
Solid-state drive	Non-volatile ✔
CPU L2 cache	Volatile ✔
Hard disk drive	Non-volatile ✔
CPU register	Volatile ✔
CPU L1 cache	Volatile ✔
Main system memory (RAM)	Volatile ✔

Your answer is correct.

The correct answer is: An external USB flash drive → Non-volatile, Solid-state drive → Non-volatile, CPU L2 cache → Volatile, Hard disk drive → Non-volatile, CPU register → Volatile, CPU L1 cache → Volatile, Main system memory (RAM) → Volatile

Question **20**

Correct

Mark 1.00 out of 1.00

Recall three major components of a typical CPU: control unit (CU), arithmetic-logic unit (ALU), and registers. Match the functionalities listed below to the corresponding CPU component.

Complexity: simpler

Time to spend: 0.5 min

The execution of arithmetic and logic operations	ALU ✔
Storage of input arguments for an instruction to be executed	registers ✔
Fetching of instructions to be executed in the following CPU cycles	CU ✔

Your answer is correct.

The correct answer is: The execution of arithmetic and logic operations → ALU, Storage of input arguments for an instruction to be executed → registers, Fetching of instructions to be executed in the following CPU cycles → CU

Question **21**

Correct

Mark 1.50 out of 1.50

Do you agree that SRAM memory units are always volatile, while DRAM - non-volatile?

Complexity: average

Time to spend: 1 min

Select one:

- True
- False ✔

The correct answer is 'False'.

Question **22**

Correct

Mark 1.50 out of 1.50

Consider a computer program running on a single processor. Let us now parallelise the execution of that program upon several processors; all processors are assumed to have the same speed. Do you agree that a program execution time, in some cases, can actually increase, rather than decreasing?

Complexity: average

Time to spend: 1 min

Select one:

- True ✔
- False

The correct answer is 'True'.

Question 23

Correct

Mark 1.00 out of 1.00

Do you agree that any assembler program is processor-specific, meaning that an assembler program written, for example, for an Intel x86 processor might not be able to run on an ARM processor?

Complexity: simpler

Time to spend: 1 min

Select one:

- True ✔
- False

The correct answer is 'True'.

Question 24

Correct

Mark 1.50 out of 1.50

Consider the following binary number represented by using two's complement binary notation:

11111001

Convert this number into decimal format.

Complexity: average

Time to spend: 1.5 min

Answer: -7 ✔

The correct answer is: -7

Question 25

Incorrect

Mark 0.00 out of 2.00

What is the most relevant effect of a "heat dissipation problem" on the design of modern computer platforms among the ones listed below?

Complexity: average

Time to spend: 2 mins

Select one:

- There is a strong trade-off between CPU cache speed and its storage capacity: a larger cache has a lower storage capacity and vice versa
- No choice is correct ✖
- There are some technological obstacles for Moore's law to remain valid
- Due to physical limitations, it is no longer possible to keep increasing the memory access speed for main memory chipsets at the same pace as before

Your answer is incorrect.

The correct answer is: There are some technological obstacles for Moore's law to remain valid

Question 26

Incorrect

Mark 0.00 out of 2.00

Recall the key differences between general-purpose processors and FPGA integrated circuits. Choose valid statements below.

Complexity: average

Time to spend: 1.5 mins

Select one or more:

- FPGA is multiple orders of magnitude faster as compared to general-purpose processors ✖
- FPGA functionality cannot be changed after it is manufactured, as opposed to a general-purpose processor ✖
- FPGA uses SRAM registers, while general-purpose processors use both, SRAM and DRAM registers ✖
- No choice is correct

Your answer is incorrect.

The correct answer is: No choice is correct

Question **27**

Partially correct

Mark 0.67 out of 1.00

One of the fundamental ideas behind modern computer platforms is a pipelined execution of CPU instructions. What is the primary motivation for such a pipelined execution?

Complexity: average

Time to spend: 1 min

Select one or more:

- a. No choice is correct
- b. The optimisation of a CPU power consumption ✖
- c. Increased reliability for floating-point operations
- d. Runtime optimisation ✔
- e. The optimisation of communication bus overheads

Your answer is partially correct.

You have selected too many options.
The correct answer is: Runtime optimisation