Github repository info and details about how you created that the repository and added the files.

Madi first created the repository as she had all the Vivado files on her personal PC. She added everyone to the group so we had access to the screenshots and v/sv/IP files needed.

I then followed instructions at https://stackoverflow.com/questions/6613166/how-to-duplicate-a-git-repository-without-forking to duplicate the repo separately so I can make personal changes without affecting Madi's original repo. I then downloaded git on my CAE machine and cloned the repo to my PC as normal.

It should also have your simulation log and a snapshot of the waveform from Vivado. In addition, discuss briefly the reason behind the differences in resource utilization between the resource usage reports from Synthesis and Implementation. (This can be extracted from the project directory or Vivado).

Synthesis just makes the relevant gates but doesn't worry about routing on the FPGA, configuring a CLB (it can use the exact gates, saving area), and physical placement. Once those are considered in Implementation, the resource utilization will go up, namely because the CLB will take up more space than an exact representation due to it having unnecessary material to implement any logic design compared to only having the gates needed.

What if you need to design a large memory? Can you think of a different way to design the memory to reduce the number of FFs used? (Hint: Look closer at the other resources available in the PL)

The PL has access to various types of RAM which I could use to store some of the data rather than making my own ROM to store it. Using this, I can reduce the number of flops used.