
# Secure Sequence Recognizer

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# 1 Introduction

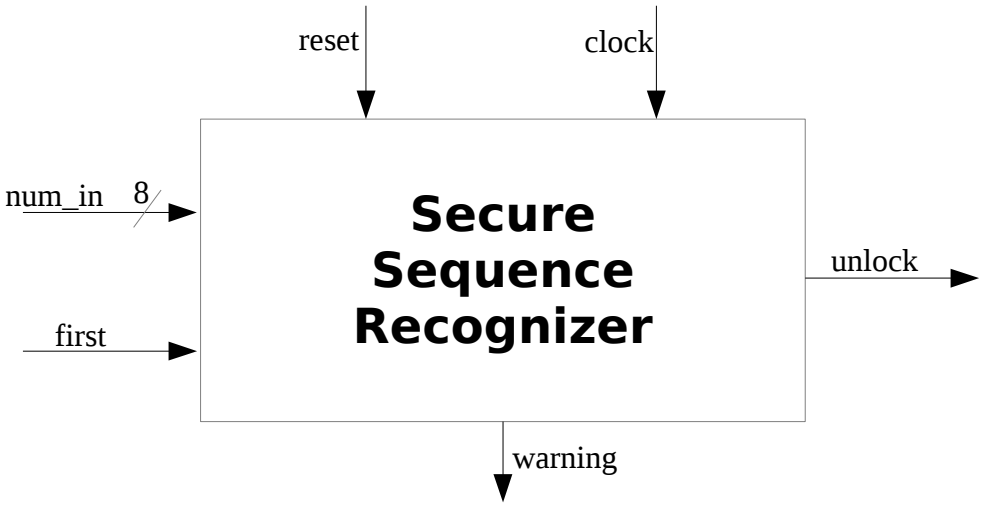
The device implemented is a synchronous sequence recognizer, the sequence numbers are five 8-bit integers. At the beginning of the process the signal must be set to '1' for one clock cycle and the following must be send to the SSR at the rate of 1 clock cycle.

The “first” pin must be kept high for no more than 1 clock cycle otherwise the SSR stops working until a future reset.

The sampling duration is always five clock cycles long and at the end the pin “unlock” is kept high for one clock cycle if the sequence has been inserted correctly.

Instead,if there is at least a wrong number in the sequence the pin “warning” goes to '1' for a clock cycle.

If  it is being inserted a wrong sequence more than three times consecutively the SSR stops working and “warning” goes to '1' permanently or at least until the input pin “reset” goes to '0'




*Picture 1: An I\O view of the device*

## 2 Architecture

The SSR is a finite state machine whose state is described in the STAR register,the latter is a 3-bit register and the possible state are:

1) **SINIT:**the SSR in this state waits for the first sequence number and enter this state whenever the pin “reset” goes to '1'
2) **S0,S1,S2,S3,S4:**In each of those states the SSR samples the input sequences and checks for their correctness
3) **S5:**In this state the “unlock” pin is set to '1' if there were no input errors otherwise the 'warning' pin goes to '1' for a clock cycle.
4) **SBLOCK**: The SSR enters this state whenever the 'first' pin is kept high too long or in the wrong moment and if the sequence is inserted incorrectly for at least three consecutive times. The device leaves this state only if the 'reset' becomes high.

Some other tools are needed in order to make a correct sampling:

- OK.: 1-bit register that contains 1 if until now the sequences are correct, otherwise 0.
- lut_seq: Lookup table that contains the correct sequence.
- SEQNUMBER: 3-bit counter that drives the input of lut_seq.
- COUNT_WRONG:2-bit counter that counts the number of consecutive wrong inputs.

## *State Diagram*

*Picture 2: SSR State diagram*