Paper Code & Roll No. to be filled in your Answer Book

Roll No. | | | | | | | | | | |

Odd Semester Examination-2016

B.Tech. (Semester-III) EC ~~PCS~~

DIGITAL ELECTRONICS AND DESIGN ASPECTS

[Time : 3 Hours] **[Maximum Marks :100]**

Note : Attempt **all** questions.

1. Attempt **any four** parts of the following : [5x4 =20]

   (a) Determine the base 'b' in each of the following cases:

   (i) $(361)_{10} = (551)_b$

   (ii) $(859)_{10} = (5B7)_b$

   (b) Define Hamming code of error detection. Obtain 7-bit Hamming code for the message signal 1101 by using even parity.

   (c) Using K-Map simplify the following expression:

   $f(A, B, C, D) = \Sigma_m (0, 1, 3, 7, 9, 11, 12)$

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(d) Explain Even and Odd parity methods for the detection of 1-bit binary error.

(e) Convert the following numbers to the base as indicated:

(i) $(101101)_2 = (?)_{10}$

(ii) $(56)_{10} = (?)_8$

(iii) $(A46)_{16} = (?)_2$

(f) Convert the followning expressions to the canonical form:

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(i) $F = AB' + A'C + A$

(ii) $F = (A + B)(B' + C)$

2. Attempt **any four** parts of the following : [5×4=20]

(a) Design a 32:1 Mux by using 8:1 Mux and 4:1 Mux.

(b) Implement the following function by using 8:1 Mux

$f(A, B, C, D) = \Sigma_m (0,1,2,4,7,11,12,13,15)$

(c) Explain the working of 3:8 Decoder.

(d) What are the differences between normal encoder and priority encoder? Design a 4-input priority encoder.

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(e) Design a 4-input combinational circuit that converts binary code to gray code.

(f) What are the drawbacks of a full adder? Explain how a parallel adder removes the drawback of a full adder?

Attempt **any two** parts of the following : [10×2=20]

(a) (i) What is Race-Around condition? Explain the master-slave flip-flop.

(ii) Analyze the circuit shown in fig. 1 to produce Boolean algebraic expression for the circuit outputs.

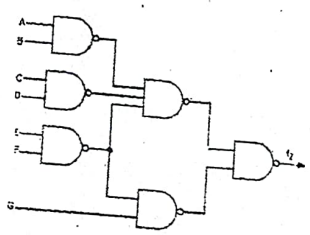

Fig. 1

(b) Explain the basic working of JK Flip-Flop. Design D Flip-Flop using JK Flip-Flop.

(c) Differentiate synchronous and asynchronous sequential circuit. Design a synchronous counter