01/01/15

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PAPER ID :

Paper ID and Roll No. to be filled in your Answer book

Roll. No.

B. Tech.
(SEM –III)
DIGITAL ELECTRONICS AND DESIGN ASPECT

Total Marks: 100 **Time: 3Hours**

Note- All Questions are compulsory

Q. 1. Attempt any four parts: **(4X 5 = 20)**

a) Show that characteristic equation for the complement output of a JK- flip flop is

$$Q'(t+1) = J'Q' + KQ.$$

b) Design the following function using 8×1 Muliplexer.

$F=\Sigma m(1,3,5,6,7,9,11,14,15)$; Select a,b and d as select line.

5 c) Design a negative edge triggered MOD-11 Ripple UP counter using JK flip-flop.

d) Design a BCD Adder. Why we call it decimal adder. Discuss the following cases, when sum is:
   (i) Valid BCD Number
   (ii) Invalid BCD Number
   (iii)Having output carry

e) Design a 4-bit universal shift register using SR flip-flop.

f) A seven- bit Hamming code (Even Parity) as received is 1111101. Check if it is correct. If not, find the correct code.

Q. 2. Attempt any four parts: **(4X 5 = 20)**

a) What is Race around condition and how can we overcome it with the help of J-K Master-Slave flip flop.

b) Design a Full Adder circuit using: (i) 3:8 decoder (ii) 2:4 decoder

c) An 8×1 multiplexer has inputs A, B and C connected to selection inputs S0,S1 and S2 respectively. The data inputs I_0 through are as follows:

$$I_1=I_2=I_7=0;\ I_3=I_5=1;\ I_0=I_4=D;\ I_6=D'$$

d) Implement the following two Boolean function using a PLA:

$F1(A,B,C)= \Sigma m(0,1,2,4)$

$F2(A,B,C)=\Sigma m(0,5,6,7)$.

e) Simplify the 5 variable Boolean functions by using K-map:

$F(A,B,C,D,E) = \Sigma m(0,2,4,6,9,13,21,23,25,29,31)$.

f) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.

Q. 3. Attempt any two parts: **(2x10 = 20)**

a) Determine the minimal expression for the following functionusing Quine-McCluskey method. How will you realize the reduced function by using NAND implementation

$F(ABCD)=\Sigma m(0,1,4,6,8,9,10,12) + d(5,7,14)$.

b) Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.

c) Design a 4 bit synchronous counter using JK flip-flop, which can count only odd numbers.

Q. 4. Attempt any two parts: **(2 X 10 = 20)**

a) A *PN* flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs *P* and *N* are 00, 01, 10, and 11, respectively.

(i) Tabulate the characteristic table.

(ii) Derive the characteristic equation.

(iii) Tabulate the excitation table.

(iv) Show how the *PN* flip-flop can be converted to a *D* flip-flop.

b) Draw a K-Map for the following function of five variables and use it to reduce the function. How will you realize the reduced function by using NOR implementation.

$F=\pi M(0,1,3,7,8,19,21,25,31)*d(2,4,10,15,28)$

c) Draw a TTL circuit with totem pole output and explain its working. Why should it not be used for wired AND connection

(2x 10 = 20)

Q. 5. Attempt any two parts:

a) Design a 4-bit Magnitude Comparator and also implement it with the help of basic gates.

b) What are the different schemes for CMOS to TTL interface? Explain one of them?

c) Reduce the number of states in the following state table and tabulate the reduced state table with drawing its state diagram. Starting from state 'a' of the state table, find the output sequence generated with an input sequence 01101110001010111. And also show that the same output sequence is obtained for reduced state table.

Present State	Next State		output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0