a) The memory hierarchy is significant because it allows for efficient data access and storage by utilizing different types of memory with varying speeds, capacities, and costs. This hierarchy includes registers, cache memory, main memory (RAM), and secondary storage (such as hard drives or SSDs).

b) Source HLL
Object is LLL

QUESTION ONE (COMPULSORY) [30 MARKS]

a) Highlight the significance of memory hierarchy. (3 marks)

b) Distinguish between source codes and object codes? (2 marks)

c) State the difference between the following categories of instructions:

i) Arithmetic instructions and logical instructions (2 marks)

ii) Machine control instructions and branching instructions (2 marks)

d) For each of the instruction below, state its category and write its hexcode:

i) SUI 5EH (2 marks)

i) SUI SEH Category: Arithmetic instruction
Hexcode: SUI - D6, SEH - Not a standard instruction code

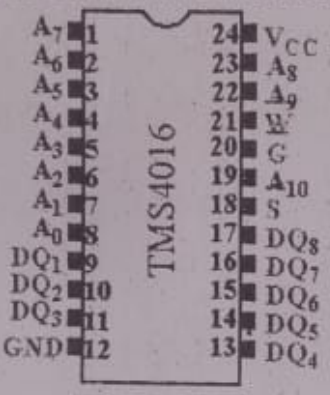
ii) LDAX B (2 marks)

ii) LDAXB Category: Data transfer instruction
Hexcode: 0A

iii) CM 4000H (3 marks)

iii) CM 4000H Category: Control transfer instruction
Hexcode: CD 40 00

e) The figure below shows a memory chip.



Determine:

i) the number of address pins 11 address pins (1 mark)

ii) the memory organization of the IC. (3 marks)

iii) the address range of the chip 2^11 = 2048 (2 marks)

f) Write an ALP to subtract contents of memory 2010h from 2011h (5 marks)

```
MOV AX, [2011H]   ; Move the content of memory location 2011H to register AX
SUB AX, [2010H]   ; Subtract the content of memory location 2010H from AX
```

i) arithmetic-mathematical operation
addition,subtraction,multiplication,division
Logical-logical operation AND OR XOR NOR

ii)Machine control- control flow of execution
loading, storing and moving.
Branching - changing direction of execution eg jump, subroutine calls.

ii)The memory organization refers to how the memory is arranged and accessed. This can include details such as the size of each memory location, the number of memory locations, and the data width. Without specific information about the memory chip in the figure, it is not possible to determine its exact memory organization.

QUESTION TWO [20 MARKS]

a) Highlight the functions of the following pins of 8085uP

i) Reset out being reset (2 marks)

ii) INTR interrupt request: general purpose interrupt (2 marks)

iii) READY signal used to delay microprocessor read/ write till peripheral is ready to send or receive data (2 marks)

iv) $\overline{INTA}$ interrupt acknowledge (2 marks)

b) Dissemble each machine instruction below and state its task:

i) C6H 45H This instruction moves the immediate data (45H) into the memory location specified by the address. (2 marks)

ii) 21H, 00H, FFH Disassembled instruction: MOV AX, 00FFH (2 marks)

iii) 0AH Disassembled instruction: PUSH AX (2 marks)

c) Distinguish between an instruction format and instruction set (4 marks)

instruction format refers to the layout and structure of an individual machine language instruction, including the arrangement of fields for operation code, source and destination register. instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute.

QUESTION THREE [20 MARKS]

a) Show the contents of the accumulator and the status of the flag bits after each of the following operations:

i) 37H+46H (4 marks)

ii) 50H + 50H – A0H (3 marks)

iii) 78H-A9H (3 marks)

b) [illegible]semble program to multiply a value 12H by 8 and provide output through port 80H (10 marks)

QUESTION FOUR [20 MARKS]

a) Describe the stages of executing a POP D instruction in the microprocessor. (4 marks)

- Fetch: The microprocessor fetches the POP D instruction from memory.
- Decode: The microprocessor decodes the POP D instruction to identify that it is a pop operation and determines the destination register (D) where the data will be popped from the stack.
- Memory Access: The microprocessor accesses the memory location pointed to by the stack pointer to retrieve the data to be popped. The stack pointer is decremented to point to the next location on the stack.
- Write: The data retrieved from the stack is written into the destination register (D).

b) Below is a delay program.

```
        LXI B, 3400H
DELAY:  DCX B
        MOV A, C
        ORA B
        JNZ DELAY
        HLT
```

i) Given a clock frequency of 3MHz, calculate the duration of the delay program (7 marks)

ii) Write the algorithm of a delay program (5 marks)

iii) Convert the assembly language of the delay program into hand code. (4 marks)

QUESTION FIVE [20 MARKS]

a) Draw a flowchart to illustrate a program that:

i. Reads a memory address 4200H
ii. set COUNTER to be equal to the read input
iii. decrements COUNTER to zero
iv. reads the next memory address and repeats steps (ii) to (iv) (8 marks)

b) Write a ALP program for part (a) above. (12 marks)

Start
|
|__ Read memory address 4200H
| |
| |__ Set COUNTER = input
| |
| |__ Decrement COUNTER
| |
| |__ Read next memory address
| |
| |__ Repeat steps (ii) to (iv) until COUNTER = 0
|
End

```
ORG 0000H

START: MOV A, 4200H ; Read memory address 4200H
       MOV COUNTER, A ; Set COUNTER = input

LOOP:  DJNZ COUNTER, READ_NEXT ; Decrement COUNTER and jump if not zero
       HLT ; End program

READ_NEXT: INC 4200H ; Read next memory address
       JMP LOOP ; Jump back to LOOP
```

INSTRUCTION SET OF 8085

HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	
00	NOP	25	DCR H	4A	MOV C, D	6F	MOV L, A	94	SUB H	B9	CMP C	DE	SBI D
01	LXI B, D16	26	MVI H, D8	4B	MOV C, E	70	MOV M, B	95	SUB L	BA	CMP D	DF	RST 3
02	STAX B	27	DAA	4C	MOV C, H	71	MOV M, C	96	SUB M	BB	CMP E	E0	RPO
03	INX B	28	-	4D	MOV C, A	72	MOV M, D	97	SUB A	BC	CMP H	E1	POP H
04	INR B	29	DAD H	4E	MOV C, M	73	MOV M, E	98	SBB B	BD	CMP L	E2	JPO A
05	DCR B	2A	LHLD Adr	4F	MOV C, A	74	MOV M, H	99	SBB C	BE	CMP M	E3	XTHL
06	MVI B, D8	2B	DCX H	50	MOV D, B	75	MOV M, L	9A	SBB D	BF	CMP A	E4	CPO
07	RLC	2C	INR L	51	MOV D, C	76	HLT	9B	SBB E	C0	RNZ	E5	PUSH
08	-	2D	DCR L	52	MOV D, D	77	MOV M, A	9C	SBB H	C1	POP B	E6	ANI D
09	DAD B	2E	MVI L, D8	53	MOV D, E	78	MOV A, B	9D	SBB L	C2	JNZ Adr	E7	RST 4
0A	LDAX B	2F	CMA	54	MOV D, H	79	MOV A, C	9E	SBB M	C3	JMP Adr	E8	RPE
0B	DCX B	30	SIM	55	MOV D, L	7A	MOV A, D	9F	SBB A	C4	CNZ Adr	E9	PCHL
0C	INR C	31	LXI SP, D16	56	MOV D, M	7B	MOV A, E	A0	ANA B	C5	PUSH B	EA	JPE A
0D	DCR C	32	STA Adr	57	MOV D, A	7C	MOV A, H	A1	ANA C	C6	ADI D8	EB	XCHG
0E	MVI C, D8	33	INX SP	58	MOV E, B	7D	MOV A, L	A2	ANA D	C7	RST 0	EC	CPE A
0F	RRC	34	INR M	59	MOV E, C	7E	MOV A, M	A3	ANA E	C8	RZ	ED	-
10	-	35	DCR M	5A	MOV E, D	7F	MOV A, A	A4	ANA H	C9	RET Adr	EE	ERI D
11	LXI D, D8	36	MVI M, D8	5B	MOV E, E	80	ADD B	A5	ANA L	CA	JZ	EF	RST 5
12	STAX D	37	STC	5C	MOV E, H	81	ADD C	A6	ANA M	CB	-	F0	RP
13	INX D	38	-	5D	MOV E, L	82	ADD D	A7	ANA A	CC	CZ Adr	F1	POP P
14	INR D	39	DAD SP	5E	MOV E, M	83	ADD E	A8	XRA B	CD	CALL Adr	F2	JP Ad
15	DCR D	3A	LDA Adr	5F	MOV E, A	84	ADD H	A9	XRA C	CE	ACI D8	F3	DI
16	MVI D, D8	3B	DCX SP	60	MOV H, B	85	ADD L	AA	XRA D	CF	RST 1	F4	CP A
17	RAL	3C	INR A	61	MOV H, C	86	ADD M	AB	XRA E	D0	RNC	F5	PUSH