CSC 211: DIGITAL ELECTRONICS II

- **Timing Circuits**

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Lesson Objectives

- At the end of this topic you should be able to:
  - recall that a monostable circuit has one stable state and one unstable state;
  - describe how an inverter can be used with a RC network as a simple time delay circuit;
  - draw the circuit diagram for a monostable using a 555 timer IC;
  - calculate the time period for a 555 monostable circuit using the formula:

    $T = 1.1\ RC$;
  - design a 555 monostable to meet a given specification.

Introduction

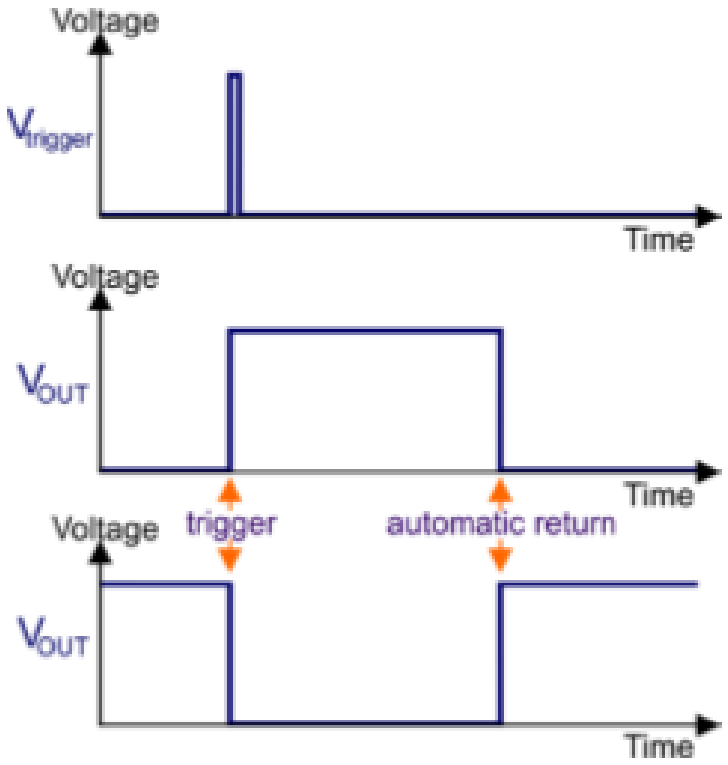
there's bistabl(in both states) e and astabl(not stable in either statese too

- Monostable circuits are useful for creating delay sub-systems of configurable length.
- For example, these can be used:
  - to keep an outside lamp on for twenty seconds when triggered by a movement sensor;
  - to set the heating time for an automatic egg boiler.

Ideal Monostable Behaviour

- A monostable circuit has one stable state, either logic 0 or logic 1.
- It remains in that state until triggered into the opposite logic state by an external signal.
- After a predetermined time, the output returns to the original stable state.
- This behaviour is shown in the voltage / time graphs for initially low or high situations.

Ideal Monostable Behaviour

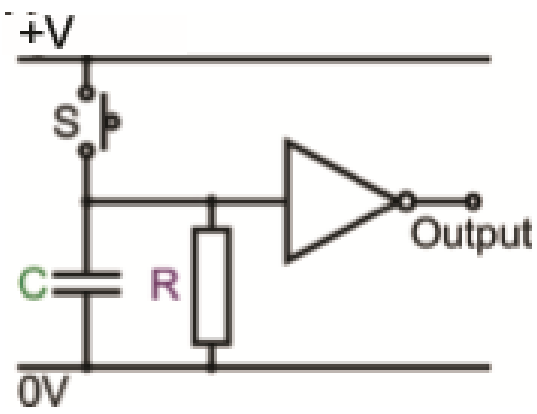


Buffering the RC network

- The basic building block of any monostable timer is the RC network.
- Where an output current flows, the timing is disturbed and the delay depends on the size of the current, which is not a desirable feature.
- The solution is to ‘buffer’ the output of the RC network with a component such as a NOT gate.
- The output current then comes from the power supply to the NOT gate and not from the RC network itself.
- The RC network controls only when the NOT gate switches.

Buffering the RC network

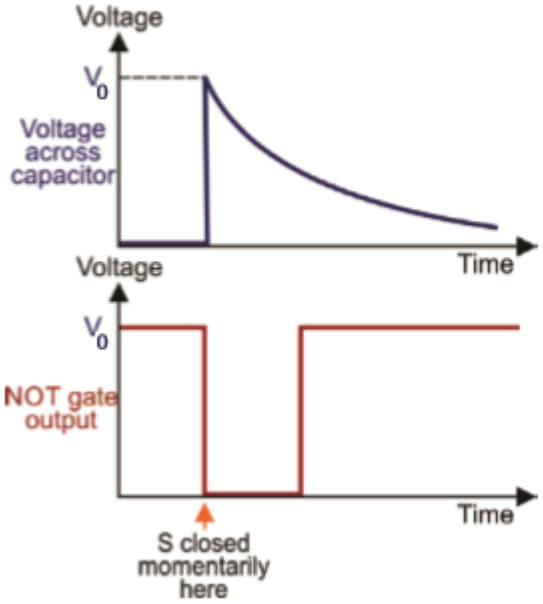
- The circuit opposite shows a RC discharge circuit buffered by a NOT gate.
- When switch S is momentarily closed, the capacitor charges to the supply voltage V_S, raising the NOT gate input to logic 1.



- As a result, the output of the NOT gate switches to logic 0.
- Once the switch is released, the capacitor begins to discharge and the voltage across it falls.
- Assuming that the NOT gate output changes when its input reaches ½ V0, this happens after 0.69 RC seconds.

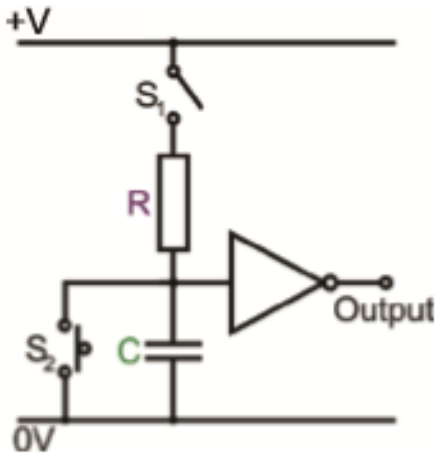
Buffering the RC network

- The output of the NOT gate stays low for 0.69 RC seconds and then returns to its stable high state until triggered again by pressing switch S.
- This behaviour is illustrated in the graphs opposite.
- Changing the resistor (or capacitor) value changes the delay (the time for which the NOT gate output sits at logic 0).



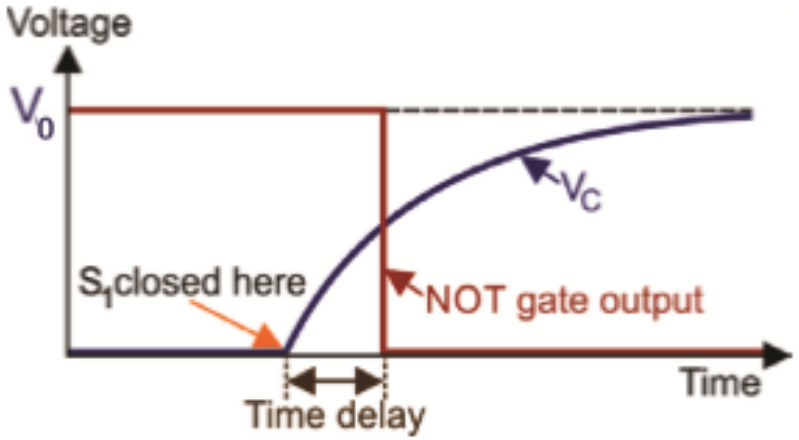
Buffering the RC network

- Now, consider the equivalent using the RC charging circuit.
- Initially, switch S_2 is pressed to discharge the capacitor, making the NOT gate input sit at logic 0 and its output at logic 1.
- When switch S_1 is closed, the capacitor charges up.
- As a result, the voltage at the input of the NOT gate rises and eventually reaches the logic 1 threshold.
- At this point, the output of the NOT gate switches to logic 0



Buffering the RC network

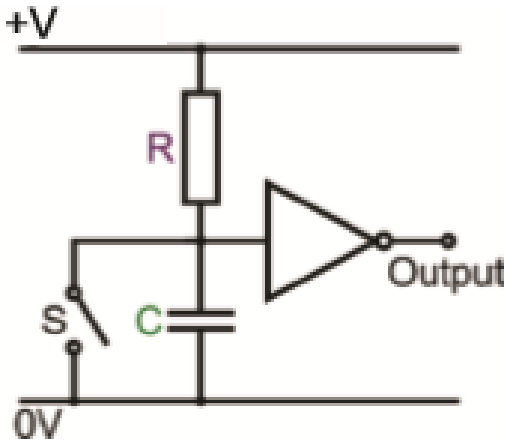
- This behaviour is shown in the graph below.



- There are practical issues with this circuit.
- It requires two switches, S_1, which has to be left closed long enough for the capacitor to charge, and S_2 which has to be momentarily closed before S_1 to initialize the circuit.

Buffering the RC network

- A modified version, using only one switch, is shown opposite.
- Switch S is normally closed. The input to the NOT gate sits at logic 0 and so its output will be logic 1.
- When switch S is opened, the capacitor charges and the voltage at the input of the NOT gate rises.
- When it reaches the logic 1 threshold, the output of the NOT gate switches to logic 0.
- The basic operation is the same.
- One issue is that the NOT gate and RC network remain ‘powered up’ unless the wider system includes a master ‘power’ switch elsewhere.

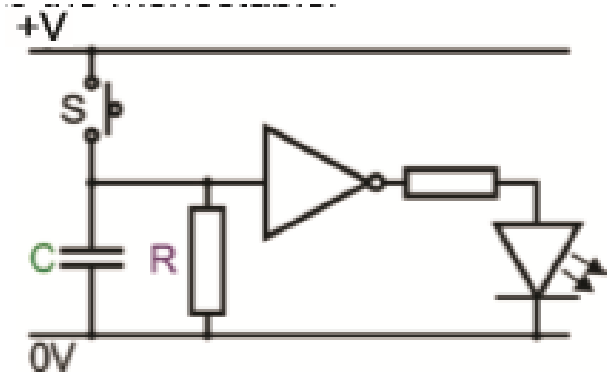


Designing monostable circuits

- Monostables, using a RC network and NOT gate, provide an easy method of creating a delay.
- However, remember that a monostable using the RC charging circuit needs a switch in parallel with the capacitor to discharge it.
- So far we have not specified the required behaviour of the load attached to the monostable.

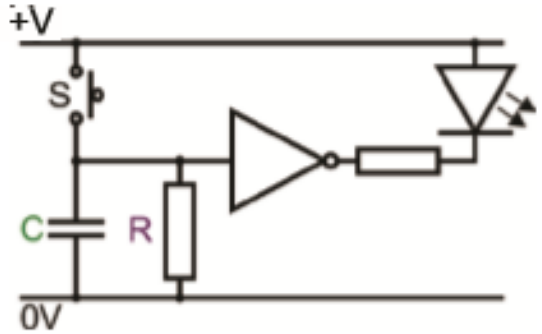
Designing monostable circuits

- In this circuit, the LED lights when the NOT gate output is logic 1 – the NOT gate sources the current.
  - In the stable state, the capacitor is discharged, making the NOT gate input logic 0 and its output logic 1. The LED is lit.
  - When switch S is pressed momentarily, the capacitor charges to V_0, changing the input of the NOT to logic 1 and its output to logic 0. The LED turns off.
  - The capacitor starts to discharge and after a time equal to 0.69 RC, the input of the NOT gate reverts to logic 0. The NOT gate output changes to logic 1 and the LED switches on again.



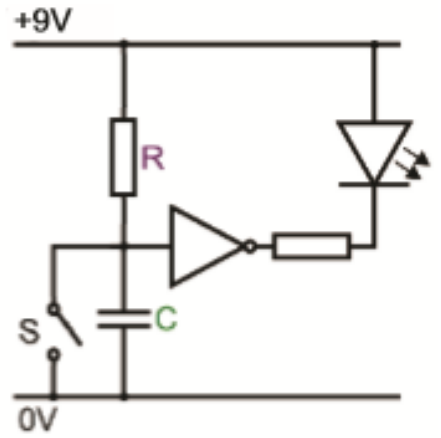
Designing monostable circuits

- In this circuit, the LED lights when the NOT gate output is logic 0 – the NOT gate sinks the current.
- A similar argument shows that the LED is off initially. When S is closed, the LED turns on for time equal to 0.69 RC.
- The CMOS 4049 inverting hex buffer contains six (hence 'hex') NOT gates. It is useful in these applications as the NOT gates switch when the input is approximately half of the supply voltage. It can source about 10 mA, sink over 40 mA and the input current is negligible.



Example 1:

- Design a circuit, using a 9 V power supply, which switches the LED on after a delay of approximately 20 seconds once switch S is opened. The basic circuit is shown opposite.
- Assuming that the output of the NOT gate changes when its input reaches ½ V_0, we select values of R and C which cause the voltage across the capacitor to fall to 4.5 V in 20 seconds.



Example 1:

- In other words, we want a half-life, t, of approximately 20 seconds. Using the formula:

$$t = 0.69.R.C$$

$$20 = 0.69.R.C$$

- so that: $R.C = 20/0.69 = 28.99$

Example 1:

- Start by choosing the capacitor value, as normally the range of capacitor values is more restricted.

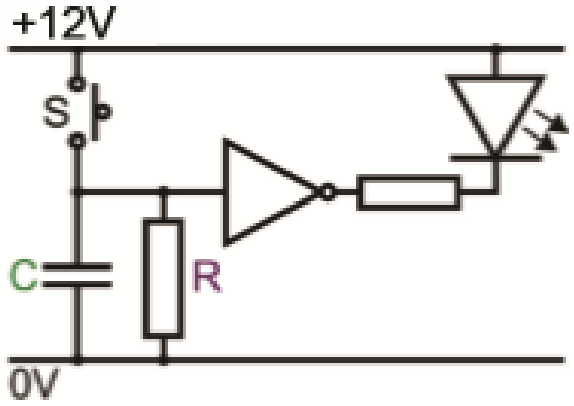
  Try: C = 1000 µF

  Then: R ≐ 29 kΩ

  The nearest preferred value is 30 kΩ.
- Using these values in the circuit diagram allows the monostable to be built and tested.
- Where the delay period is critical, it is normal to use a variable resistor, allowing fine tuning of the time delay.

Example 2

- Design a circuit, using a 12 V power supply, that switches on an LED for approximately 10 seconds after switch S is momentarily pressed and released.
- The basic circuit is shown opposite:
- Assuming that the output of the NOT gate changes when its input voltage reaches ½ V_0, the values of R and C are chosen to give a half-life, t, of around 10 seconds.



Example 2

- Using: $t = 0.69.R.C$

  $10 = 0.69.R.C$

  so that: $R.C = 10/0.69$

  $= 14.5$

Using the same capacitor as before:

$C = 1000\ \mu F$

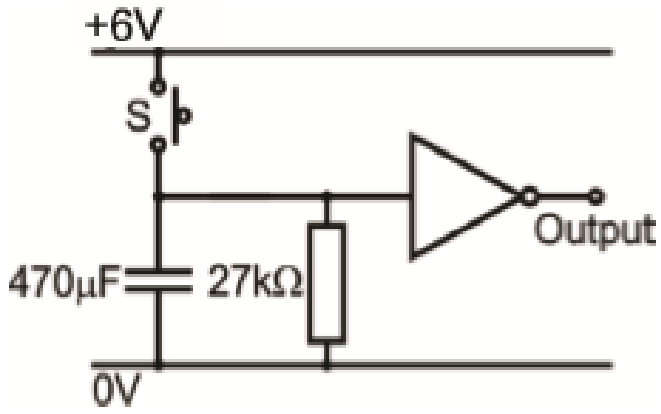
Then: $R = 14.5\ k\Omega$

The nearest preferred value is 15 kΩ.

Using these values in the circuit diagram allows this second monostable to be built and tested.

Example 3

- This time, the circuit for the monostable sub-system is provided.
- The task is to analyse it.
- For the circuit shown, determine the time taken for the output to change after the switch is momentarily closed and then reopened.
- (Assume that the output of the NOT gate changes when its input reaches 3 V.)



Example 3

- Using the assumption given in the question, the output of the NOT gate changes when its input reaches 3 V, which is half of the supply voltage.
- The time taken to do this is the half-life of the monostable.
- Using: $t = 0.69.R.C$

  $= 0.69 \times 27 \times 10^{3} \times 470 \times 10_{-6}$
- so that: $= 8.76$ s

  $\underline{=}$ 9 s
- The delay between the switch being opened and the output changing will be roughly 9 s.

Exercise

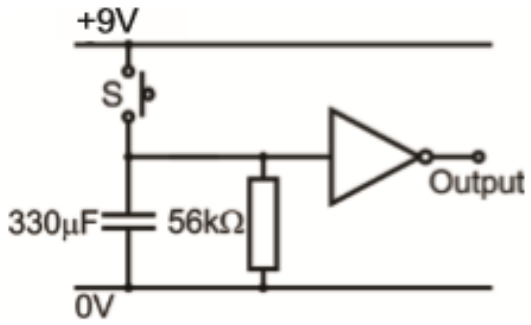
- For all three questions, assume that the NOT gate output changes logic level when the input reaches half of the supply voltage

1. Design a monostable circuit using a RC network and NOT gate that switches on a LED for approximately 45 s after a switch is momentarily closed and released. It operates on a 12 V power supply
2. An alarm system is required to switch on a buzzer exactly 3 minutes after a safe door is opened. The circuit uses a RC network, a NOT gate and a component that allows the time to be adjusted to exactly 3 minutes. It operates on a 6 V power supply.

Draw your design in the space provided and show any calculations used to determine component values.

Exercise

3. For the circuit shown, determine the time taken for the output to change after the switch is momentarily closed and then opened.

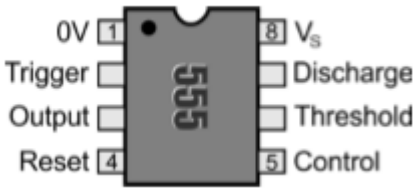


555 timer

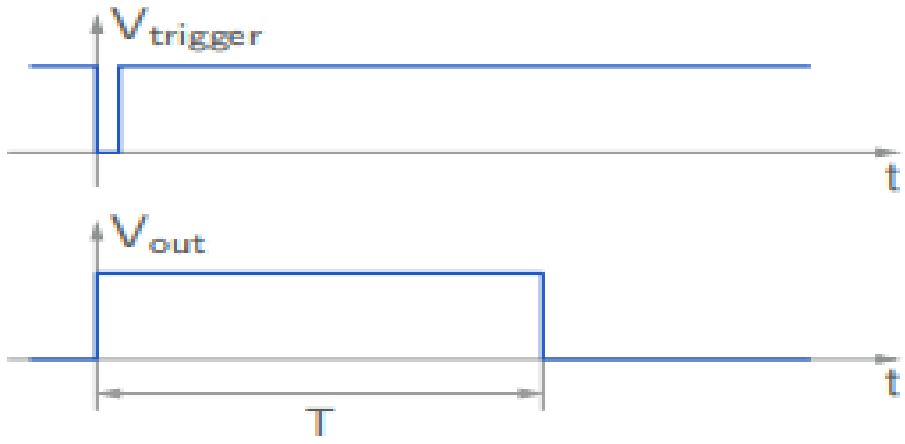
The 555 timer is useful in timer, pulse generation, and oscillator applications. We will look at two common applications.

The 555 timer is one of the most widely used ICs in electronics, at the heart of many astable, and monostable circuits

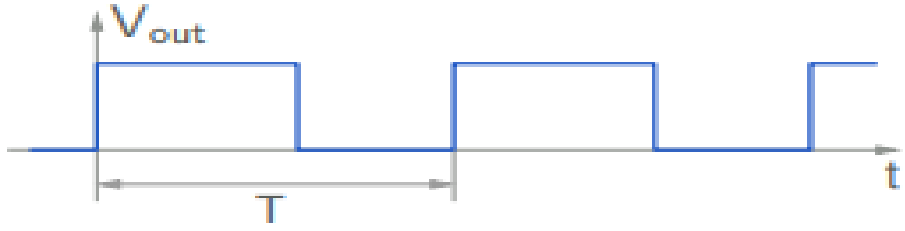
The diagram shows the pinout for the usual format of the 555 timer IC, though you are not required to memorise it or the information that follows. Both will be useful when you use the IC in investigations and project work.



* Monostable multivibrator

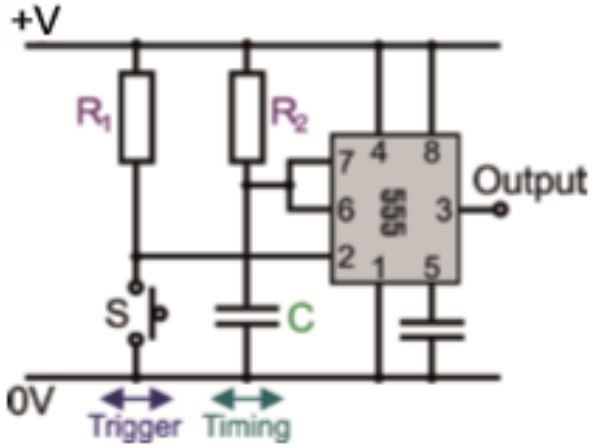


* Astable multivibrator



The 555 Monostable

- Here is the standard circuit diagram for a 555 monostable. The time delay produced by it is given by the formula: T = 1.1RC (This equation is given with the examination paper and so need not be memorised. However, candidates are expected to recall and draw this circuit diagram for a 555 monostable.)



The 555 Monostable

- NB:
- The minimum value of resistance for the timing resistor is 1 kΩ. Limiting the current in this way prevents overheating the component.
- The small capacitor connected to pin 5 is usually 10 nF – the precise value is unimportant for any calculations

Example

- Calculate the time delay produced when the monostable circuit shown opposite is triggered.
- The time delay, T, produced by the monostable timer is:

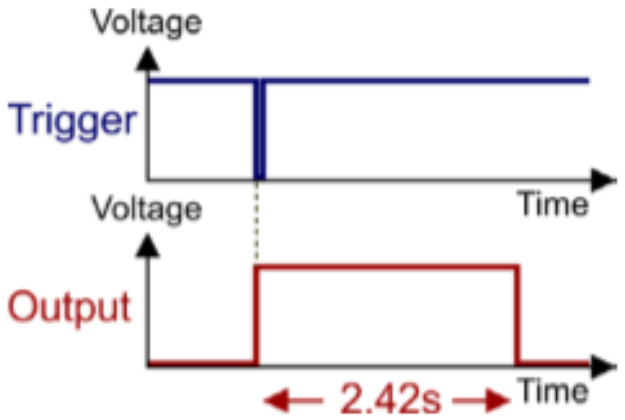
$$T = 1.1\ R\ C.$$

$$= 1.1 \times 22 \times 10^{3} \times 100 \times 10^{-6}$$

$$= 2.42\ s$$

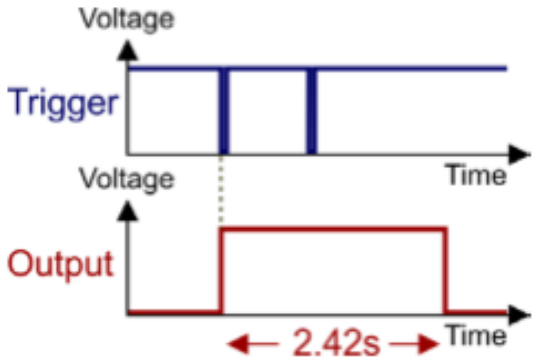
Features

- The following graphs illustrate some features of the behaviour of this monostable circuit:
- When the trigger (pin 2) is pulled low by closing switch S the output goes high and stays there for the calculated period of 2.42 s.



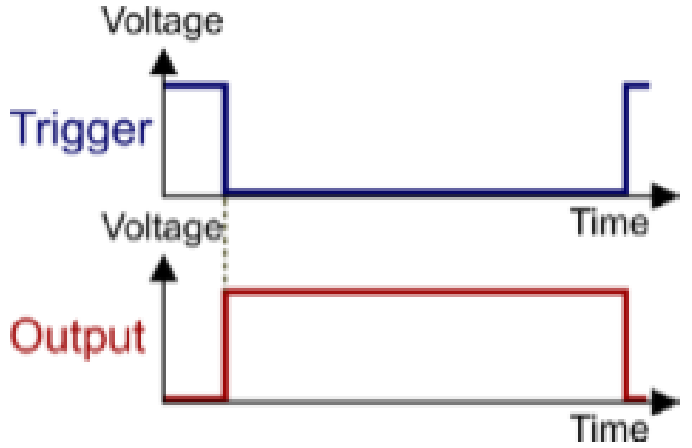
Features

- If a second trigger event occurs before the timing period has ended, this pulse is ignored.



Features

- If the switch is held closed for too long, producing a very long trigger pulse, the output remains high beyond the normal duration.



Astable Circuits

- Learning Objectives:
- At the end of this topic you should be able to:
  - recall that an astable circuit has two unstable states;
  - calculate the mark space ratio for an astable signal.
  - draw the circuit diagram for an astable using a 555 timer IC;
  - select and use the following formulae for a 555 astable circuit:
    - the time the output is high: $t_H = 0.7(R1 + R2).C$
    - the time the output is low: $t_L = 0.7R2C$
    - the pulse frequency: $f = 1.44/(R1 + 2R2).C$
    - mark: space ratio: $T_{ON} / T_{OFF} = (R_1 + R_2)/R_2$
  - design a 555 astable to meet a given specification.

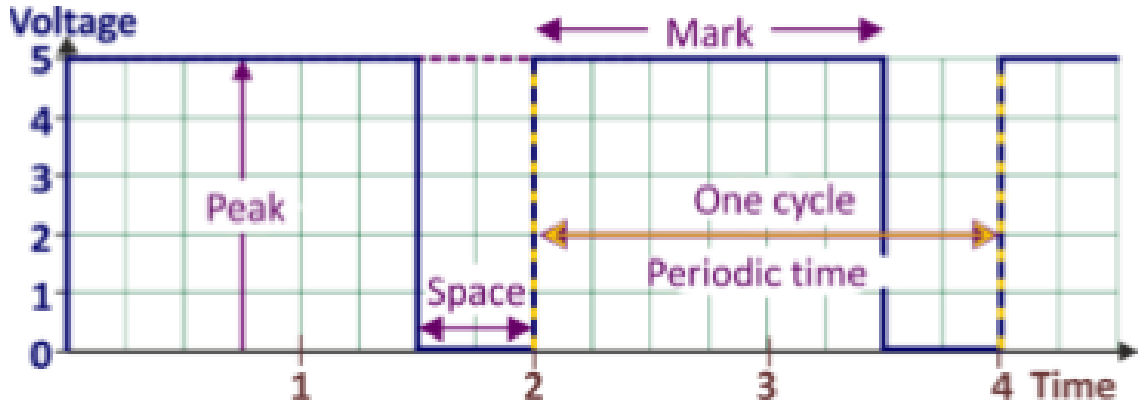
Introduction

- The astable circuit is used in a variety of applications, such as causing flashing lights and pulsing buzzers in alarm circuits and triggering counters.
- Ideal astable behaviour
- The previous section looked at the behaviour of monostable circuits, which had just one stable state.
- In contrast, the astable circuit has no stable states. Its output switches continually between logic 1 and logic 0.
- It is sometimes known as a ‘pulse generator’ or a ‘clock’.

Introduction

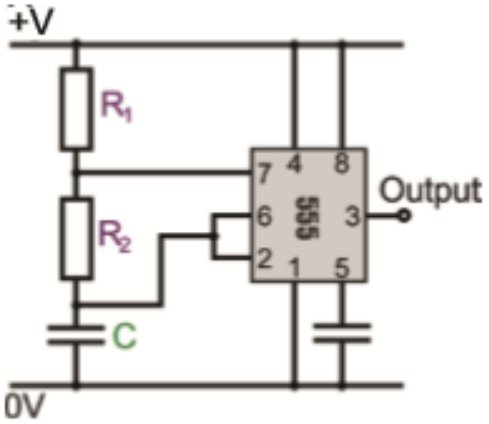
- The parameters of the signal generated by an astable circuit include the ‘mark-space ratio’.
- The ‘mark’ refers to the ‘on’ time (at logic 1), the ‘space’ is simply the ‘off’ time (at logic 0).
- For example, a mark-space ratio of 3:1 means that the ‘on’ time must be three times as long as the ‘off’ time.

- The output of an astable circuit is shown in the timing diagram below. Logic 1 is represented by +5 V and logic 0 by 0 V in this diagram:



- The peak voltage is also known as the amplitude of the signal.
- For this signal:
  - Peak voltage = 5 V
  - Periodic time = 2 s
  - Mark-space ratio = 3:1
- As for all periodic signals, frequency f =1/T, where T is the periodic time (usually referred to as simply the period).
- In this case, then, frequency = 1/2 = 0.5 Hz

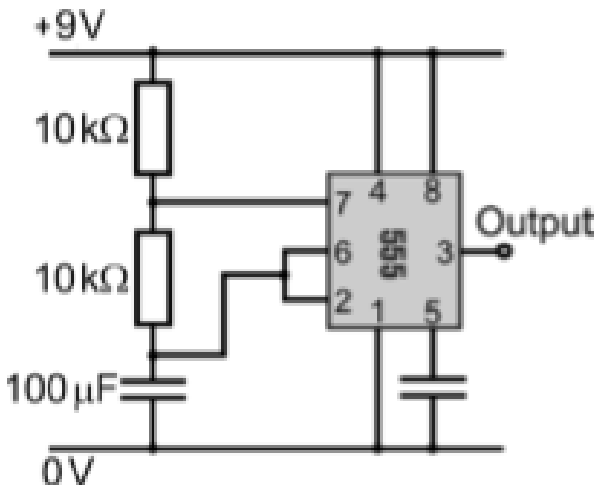
- The circuit diagram for one form of 555 astable circuit is shown below.



- NB:
- The ‘mark’ is always longer than the ‘space’. They are roughly the same if $R_2 >> R_1$.
- The minimum value of resistance for R_1 and R_2 is 1k to prevent overheating.
- Once again, the capacitor on pin 5 is 10nF but the actual value is unimportant.

Example

- For the 555 astable shown opposite, calculate:
  a) the time t_H for which the output is high;
  b) the time t_L for which the output is low;
  c) the mark: space ratio;
  d) the frequency of the pulses produced.



Solution

a) $t_H = 0.7(R1 + R2).C$

$= 0.7(10\times10^3+10\times10^3).100\times10^{-6}$

$= 1.4$ s

The output is high for 1.4 s.

a) $t_L = 0.7R2C = 0.7\times10\times10^3\times100\times10^{-6}$

$= 0.7$ s

- The output is low for 0.7 s.
- (c) These results can be written as:

Mark = 1.4 s Space = 0.7 s.

The mark: space ratio is therefore 2:1.

- Alternatively, $T_{ON} / T_{OFF} = (R_1 + R_2)/R_2$
- Mark: Space = (10kΩ + 10kΩ)/10kΩ = 2:1

Solution

d) $f=1.44/(R_1+R_2)$

$=1.44/(10\times10^3+20\times10^3)*100\times10^{-6} = 0.48$ Hz

- The pulse frequency is 0.48 Hz.
- Alternatively,
- $f =1/(t_H + t_L)$

$= 1/ 2.1 = 0.476$ Hz

Exercise

1. Use the grid below to draw an astable waveform with:
   - peak voltage of 8 V;
   - periodic time of 3 s;
   - mark: space ratio of 2:1.