System Architecture

System Architecture:

- Machine level architecture of a Computer system includes the specification of the
  - system function (external architecture)
  - components and the interconnections.

- From a functional view point, a computer system
  - Accepts data
  - Perform some prescribed processing on the data
  - Output results

System Architecture:

- Concrete (internal) architecture options
  - hardwired

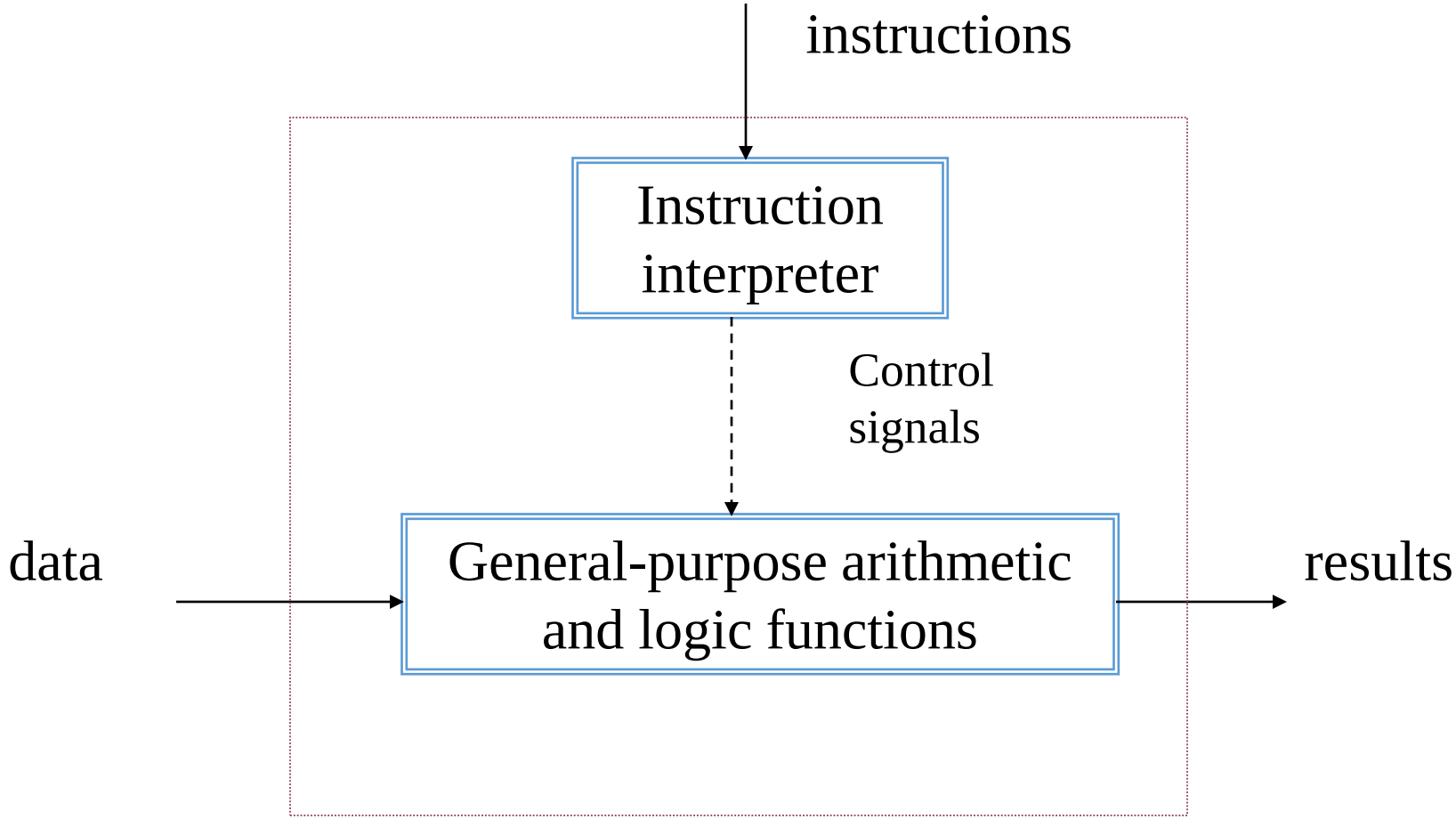
The Concept of a Programmable Machine

- The processing performed on the data is determined by a program
- The machine is provided with an appropriate program in order to perform a specified computation
- the machine can perform a variety of computations
    - programmable machine (softwired)

The Concept of a Programmable Machine

- The hardware is a programmable machine consisting of
  - 1. a general-purpose arithmetic and logic unit able to execute a small set of simple/basic functions selectable by control signals.
  - 2. an instruction interpreter which reads instruction codes one at a time and generates an appropriate sequence of control signals.

The Concept of a Programmable Machine



The Concept of a Programmable Machine

- Any computation can be expressed as a sequence of instructions selected from a small set (i.e. a program).

- The machine executes the instructions, using the provided data, to generate the results.

The Concept of a Programmable Machine

Advantages:

- Software programming is much simpler and more flexible than hardware programming.
- A single machine can be easily programmed to perform a wide variety of computations or processing.
- The machine is more versatile and can quickly be switched between a wide variety of processing functions.
- Since all complex computations can be expressed as a sequence of very simple operations, the hardware required is that much simpler.

Components of the Programmable Machine

- Instruction interpreter + general purpose arithmetic and logic functions

  $\Rightarrow$*CPU*

- An input unit to accept data and instructions in external form and converts to internal form.
- An output unit to accept results in internal form and presents in external form.
- Input Unit + Output unit =

  $\Rightarrow$*I/O Module*

Components of the Programmable Machine

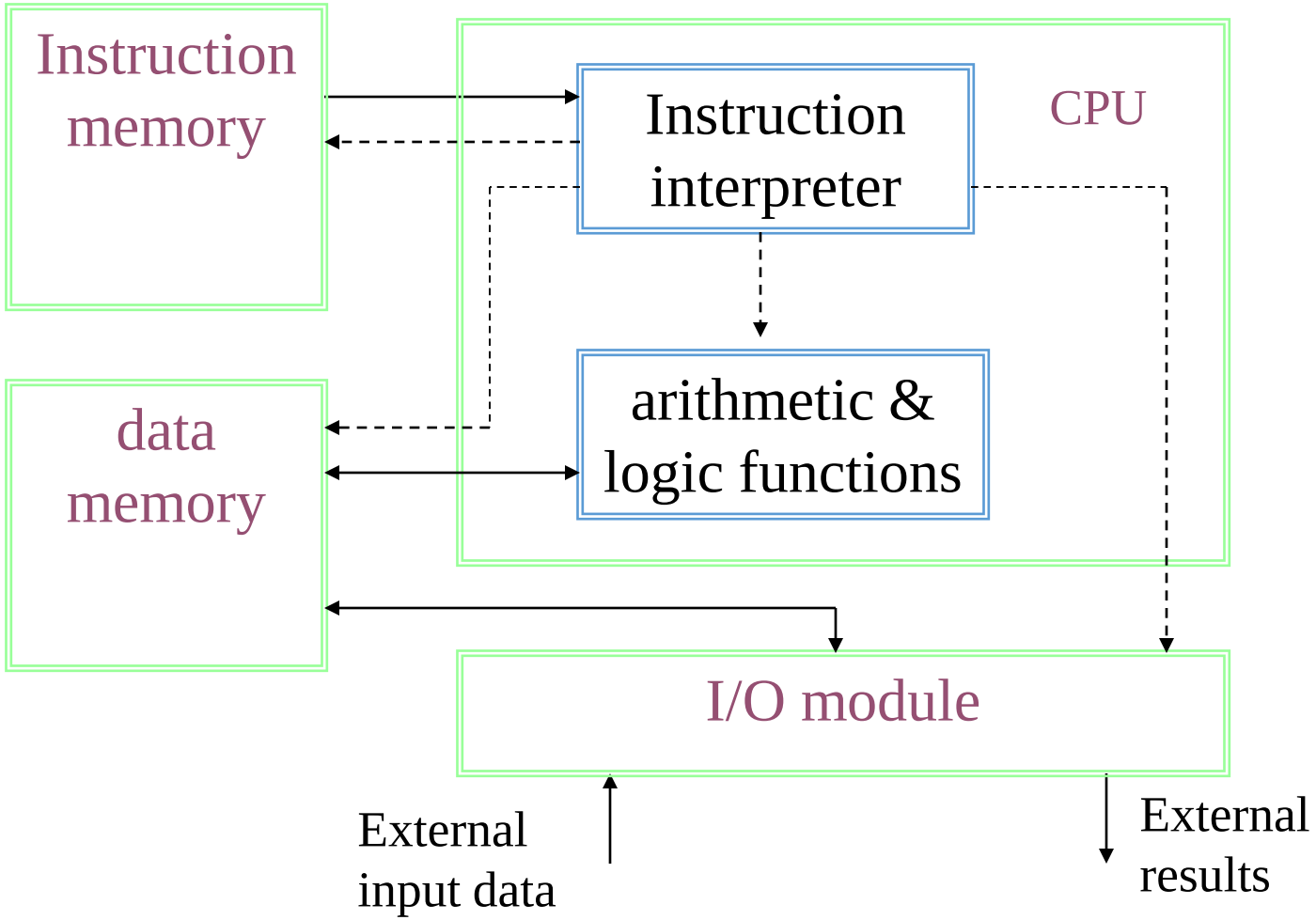
- To support branching and iterative execution within instruction streams we need a random access

  ⇒*Instruction Memory unit*

- To support access to several elements of data at a time we need a random access

  ⇒*Data Memory unit*

System Architecture: Components of the Programmable Machine



CPU ARCHITECTURE

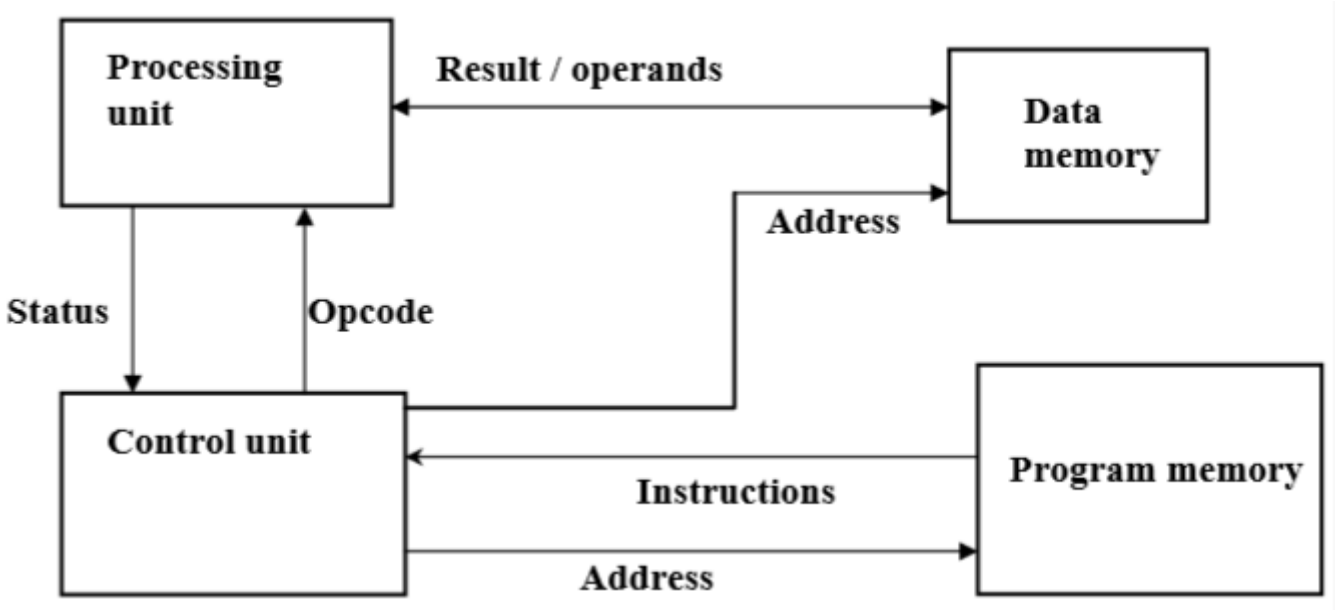
Basically there are two architectures:

- Harvard Architecture
- Von Neumann Architecture
  - also called the Princeton University Architecture

Harvard architecture

- in this memory architecture, there are two distinct memory spaces.
  - Program memory and
  - data memory.

Harvard Architecture



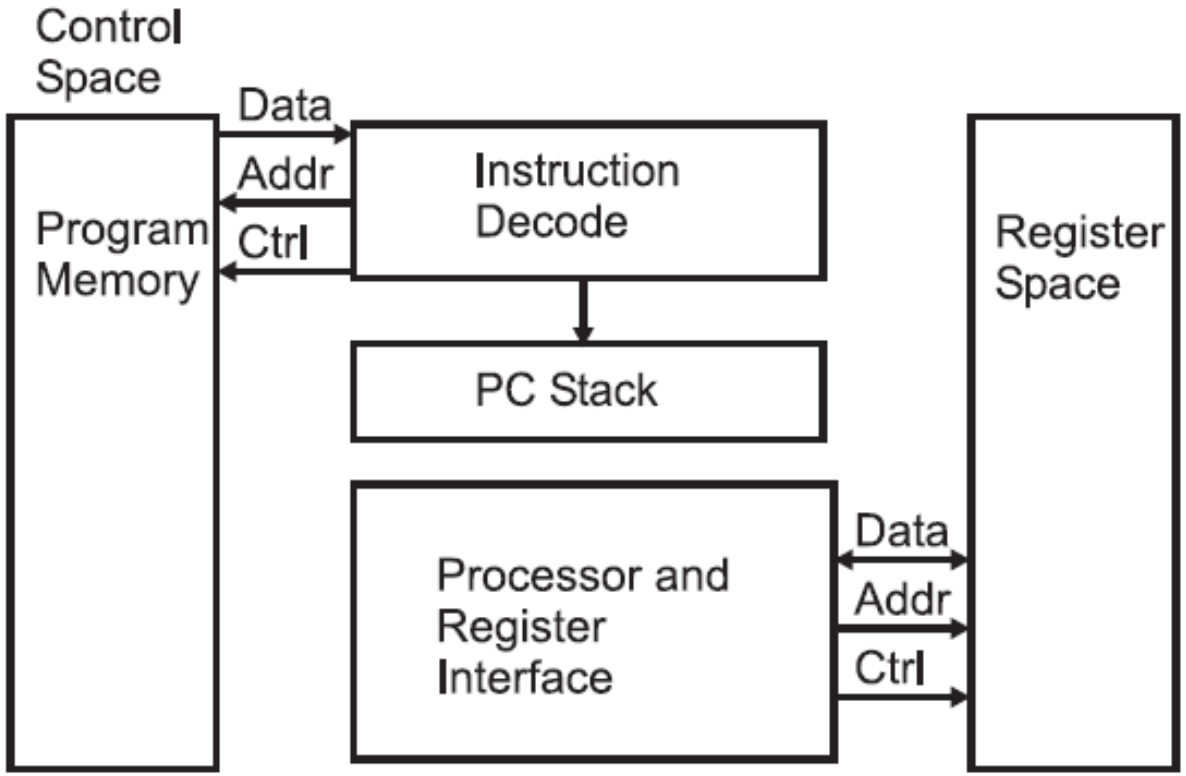
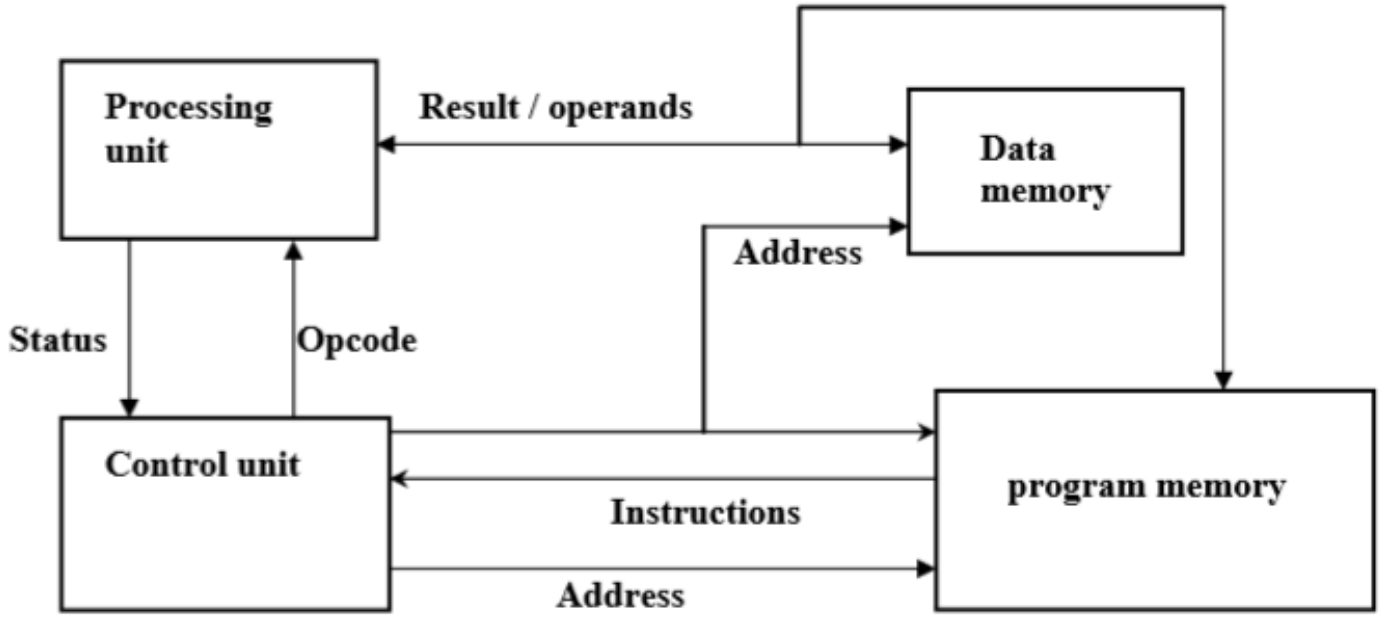


Fig. 12-2. Harvard processor architecture.

Modified Harvard Architecture

- Results and operands can be fed to the program memory



The von Neumann Model

- Is a for all modern computers to use stored program
- Both program and data are stored in a common memory
- The concept was designed by ISA computer team lead by Von Neumann.

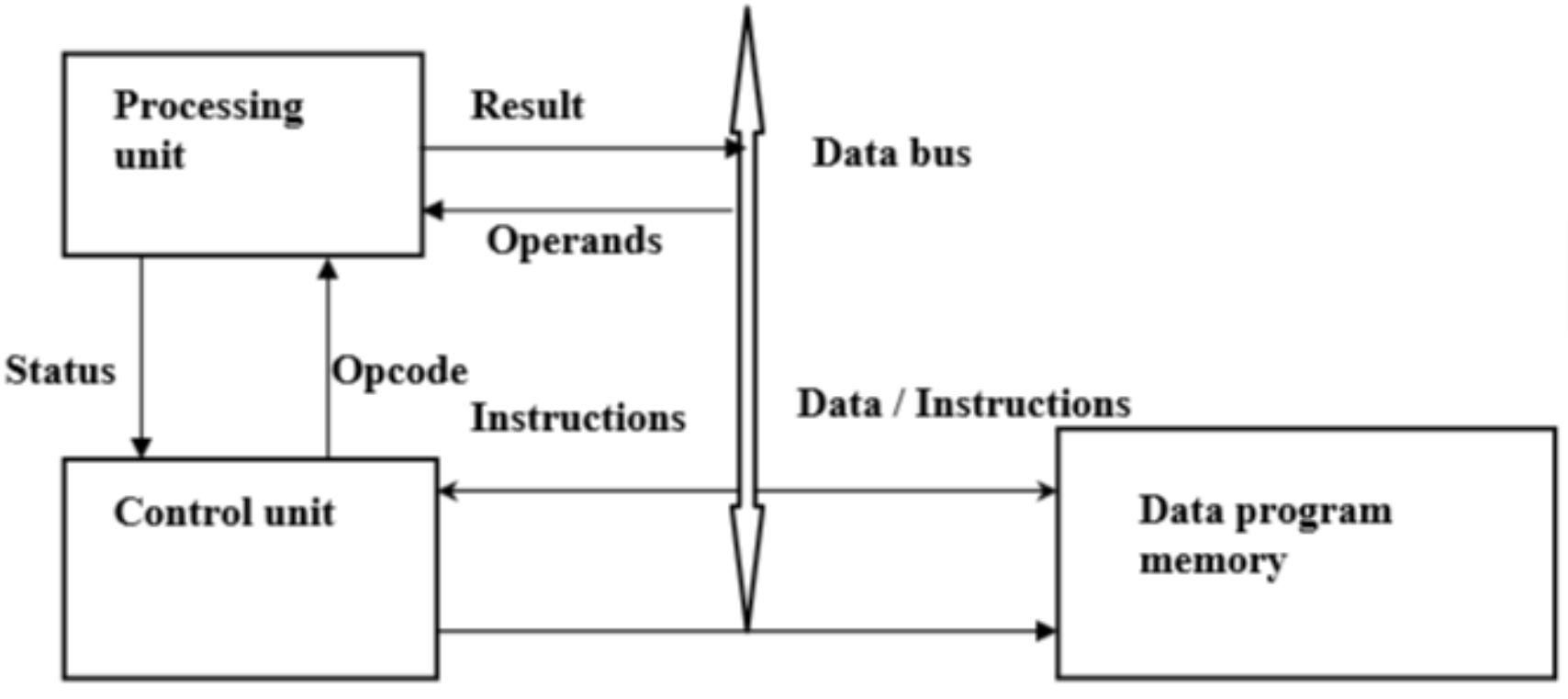
The von Neumann Model

- The essential of stored program concept are as follows:
- i) The computer has five different types of units:
  - Memory,
  - ALU,
  - Control unit,
  - Input/Output unit.
- ii) The program and data are stored in common memory
- iii) Once a program is in memory the Central Processing Unit (CPU) can execute it automatically.
- iv) The control unit fetches and executes the instructions in sequence one by one. Execution occurs in sequential fashion from one instruction to the next unless explicitly modified
- iv) An instruction can modify the content of any location in memory. Hence a program can modify itself; instruction execution sequence can also be modified.

The von Neumann Model

- Several *registers* are required within the CPU to support the basic interactions, namely,
  - MAR – memory address register
  - MBR – memory buffer register
  - MDR – memory/data register

Von Neuman Architecture



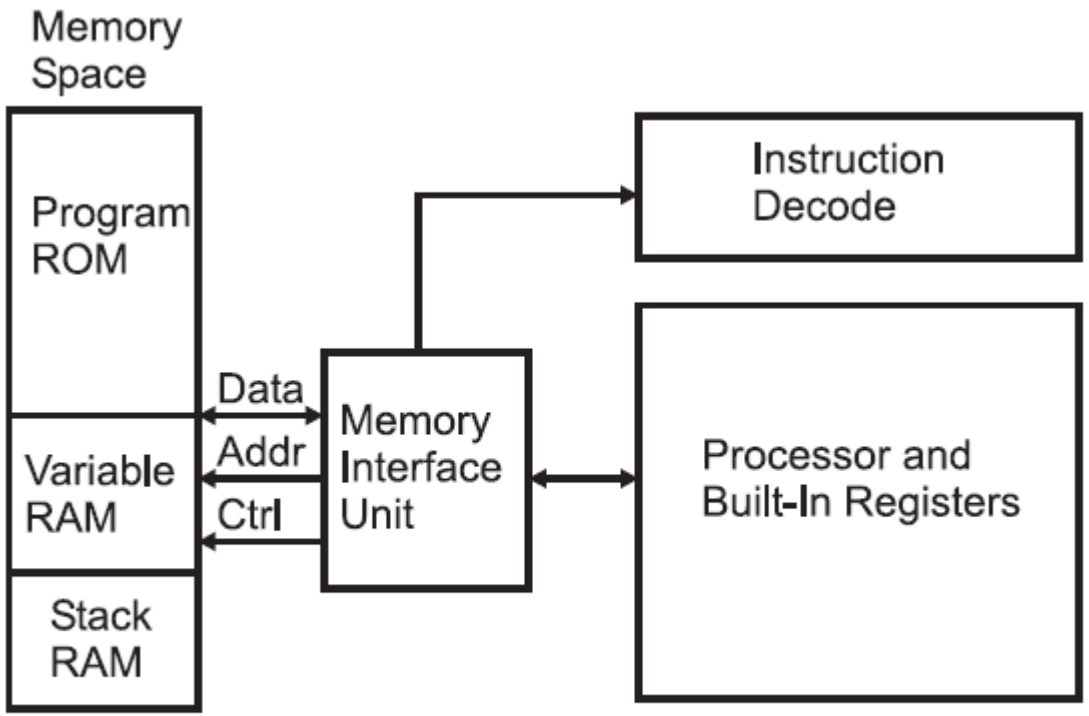
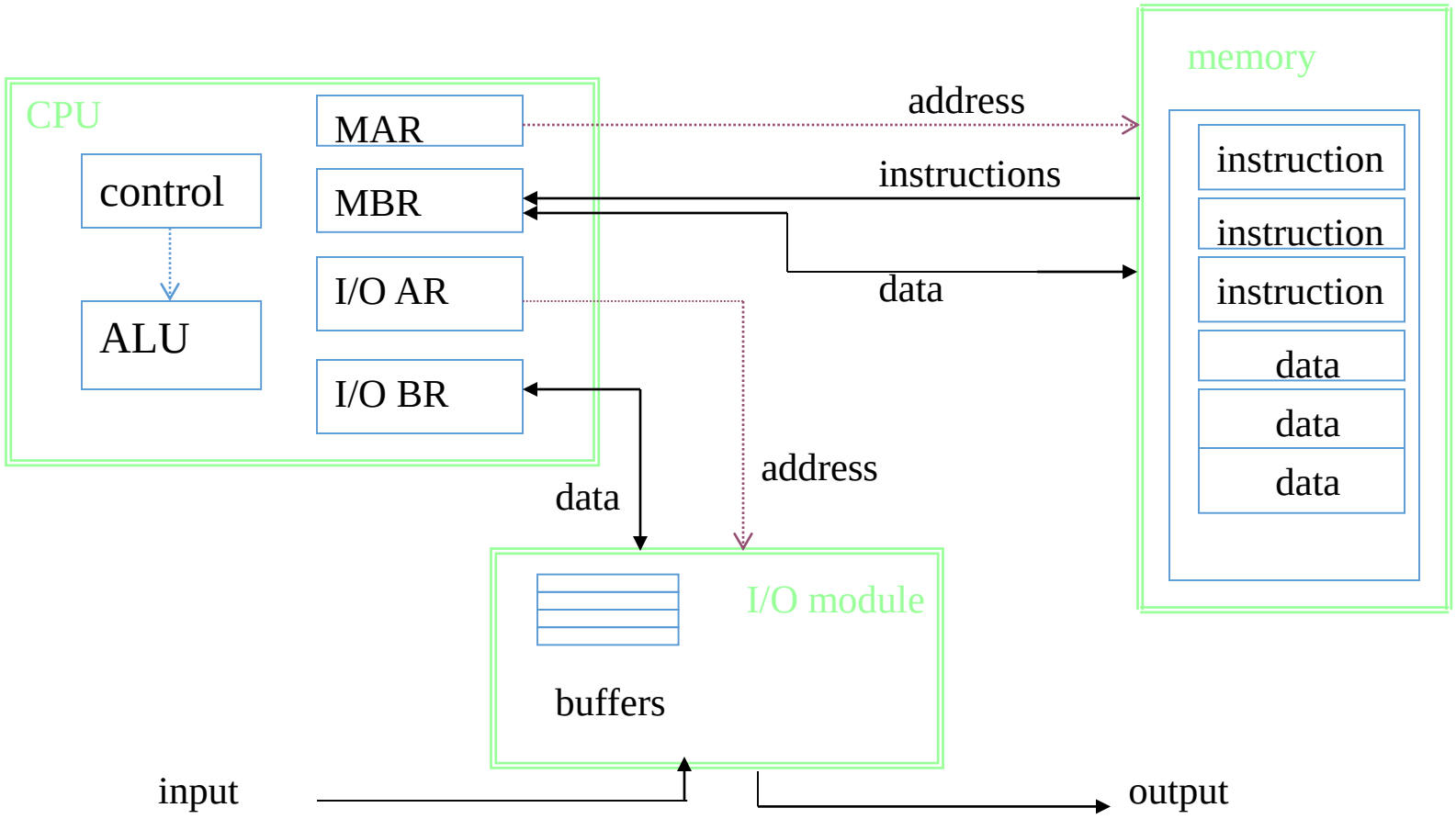


Fig. 12-1. Princeton processor architecture.

System Architecture: The von Neumann Model



Computer architecture classified based on instruction set

- The instruction set for a particular computer determines the way machine language programs are constructed.
- They are two architectures
  - Reduced Instruction Set Computer (RISC)
  - Complex Instruction Set Computer (CISC)

RISC Architecture

- The concept of RISC architecture involves an attempt to reduce execution time by simplifying the instruction set of the computer.

- RISC is computer with limited number of instructions: instructions are fewer and simple instructions. From these basic instructions programmers can derive more complex operations.
- Instructions execute very fast because instructions are very small and simple. Most instructions complete in one cycle, which allows the processor to handle many instructions at same time.
- Uses small set of instructions to make processor design simpler and less costly.
- Usually fixed-length instruction. RISC execute faster in memory and do not use a lot of memory storage. Eg pentium x86
- Instructions are register based and data transfer takes place from register to register.

RISC characteristics

- Relatively few instructions
- Relatively few addressing modes
- Memory access limited to load and store instructions
- All operations done within the registers of the CPU
- Fixed-length, easily decoded instruction format
- Single-cycle instruction execution
- Hardwired rather than micro-programmed control
- A relatively large number of registers in the processor unit
- Use of overlapped register windows to speed-up procedure call and return
- Efficient instruction pipeline
- Compiler support for efficient translation of high-level language programs into machine language programs.

RISC characteristics

- RISC processors have ability to execute one instruction per clock cycle. This is done by overlapping the fetch, decode and execute phases of two or three instructions by using a procedure referred to as pipelining.
- A load or store instruction may require two clock cycles because access to memory takes more register operations.
- Efficient pipelining, as well as a few other characteristics, are sometimes attributed to RISC, although they may exist in non-RISC architectures as well.

CISC Architecture

- As digital hardware became cheaper with the advent of integrated circuits, computer instructions tended to increase both in number and complexity.

- Complex Instruction Set Computer (CISC):
  - Is computer with a large number of instructions.
  - Wide ranging complicated instructions.
  - Have complicated CPU decode circuitry.
  - Often have variable length instructions.
  - And often instructions can operate on memory directly. Data transfer is from memory to memory e.g. MIPS processors
  - In this instructions are not register based.
  - Instructions cannot be completed in one machine cycle.
  - Micro programmed control unit is found in CISC.

CISC characteristics

- A large number of instructions-typically from 100 to 250 instructions
- Some instructions that perform specialized tasks and are used infrequently
- A large variety of addressing modes-typically from 5 to 20 different modes
- Variable-length instruction formats
- Instructions that manipulate operands in memory

Difference Between CISC and RISC

Architectural Characterstics	**Complex Instruction Set Computer(CISC)**	**Reduced Instruction Set Computer(RISC)**
Instruction size and format	Large set of instructions with variable formats (16-64 bits per instruction).	Small set of instructions with fixed format (32 bit).
Data transfer	Memory to memory.	Register to register.
CPU control	Most micro coded using control memory (ROM) but modern CISC use hardwired control.	Mostly hardwired without control memory.
Instruction type	Not register based instructions.	Register based instructions.
Memory access	More memory access.	Less memory access.
Clocks	Includes multi-clocks.	Includes single clock.
Instruction nature	Instructions are complex.	Instructions are reduced and simple.

THE SYSTEM BUSES

Bus is a group of parallel lines carrying digital information between digital devices in a system.

Three types:

- Data bus: Is a bidirectional bus in which information flows in either direction.
- Address bus: Is a unidirectional bus on which the address information flows only in one direction from CPU to memory or IO devices
- control bus: A collection of various control lines.
  - Facilitate data movement within the CPU.

THE CONTROL UNIT

- The function of control unit is to generate relevant timing and control signals to all operations in the computer.
- It controls the flow of data between the processor and memory and peripherals
- Control unit may signal an internal component to place its data on the bus or sample the data on the bus

The Control unit

The control unit performs two basic tasks:

i) ***Sequencing*****:** The control unit causes the processor to step through a series of micro-operations in the proper sequence based on the program being executed.

ii) ***Execution*****:** The control unit causes each micro-operation to be performed

Functions of the Control Unit

- The control unit directs the entire computer system to carry out stored program instructions.
- The control unit must communicate with both the arithmetic logic unit (ALU) and main memory.
- The control unit instructs the arithmetic logic unit which logical or arithmetic operation is to be performed.
- The control unit co-ordinates the activities of the other two units as well as all peripherals and auxiliary storage devices linked to the computer

All micro-operations (prefix *micro* refers to the fact that each step is very simple and accomplishes very little) fall into the following categories

i) Transfer data from register to another

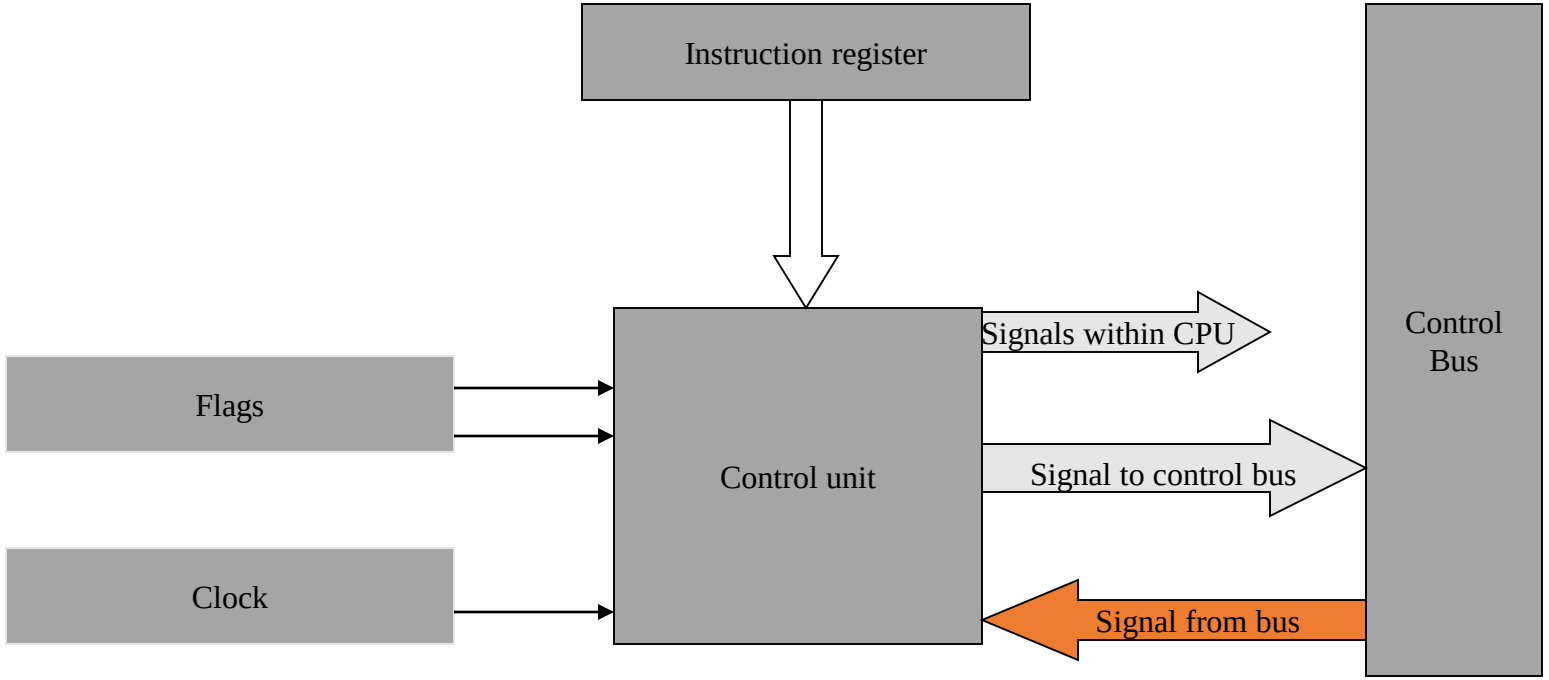
ii) Transfer data from register to external interface (system bus)

iii) Transfer data from an external interface to a register.

iv) Perform an arithmetic and logic operations.

CU block diagram

- CU



CU block diagram

- Consists of:
- i) *Clock:*This is how CU ‘keeps time' The CU causes one micro operation or simultaneous operations to be performed for each clock pulse called clock cycle time.
- ii) *Instruction Register:*the opcode of the current instruction is used to determine which micro operation to perform during the execute cycle.
- iii)F*lags*: needed by the CU to determine the status of processor and the outcome of the previous ALU operations,e.g. for the Increment and Skip if Zero (ISZ) instruction, the CU will increment the PC if zero flag is set.
- iv) *Control signals from control bus:*The control bus portion of the Systems bus provides signal to the control units such as interrupt signals and acknowledgment.
-

Block diagram description:

- The outputs are:
- a) Control signal within the processor: There are two types: those that cause data to be moved from one register to another and those that activate specific ALU functions.
- b) Control signal to the controls bus: Also of two types; Control signal to memory and Control signal to the I/O modules.

Control unit implementation

- **There are two types of control unit implementation**

a) Hard-wired implementation

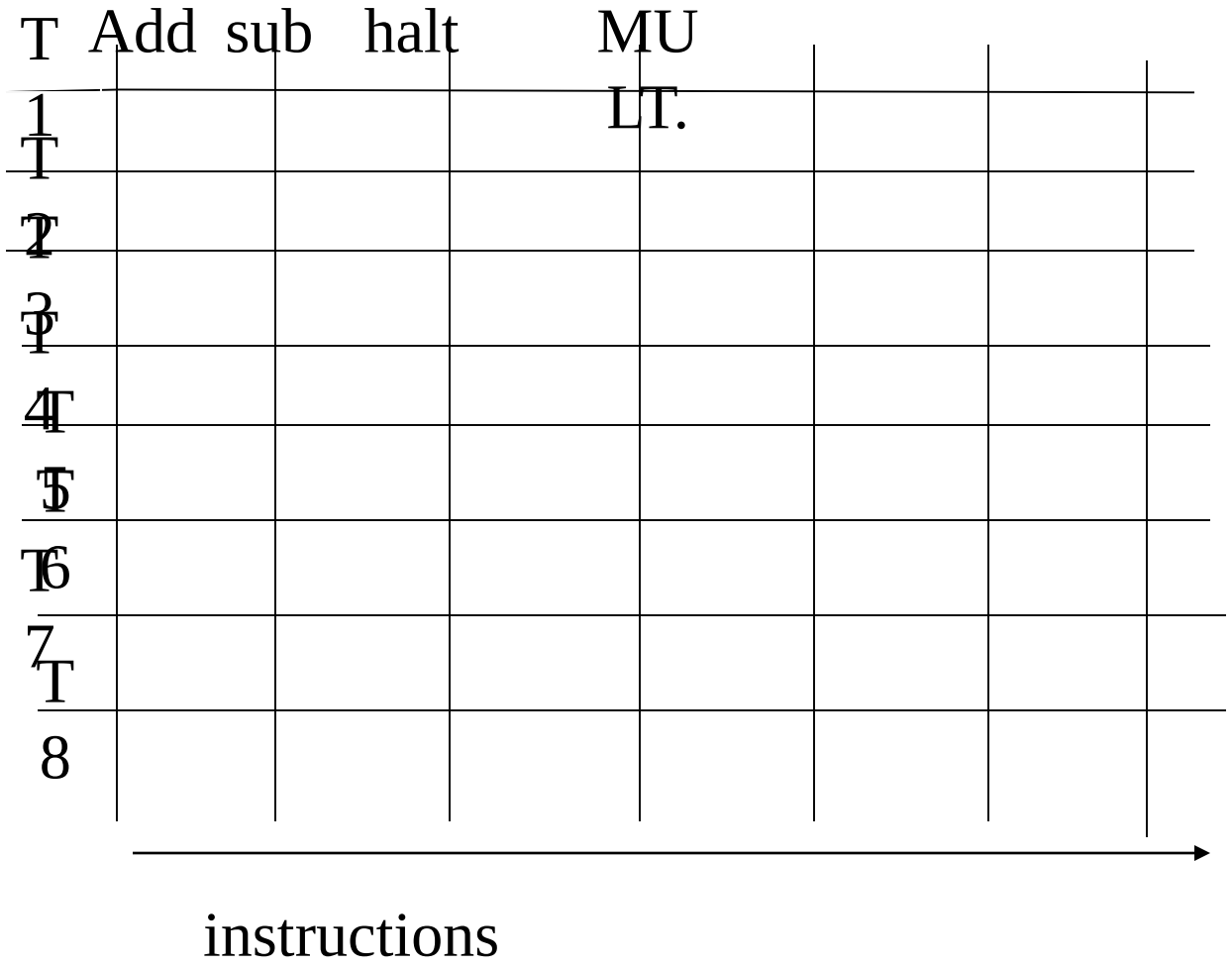
b) Micro-programmed implementation

Hardwired implementation

- It is implemented as logic circuits (gates, flip-flops, decoders etc.) in the hardware
- the control unit is essentially a combinatorial circuit i.e. an interconnection of basic logic elements
- Its input logic signals are transformed into a set of output logic signals which are the control signals i.e. a decoder will have n binary inputs and produce 2^n binary outputs.
- This organization is very complicated if we have a large control unit
- n this organization, if the design has to be modified or changed, requires changes in the wiring among the various components. Thus the modification of all the combinational circuits may be very difficult.

- SEE diagram Lecture 1e.pdf on slide 8 page 2

Hardwired control unit



Hardwired CU

- ✖The timing pulses T1, T2, T3… have definite time delays. They are used as time reference signals.
- ✖For a given instruction the required *micro*-operations are time sequenced using the time pulses.
- ✖E,g for LDA instruction if reading from memory is done in T1storing in accumulator can be done in T2.

Adv/disd

Advantages: Faster than micro-programmed unit of comparable technology

Hardwired Control Unit is fast because control signals are generated by combinational circuits.

- *The delay in generation of control signals depends upon the number of gates.*

Disadvantage:

Must contain complex logic for sequencing through the many micro-operation of instruction cycle.

The design does not give any flexibility

More is the control signals required by CPU; more complex will be the design of control unit.

- *Modifications in control signal are very difficult. That means it requires rearranging of wires in the hardware circuit.*
- *It is difficult to correct mistake in original design or adding new feature in existing design of control unit*

b) The Micro-programmed Control Unit

The micro-program

- Consists of a sequence of *μinstructions* known as micro-program or firmware. A micro-programmed control unit is implemented using programming approach. A sequence of micro- operations are carried out by executing a program consisting of micro-instructions stored in the control memory of the control unit.
- Execution of a micro-instruction is responsible for generation of a set of control signals.
- Iteratively fetches and processes instructions. The format of the micro instruction or control word is as follows.
- i) There is one bit for each internal processor and one bit for each systems bus control line.
- ii) There is a condition field indicating the condition under which there should be a branch.
- iii) There is a field with the address of the micro instructions to be executed next when a branch is taken.

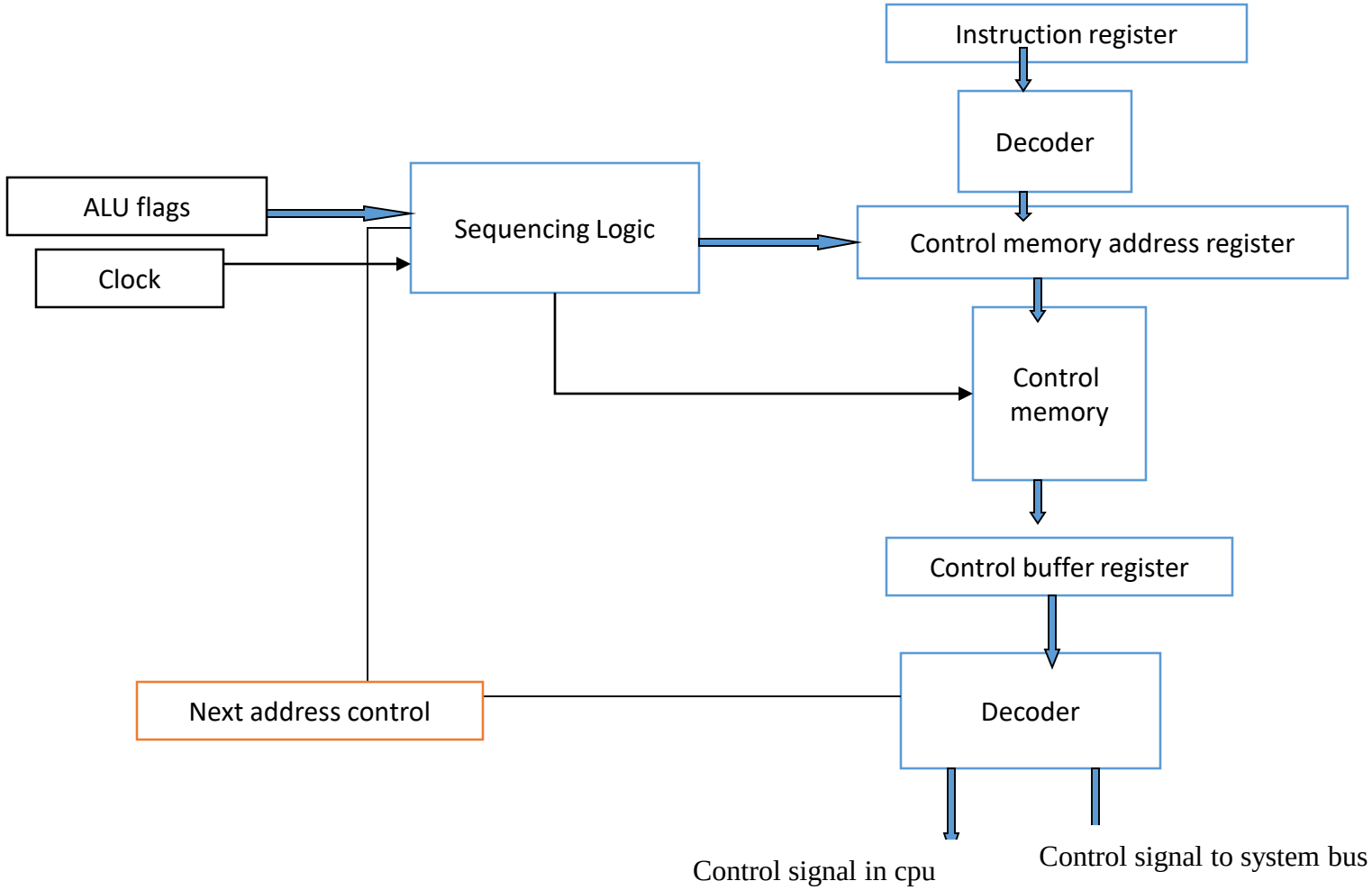
- A micro-instructionconsists of: One or more micro-operations to be executed. Address of next microinstruction to be executed.
- Micro-Operations:The operations performed on the data stored inside the registers are called micro-operations.
- Micro-Programs:Microprogramming is the concept for generating control signals using programs. These programs are called micro-programs.

MICRO-PROGRAMMED CONTROL UNIT

- Micro-Instructions:The instructions that make micro-program are called micro-instructions.
- Micro-Code: Micro-program is a group of micro- instructions. The micro-program can also be termed as micro-code.
- Control Memory: Micro-programs are stored in the read only memory (ROM). That memory is called control memory.

The Micro-programmed Control Unit

CU



Functioning of micro-programmed CU

- 1. To execute an instruction ,the sequencing logic unit issues a READ command to the control memory
- 2. The word whose address is specified in the control address register is read in the control buffer register.
- 3. The content of the control address buffer register generates control signals and next address information for the sequencing logic unit.
- 4. The sequencing logic unit loads a new address into the control address register based on the next address information from the control buffer register and the ALU flags.

ALL these happens during one clock cycle.

ADVANTAGES/DISADVANTAGES

Advantage of micro-programmed: It simplifiers the design of the control unit

The design of micro-program control unit is less complex because micro-programs are implemented using software routines.

- *The micro-programmed control unit is more flexible because design modifications, correction and enhancement is easily possible.*
- *The new or modified instruction set of CPU can be easily implemented by simply rewriting or modifying the contents of control memory.*
- *The fault can be easily diagnosed in the micro-program control unit using diagnosticcs tools by maintaining the contents of flags, registers and counters*

Disadvantage: Its somewhat slower than hard wired of comparable technology.

- The micro-program control unit is slower than hardwired control unit. That means to execute an instruction in micro-program control unit requires more time.
- The micro-program control unit is expensive than hardwired control unit in case of limited hardware resources.
- The design duration of micro-program control unit is more than hardwired control unit for smaller CPU.

Questions:

1. Why microprocessor is called the heart of the computer?
2. What do you mean by 8 bit, 16 bit, 32 bit microprocessor. Why they are named so.
3. Differentiate RISC and CISC.
4. Find out which microprocessor you are using in your computer. Find out its features.
5. What do you mean by pipelining, decoding, instruction format, execution time.

EXTRA information…

- Controller: A device that controls the transfer of data from a computer to a peripheral device and vice versa. • For example, disk drives, display screens, keyboards and printers all require controllers. • In personal computers, the controllers are often single chips. • When you purchase a computer, it comes with all the necessary controllers for standard components, such as the display screen, keyboard, and disk drives. If you attach additional devices, however, you may need to insert new controllers that come on expansion boar
- There are three standard bus architectures for PCs - the AT bus, PCI (Peripheral Component Interconnect) and SCSI.
- When you purchase a controller, therefore, you must ensure that it conforms to the bus architecture that your computer uses.

- Short for Peripheral Component Interconnect, a local bus standard developed by Intel Corporation. • Most modern PCs include a PCI bus in addition to a more general IAS expansion bus. • PCI is also used on newer versions of the Macintosh computer. • PCI is a 64-bit bus, though it is usually implemented as a 32 bit bus. It can run at clock speeds of 33 or 66 MHz. • At 32 bits and 33 MHz, it yields a throughput rate of 133 MBps. • Short for small computer system interface, a parallel interface standard used by Apple Macintosh computers, PCs, and many UNIX systems for attaching peripheral devices to computers. • Nearly all Apple Macintosh computers, excluding only the earliest Macs and the recent iMac, come with a SCSI port for attaching devices such as disk drives and printers.

- SCSI interfaces provide for faster data transmission rates (up to 80 megabytes per second) than standard serial and parallel ports. In addition, you can attach many devices to a single SCSI port, so that SCSI is really an I/O bus rather than simply an interface • Although SCSI is an ANSI standard, there are many variations of it, so two SCSI interfaces may be incompatible. • For example, SCSI supports several types of connectors. • While SCSI has been the standard interface for Macintoshes, the iMac comes with IDE, a less expensive interface, in which the controller is integrated into the disk or CD-ROM drive. • The following varieties of SCSI are currently implemented: • SCSI-1: Uses an 8-bit bus, and supports data rates of 4 MBps.
- SCSI-2: Same as SCSI-1, but uses a 50-pin connector instead of a 25-pin connector, and supports multiple devices. This is what most people mean when they refer to plain SCSI. • Wide SCSI: Uses a wider cable (168 cable lines to 68 pins) to support 16-bit transfers. • Fast SCSI: Uses an 8-bit bus, but doubles the clock rate to support data rates of 10 MBps. • Fast Wide SCSI: Uses a 16-bit bus and supports data rates of 20 MBps. • Ultra SCSI: Uses an 8-bit bus, and supports data rates of 20 MBps. • Wide Ultra2 SCSI: Uses a 16-bit bus and supports data rates of 80 MBps.
- SCSI-3: Uses a 16-bit bus and supports data rates of 40 MBps. Also called Ultra Wide SCSI. • Ultra2 SCSI: Uses an 8-bit bus and supports data rates of 40 MBps.