b) Source HLL Object is LLL  a) Highlight the significance of memory hierarchy. (3 marks)  b) Distinguish between source codes and object codes? (2 marks)  c) State the difference between the following categories of instructions:  i) Arithmetic instructions and logical instructions (2 marks)  ii) Machine control instructions and branching instructions (2 marks)  ii) Machine control instructions and branching instructions (2 marks)  ii) Machine control instructions and branching instructions (2 marks)  iii) Machine control instructions and branching instructions (2 marks)  iii) Machine control instructions and branching instructions (2 marks)  iii) SUI SEH  Code  iii) LDAX B ii) LDAXB Classification in the code of the	of memory with v	aryin	chy is significant because it allows for efficient data access and storage g speeds, capacities, and costs. This hierarchy includes registers, cac v storage (such as hard drives or SSDs).	
Object is LLL  QUESTION ONE (COMPULSORY) [30 MARKS]  a) Highlight the significance of memory hierarchy.  b) Distinguish between source codes and object codes?  c) State the difference between the following categories of instructions:  i) Arithmetic instructions and logical instructions (2 marks)  ii) Machine control instructions and branching instructions (2 marks)  d) For each of the instruction below, state its category and write its hexcode:  i) SUI SEH  Category Arithmetic instruction  (2 marks)  (3 marks)  d) For each of the instruction below, state its category and write its hexcode:  i) SUI SEH  Category Data transfer instruction (2 marks)  Hexcode: (3) However, (4) However, (4) However, (5) However, (6) However, (7)	b) Source HLL			
a) Highlight the significance of memory hierarchy.  b) Distinguish between source codes and object codes?  c) State the difference between the following categories of instructions:  i) Arithmetic instructions and logical instructions  ii) Machine control instructions and branching instructions (2 marks)  iii) Machine control instructions and branching instructions (2 marks)  d) For each of the instruction below, state its category, and write its hexcode:  code  iii) SUI SEH  code  iii) LDAXB ii) LDAXB Category, Data transfer instruction (2 marks)  Hexcode: OA  Hexcode: OA  iii) CM 4000H, ii) CM 4000H Category, Control transfer instruction (3 marks)  Hexcode: OA  iii) CM 4000H, iii) CM 4000H Category, Control transfer instruction (3 marks)  Hexcode: OA  iii) CM 4000H, iii) CM 4000H Category, Control transfer instruction (3 marks)  Hexcode: OA  iii) CM 4000H, iii) CM 4000H Category, Control transfer instruction (3 marks)  Hexcode: OA  iii) CM 4000H, iii) CM 4000H Category, Control transfer instruction (3 marks)  Hexcode: OA  iii) CM 4000H, iii) CM 4000H Category, Control transfer instruction (3 marks)  Hexcode: OA  iii) CM 4000H, iii) CM 4000H Category, Control transfer instruction (3 marks)  Logical-logical operation AND OR XOR NOR  A			OUESTION ONE (COMPULSORY) [30 MARKS]	
State the difference between the following categories of instructions:  i) Arithmetic instructions and logical instructions:  ii) Machine control instructions and branching instructions:  ii) Machine control instructions and branching instructions:  iii) SUI SEH Category: Arithmetic instruction  iii) SUI SEH Category: Arithmetic instruction (2 marks)  iii) CM 4000H <sub>iii</sub> ) CM 4000H Category: Control transfer instruction (2 marks)  Hexode: OA Hexode:		a)	Highlight the significance of memory hierarchy.	(3 marks)
i) Arithmetic instructions and logical instructions (2 marks)  ii) Machine control instructions and branching instructions (2 marks)  d) For each of the instruction below, state its category and write its hexcode:  i) SUI SEH Category. Arithmetic instruction (2 marks)  iii) LDAX B i) LDAXB Category. Data transfer instruction (2 marks)  Hexcode: OA Hexc		b)		
ii) Machine control instructions and branching instructions (2 marks)  d) For each of the instruction below, state its category and write its hexcode:  ii) SUI SEH  Category. Affirmétic instruction  Hexcode: SUI - D6, SEH - Not a stan(2 marks) below the state of th		c)		
ii) Machine control instruction below, state its category and write its hexcode:  i) SUI SEH  ii) SUI SEH  iii) Code  iii) LDAXB ii) LDAXB  Category: Data transfer instruction (2 marks)  Hexcode: ON  Category: Control transfer instruction (2 marks)  Hexcode: ON  Category: Control transfer instruction (3 marks)  Hexcode: ON  Category: Control transfer instruction (3 marks)  Hexcode: ON  The figure below shows a memory Schip  Category: Control transfer instruction (3 marks)  Provided in the figure below shows a memory Schip  Category: Control transfer instruction (3 marks)  Provided in the figure below shows a memory Schip  Category: Control transfer instruction (3 marks)  Provided in the figure below shows a memory schip  Category: Control transfer instruction (3 marks)  Provided in the figure below shows a memory schip in the figure schip in the figure schip in the figure schip in the figure in the			i) Arithmetic instructions and logical instructions	(2 marks)
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ii) LDAX B iii) LDAX B (iii) CM 4000H Category: Data transfer instruction (2 marks) Hexacede: 0A (2 marks) Hexaced		d)	For each of the instruction below, state its category and write its i) SUI SEH Category: Arithmetic instruction	
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A didition, subtraction, multiplication, division Logical-logical operation AND OR XOR NOR  ii) Machine control- control flow of execution loading, storing and moving.  Branching - changing direction of execution eg logical flowers and moving.  Branching - changing direction of execution eg lump, subroutine calls.  iii) The memory organization refers to how the memory is arranged and accessed. This can include details such as the size of each memory specific information about the memory chap in the figure, it is not possit to determine its exact memory organization.  ii) the number of address pins 11 address pins  (1 mark)  iii) the address range of the chip 241 = 2048  Write an ALP to subtract contents of memory 2010h from 2011h Mova X, [2011H]; Subtract contents of memory location 2011h from 2011h Mova X, [2011H]; Subtract contents of memory location 2011h from 2011h Mova X, [2011H]; Subtract the content of memory location 2010h from 301  III) Reset out being reset  ii) READY signal used to delay microprocessor read/ write till peripheral is resolved at a content sort of the subtract		e)	The figure below shows a memory chip.	
ii) the number of address pins 11 address pins  i) the memory organization of the IC.  iii) the address range of the chip 241 = 2048  Write an ALP to subtract contents of memory 2010h from 2011h (5 marks)  Write an ALP to subtract contents of memory location 2011H to register Ax  SUB AX, (2010H); Subtract the content of memory location 2011H to register Ax  SUB AX, (2010H); Subtract the content of memory location 2011H to register Ax  III) Reset out being reset  ii) INTR interrupt request; general purpose interrupt  iii) READY signal used to delay microprocessor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a content some processor read/ write till peripheral is resolved at a cont			addition, subtraction, multipli	cation, division •
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the memory organization of the IC.  (ii) the address range of the chip2^11 = 2048  Write an ALP to subtract contents of memory 2010h from 2011h  MOV AX, [2011H]: Move the content of memory location 2011H to register AX  SUB AX, [2010H]: Subtract the content of memory location 2010H from AX  QUESTION TWO  [20 MARKS]  a) Highlight the functions of the following pins of 8085uP  i) Reset out being reset  ii) INTR interrupt request: general purpose interrupt  iii) READY signal used to delay microprocessor read/ write till peripheral is ready watered at a content of memory location 2010H from AX  QUESTION TWO  [20 MARKS]  b) Dissemble each machine instruction below and state is the state of				
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MOV AX, [2011H] : Move the content of memory 2010h from 2011k (5 marks) SUB AX, [2010H] : Subtract the content of memory location 2010h from AX QUESTION TWO  [20 MARKS]  a) Highlight the functions of the following pins of 8085uP  i) Reset out being reset  ii) INTR interrupt request: general purpose interrupt  iii) READY signal used to delay microprocessor read/write till peripheral is result of a receive data (2 marks)  b) Dissemble each machine instruction below and state is resulted as (2 marks)  i) C6H 45HThis instruction moves the immediate data (45H) into the  ii) 21H, 00th memory location specified by the address.  c) Dissinguish between an instruction: PUSH AX  c) Dissinguish between an instruction format and instruction, setuding the 4rm marks of the layout and structure of an individual machine language instructions that a particular CPU or receive an executive the layout and structure of the accumulator and the status of the flag bits after each of the following operations:  i) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  TEL IID semble program to multiply a value 12H by 8 and provide output through port				
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a) Highlight the functions of the following pins of 8085uP  i) Reset out being reset  ii) INTR interrupt request: general purpose interrupt  iii) READY signal used to delay microprocessor read/ write till peripheral is ready to send or receive data (2 marks)  iii) READY signal used to delay microprocessor read/ write till peripheral is ready to send or receive data (2 marks)  iii) INTA interrupt acknowledge  Dissemble each machine instruction below and state its fast (2 marks)  i) C6H 45H This instruction moves the immediate data (45H) into the  ii) 21H, 00H memory location specified by the address.  iii) 0AH Disassembled instruction: MOV AX, 00FFH  iii) 0AH Disassembled instruction: PUSH AX  c) Distinguish between an instruction format and instruction, reducing the 4H marks)  instruction format refers to the layout and structure of an individual machine language instruction, reducing the 4H marks)  instruction code, source and destination register, instruction set refers to the contents of instructions that a particular CPU or miletoprocessor can execute.  Show the contents of the accumulator and the status of the flag bits after each of the  ii) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  TELIFIC semble program to multiply a value 12H by 8 and provide output through port			SUB AX, [2010H] ; Subtract the content of memory location 2010H from AX	(5 marks)
ii) Reset out being reset  iii) INTR interrupt request: general purpose interrupt  iiii) READY signal used to delay microprocessor read/ write till peripheral is ready to send or receive data (2 marks)  iv) INTA interrupt acknowledge (2 marks)  i) C6H 45H his instruction below and state its hand the  ii) 21H, 00H, FFH Disassembled instruction: MOV AX, 00FFH  iii) 0AH Disassembled instruction: PUSH AX (2 marks)  c) Distinguish between an instruction format and instruction first and instruction to the layout and structure of an individual machine language instruction. Moduling the arrangement of fields for operation code, source and destination register, instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute.  Show the contents of the accumulator and the status of the flag bits after each of the  ii) 37H+46H  iii) 78H-A9H  TELING semble program to multiply a value 12H by 8 and provide output through port		a)		
ii) INTR interrupt request: general purpose interrupt  READY signal used to delay microprocessor read/ write till peripheral is ready to send or receive data  iv) INTA interrupt acknowledge  Dissemble each machine instruction below and state its fish into the  i) C6H 45H his instruction moves the immediate data (45H) into the  ii) 21H, 00H nemory location specified by the address.  iii) 0AH Disassembled instruction: MOV AX, 00FFH  iii) 0AH Disassembled instruction: PUSH AX  c) Distinguish between an instruction format and instruction format refers to the layout and structure of an individual machine language instruction, ficulting the artifaction of fields for operation code, source and destination register, instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute  a) Show the contents of the accumulator and the status of the flag bits after each of the  ii) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  TELFILE semble program to multiply a value 12H by 8 and provide output through port			i) Reset out being reset	
READY signal used to delay microprocessor read/ write till peripheral is ready to send or receive data  (2 marks)  (2 marks)  (3 marks)  (2 marks)  (3 marks)  (4 marks)  (5)  (6)  (6)  (7)  (8)  (8)  (9)  (9)  (9)  (9)  (1)  (1)  (1)  (1			Boiling 1000t	(2 marks)
Dissemble each machine instruction below and state (45H) into the  i) C6H 45HThis instruction moves the immediate data (45H) into the  ii) 21H, 00H FFH Disassembled instruction: MOV AX, 00FFH  iii) 0AH Disassembled instruction: PUSH AX  c) Distinguish between an instruction format and instruction format refers to the layout and structure of an individual machine language instruction, including the arrangement of fields for operation code, source and destination register instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute.  Show the contents of the accumulator and the status of the flag bits after each of the following operations:  i) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  TEEINO semble program to multiply a value 12H by 8 and provide output through port		6	READY signal used to delay microprocessor read/ write till peripheral is	
iii) 0AH Disassembled instruction: MOV AX, 00FFH  C) Distinguish between an instruction format and instruction fielding the arrangement of fields for operation code, source and desination register, instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute  Show the contents of the accumulator and the status of the flag bits after each of the ii) 37H+46H  iii) 50H + 50H - A0H  TELINOsemble program to multiply a value 12H by 8 and provide output through port		b)	Interrupt detrieviouge	(2 marks)
iii) 0AH Disassembled instruction: MOV AX, 00FFH  C) Distinguish between an instruction format and instruction fielding the arrangement of fields for operation code, source and desination register, instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute  Show the contents of the accumulator and the status of the flag bits after each of the ii) 37H+46H  iii) 50H + 50H - A0H  TELINOsemble program to multiply a value 12H by 8 and provide output through port			C6H 45 This instruction moves the immediate data (45H) into the	
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Instruction format refers to the layout and structure of an individual machine language instruction, including the arrangement of fields for operation code, source and destination register, instruction set refers to the complete collection of instructions that a particular CPU or microprocessor can execute.  [20 MARKS]  Show the contents of the accumulator and the status of the flag bits after each of the following operations:  i) 37H+46H  ii) 50H+50H-A0H  (4 marks)  iii) 78H-A9H  TELITE semble program to multiply a value 12H by 8 and provide output through port			Disassembled instruction: MOV AX, 00FFH Disassembled instruction: PUSH AX	(2 marks)
operation code, source and designation register, instruction set refers to the complete collection of instructions that a particular CPU of increprocessor can execute.  [20 MARKS]  Show the contents of the accumulator and the status of the flag bits after each of the following operations:  i) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  [3 marks]  [3 marks]  [3 marks]  [3 marks]  [4 marks]  [5 ARK 9 marks]		c)	Distinguish between an instruction c	(2 marks)
Show the contents of the accumulator and the status of the flag bits after each of the following operations:  i) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  (3 marks)  (3 marks)  (3 marks)  (3 marks)	instruction forma operation code, s	at refers	s to the layout and structure of an individual machine language instruction, including and destination register, instruction set refers to the complete collection of instruction	the arrangement of fields for
following operations:  i) 37H+46H  ii) 50H + 50H - A0H  iii) 78H-A9H  [3 marks]  (3 marks)  (3 marks)  (3 marks)  (3 marks)  (3 marks)	microprocessor c		COULESTION THREE	
ii) 50H + 50H - A0H iii) 78H-A9H TELLING semble program to multiply a value 12H by 8 and provide output through port		4)	Show the contents of the accumulator and the state	
TELL (3 marks)  (3 marks)  (3 marks)  (3 marks)  (3 marks)  (3 marks)			9 2/11/4011	s after each of the
TELL (3 marks)  (3 marks)  (3 marks)  (3 marks)  (3 marks)  (3 marks)		1	11) 50H + 50H - A0H	(4 marks)
SPARK 9. (3 marks)		b)	1111 /XH_AQD	da
SPARK 9 <sub>T</sub> (10 marks)	000		8011	(3 marks)
(10 marks)			SPARK 9.	ide output through port
				(10 marks)

**OUESTION FOUR** 

## [20 MARKS]

Describe the stages of executing a POP D instruction in the microprocessor. (4 marks)

Below is a delay program.

- Fetch: The microprocessor fetches the POP D instruction

from memory.

LXI B, 3400H - Decode: The microprocessor decodes the POP D instruction to identify that it is a pop operation and

DELAY: DCX B

determines the destination register (D) where the data will be popped from the stack.

MOV A, C

- Memory Access: The microprocessor accesses the

ORA B JNZ DELAY

HLT

memory location pointed to by the stack pointer to retrieve the data to be popped. The stack pointer is decremented to point to the next location on the stack.

· Write: The data retrieved from the stack is written into the destination register (D).

i) Given a clock frequency of 3MHz, calculate the duration of the delay program

(7 marks)

ii) Write the algorithm of a delay program

(5 marks)

iii) Convert the assembly language of the delay program into hand code. (4 marks)

ORG 0000H

QUESTION FIVE Start

[20 MARKS]

START: MOV A, 4200H; Read memory address

Read memory address 4200H

MOV COUNTER, A; Set COUNTER = input

Reads a memory address 4200H

Set COUNTER = input ii. set COUNTER to be equal to the read input LOOP: DJNZ COUNTER, READ\_NEXT;

Decrement COUNTER and jump if not zero HLT; End program

Decrement COUNTERiii. decrements COUNTER to zero

(8 marks)

Read next memory address reads the next memory address and repeats steps (ii) to (iv)

READ\_NEXT: INC C 4200H : Read next memory

b) Write a ALP program for part (a) above. Repeat steps (ii) to (iv) until COUNTER = 0

JMP LOOP; Jump back to LOOP

## INSTRUCTION SET OF 8085

HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL -	HEX	(
00	NOP	25	DCR H	4A	MOV C, D	6F	MOV L, A	94	SUB H	B9	CMP C	DE	SE
01	LXIB, D16	26	MVI H, D8	4B	MOV C, E	70	MOV M, B	95	SUB L	BA	CMP D	DF	R
02	STAX B	27	DAA	4C	MOV C, H	71	MOV M, C	96	SUB M	BB	CMP E	EO	R
03	INX B	28		4D	MOV C, A	72	MOV M, D	97	SUB A	BC	CMP H	E1	P
04	INR B	29	DADH	4E	MOV C, M	73	MOV M, E	98	SBB B	BD	CMP L	E2	JF
05	DCR B	2A	LHLD Adr	4F	MOV C, A	74	MOV M, H	99	SBB C	BE	CMP M	E3	X
06	MVI B, D8	2B	DCX H	50	MOV D, B	75	MOV M, L	9A	SBB D	BF	CMP A	E4	C
07	RLC	2C	INR L	51	MOV D, C	76	HLT	9B	SBB E	C0	RNZ	E5	PI
08	-	2D	DCR L	52	MOV D, D	77	MOV M, A	9C	SBB H	C1	POP B	E6	A
09	DADB	2E	MVI L, D8	53	MOV D, E	78	MOV A, B	9D	SBB L	C2	JNZ Adr	E7	
0A	LDAX'B	2F	CMA	54	MOV D, H	79	MOV A, C	9E	SBB M	C3	JMP Adr	E8	
0B	DCX B	30	SIM	55	MOV D, L	7A	MOV A, D	9F	SBB A	C4	CNZ Adr	E9	
0C	INR C	31	LXI SP, D16	56	MOV D, M	7B	MOV A, E	A0	ANA B	C5	PUSH B	EA	JP
0D	DCR C	32	STA Adr	57	MOV D, A	7C	MOV A, H	A1	ANA C	C6	ADI D8	EB	
0E	MVI C, D8	33	INX SP	58	MOV E, B	7D	MOV A, L	A2	ANA D	C7	RST 0	EC	CI
0F	RRC	34	INR M	59	MOV E, C	7E	MOV A, M	A3	ANA E	C8	RZ	ED	-
10	-	35	DCR M	5A	MOV E, D	7F	MOV A, A	A4	ANA H	C9	RET Adr	EE	
11	LXI D, D8	36	MVI M, D8	5B	MOV E, E	80	ADD B	A.5	ANA L	CA	JZ	EF	
12	STAX D	37	STC	5C	MOV E, H	81	ADD C	A6	ANA M	CB	-	F0	
13	INX D	38		5D	MOV E, L	82	ADD D	A7	ANA A	CC	CZ Adr		PC
14	INR D	39	DAD SP	5E	MOV E, M	83	ADD E	A8	XRA B	CD	CALL Adr	F2	-
15	DCR D	3A	LDA Adr	5F	MOV E, A	84	ADD H	A9	XRA C	CE	ACI D8	-	D
16	MVI D, D8		DCX SP	60	MOV H, B	85	ADD L	AA	XRA D	CF	RST 1	F4	100
17	RAL		INR A	61	MOV H, C	86	ADD M	AB	XRA E	D0	RNC	F5	PI