8255 Programmable Interface

Intel's 8255 A programmable peripheral interface provides a good example of a parallel interface. As
shown in Figure 4.2, the interface contain a control register and three separately addressable ports, denoted
A, B, and C. Whether or not an 8255A is being accessed is determined by the signal on the CS pin and the
direction of the access is according to the RD ad WR signals. Which of the four registers is being addressed
is determined by the signals applied to the pins A1 and A0. Therefore, the lowest port address assigned to
an 8255 A must be divisible by 4. A summary of the 8255 A's addressing is:

A1 A0 RD WR CS Transfer Description
0 0 0 1 0 Port A to data bus
0 1 0 1 0 Port B to data bus
1 0 0 1 0 Port C to data bus
0 0 1 0 0 Data bus to port A
0 1 1 0 0 Data bus to port B
1 0 1 0 0 Data bus to port C
1 1 1 0 0 Data bus to control register if D7= 1; if D7=0 input from the data
bus is treated as a Set/Reset instruction
x x x x 1 D7-D0 go to high-impedance state
1 1 0 1 0 Illegal combination
x x 1 1 0 D7-D0 go to high-impedance state
Where 0 is low and 1 is high

Because the bits in port C are sometimes used as control bits, the 8255 A is designed so that they can be output to individually using a Set/Reset instruction. When the 8255 A receives a byte that is directed to its control register, it examines the data bit 7.

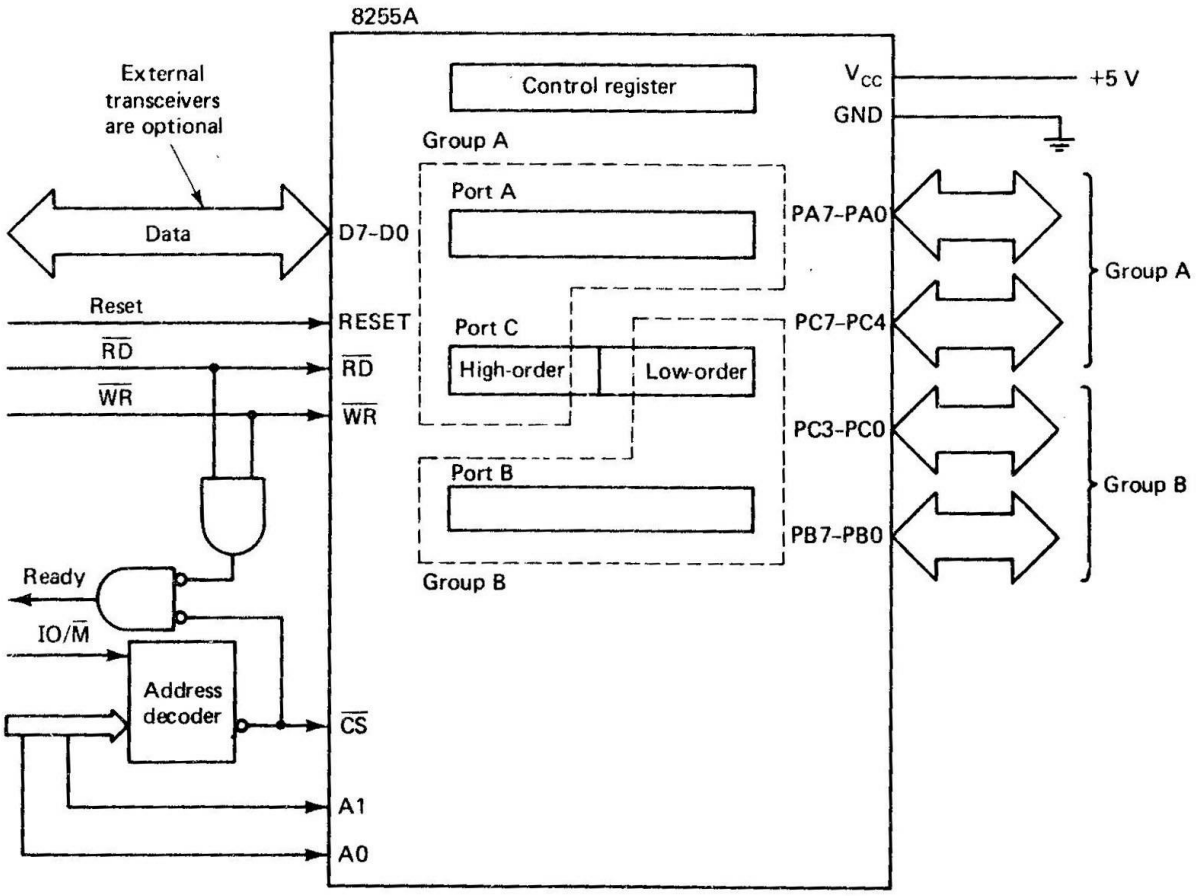

Figure 4.2: Diagram of the 8255 A

If this bit is 1, the data are transferred to the control register, but if it is 0, the data re treated as a Set/Reset instruction and is used to set or clear the port C it specified by the instruction. Bits 3-1 give the bit number

of the bit to be changed and bit 0 indicates whether it is to be set or cleared. The remaining bits are unused.

The bits in the three ports are attached to pins that may be connected to the I/O device. These bits are divided into groups A and B, with group A consisting of the bits in port A and the four MSBs of port C and group b consisting of port B and the four LSBs of port C. the use of each of the two groups is controlled by the mode associated with it. Group A is associated with one of three modes, mode 0, mode 1, and mode 2, and group B with one of two modes, mode 0 and mode 1. The modes are determined by the contents of the control register, whose format is given in

Fig. 4.3. These modes are:

Mode 0: If a group is in mode 0, it is divided into two sets. For group A these sets are port A ad the upper 4 bits of port C, and for group B they are port B ad the lower 4 bits of port C. each set may be used for inputting or outputting, but not both. Bits D4, D3, D1, and D0 in the control register specify which sets are for input and which are for output.

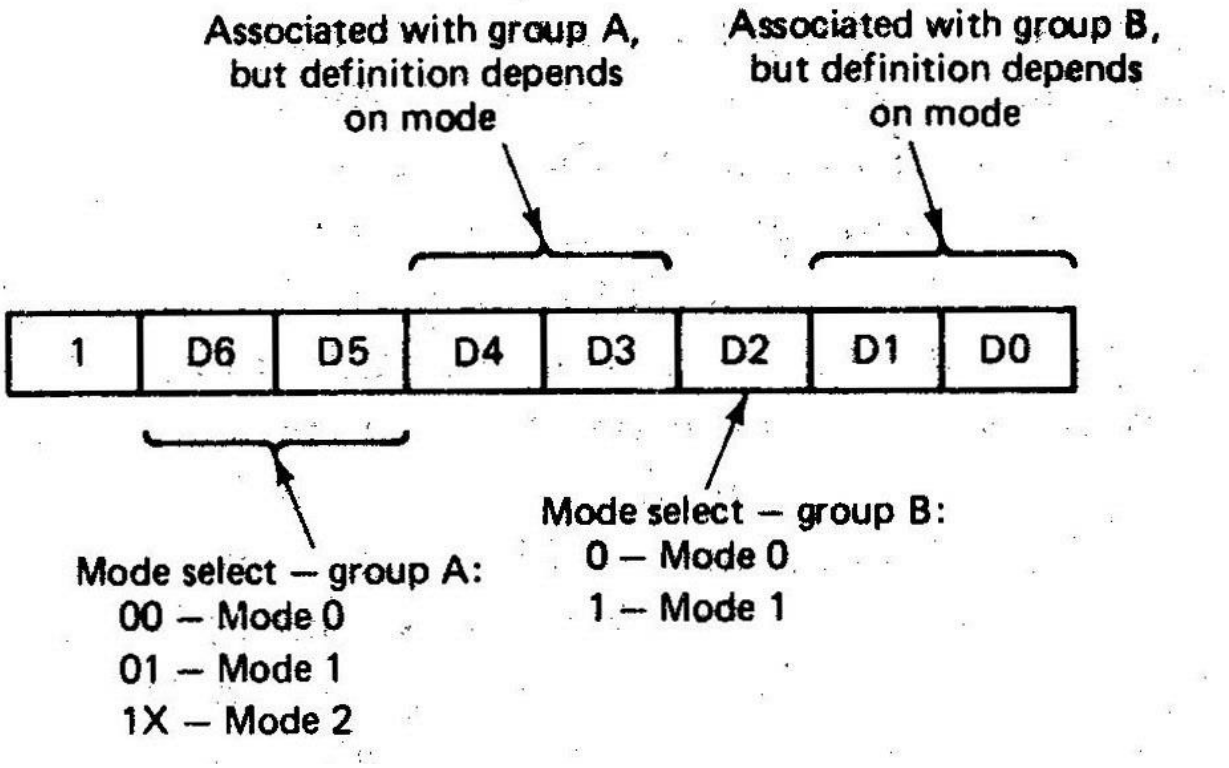

Figure 4.3: Format of the 8255 A's control register.

These bits are associated with the sets as follows:

D4 - Port A.

D3 - Upper half of port C.

D1 - Port B.

D0 – Lower half of port C.

If a bit is 0, then the corresponding set is used for output; if it is 1, the set is for input.

Mode 1: When group A is in this mode port A is used for input or output according to bit D4 (d4=1

indicates input), and the upper half of ports C is used for handshaking and control signals. For inputting, the

four MSBs of port C are assigned the following symbols and definition:

PC4	STBA	A 0 applied to this pin causes PA7-PA0 to be latched, or "strobed," into port A.
PC5	IBFA	Indicates that the input buffer is full. It is 1 when port A contains data that have not yet been input to the CPU. When a 0 is on this pin the device can input a new byte to the interface.
PC6,	PC7	May be used to output control signals to the device or input status from the device. If D3 of the control register is 0, they are for outputting control signals; otherwise, they are for inputting status.

For outputing

PC4,	PC5	Serve the same purpose as described above for PC6 and PC7
PC7	OBFA	indicates that the output buffer is full. It outputs a 0 to the device when port A is outputting new data to be taken by the device.
PC6	ACKA	Device puts a 0 on this pin when it accepts data from port A.

In mode 1, PC3 is denoted INTERA and is associated with group A. It is used as an interrupt request line and is tied to one of the IR line in the system bus. When inputting to port A, this pin becomes 1 when new data are put in port A (i. e., it is controlled by PC4) and is cleared when the CPU takes the data. For output, this pin is set to 1 when the contents of port A are taken by the device as cleared when new data are sent from the CPU. If group B is in mode 1, port B is input to or output from according to bit D1 of the control register (D1=1 indicates input). For input, PC2 and PC1 are denoted STBB and IBFB, respectively, and serve the same purposes for group B as STBAAND IFBA do for group A. Similarly, for output PC1 and PC2 are denoted OBFB and ACKB. PC0 becomes INTERB and its use is analogous to that of INTRA. The interrupt enable for group A is controlled by setting or clearing integral flags. Setting or clearing these flags is simulated by setting or clearing PC4, for input, or PC6, for output, using a Set/Reset instruction.

Similarly, the interrupt enable for group B is controlled by set/clear of PC2 for both input and output.

Mode 2: This mode applies only to group A, although it also uses PC3 for making interrupt requests. In mode 2, port A is a bidirectional port and the four MSBs of port C are defined as follows:

PC4 STB A 0 on this line causes the data on PA7 – PA0 to be strobed into port A.

PC5 IBF_A Becomes 1 when port A is filled with new data from lines PA7 – PA0 and is cleared when these data are taken by the CPU.

PC6 ACK_A Indicates that the device is ready to accept data from PA7-PA0.

PC7 OBFA Becomes 0 when port A is filled with new data from the CPU and is set to 1 when data are taken by the device.

While group A is in mode 2, group B may be in either mode 0 or mode 1. However, if group B is mode 0, only PC2 – PC0 can be used for input or output because group A has borrowed PC3 to use as an interrupt request line. Normally, if group A is in mode, PC2 – PC0 would be connected to control and status pons on the device attached to the port A lines. Port B may used also be used for this purpose.

In all three modes port C reflects the signals on PC7 – PC0 and can be read with an IN instruction.