Memory and Input/ Output Interface

General Bus Operation

The 8086 has a combined address and data bus commonly referred to as a time multiplexed address and data bus. The main reason behind multiplexing address and data over the same pins is the maximum utilization of processor pins and it facilitates the use of 40 pin standard DIP package. The bus can be demultiplexed using a few latches and transceivers, whenever required. In the following text, we will discuss a general bus operation cycle.

Basically, all the processor bus cycles consist of at least four clock cycles. These are referred to as T1, T2,T3 and T4· The address is transmitted by the processor during T1. It is present on the bus only for one cycle.

During T2, i.e. the next cycle, the bus is tristated for changing the direction of bus for the following data read cycle. The data transfer takes place during T3 and T4. In case, an addressed device is slow and shows 'NOT READY status the wait states Tw are inserted between T3 and T4. These clock states during wait period are called idle states (Ti), wait states (Tw) or inactive states. The processor uses these cycles for internal housekeeping. The address latch enable (ALE) signal is emitted during T, by the processor(minimum mode) or the bus controller (maximum mode) depending upon the status of the MN/MX input.

The negative edge of this ALE pulse is used to separate the address and the data or status information. In maximum mode, the status lines S0, S1 and S2 are used to indicate the type of operation as discussed in the pin description of this unit. Status bits BHE/s7 are multiplexed with higher order address bits and the BHE signal. Address is valid during T1 while the status bits S3 to S7 are valid during T2 through T4. The Figure 2.7 shows a general bus operation cycle of 8086.

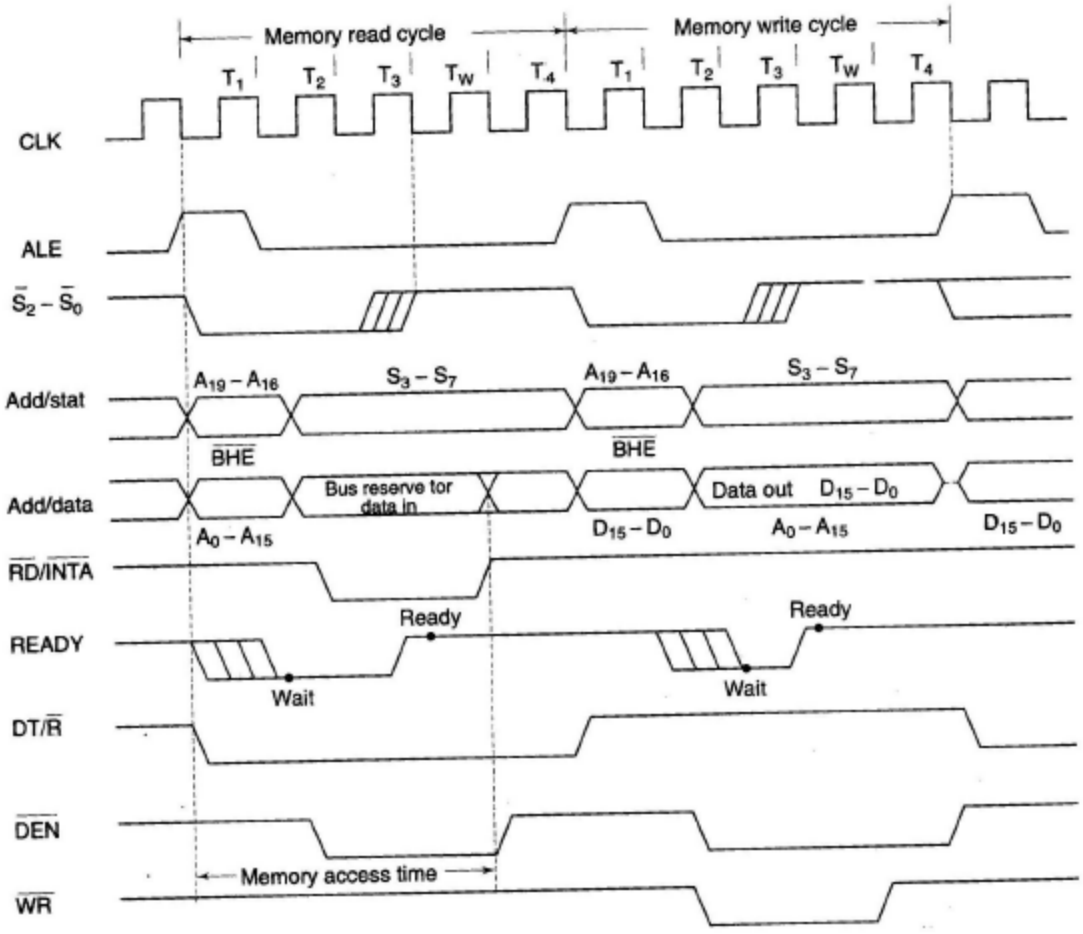

Figure 2.7: General Bus Operation Cycle in Maximum Mode

Minimum mode 8086 system and Timings

In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its MN/MX pin to logic 1. In this mode, all the control signals are given out by the microprocessor chip itself.

There is a single microprocessor in the minimum mode system. The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices. Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.

The latches are generally buffered output D-type flip-flops, like, 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086. Tran receivers are the bi-directional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the

time multiplexed address/data signal. They are controlled by two signals, namely, DEN and DT/R. The DEN signal indicates that the valid data is available on the data bus, while DT/R indicates the direction of data, i.e. from or to the processor. The system contains memory for the monitor and users program storage. Usually, EPROMS are used for monitor storage, while RAMs for users program storage. A system may contain I/O devices for communication with the processor as well as some special purpose I/O devices. The clock generator generates the clock from the crystal oscillator and then shapes it and divides to make it more precise so that it can be used as an accurate timing reference for the system. The clock generator also synchronizes some external signals with the system clock. The general system organization is shown in Figure 2.8. Since it has 20 address lines and 16 data lines, the 8086 CPU requires three octal address latches and two octal data buffers for the complete address and data separation.

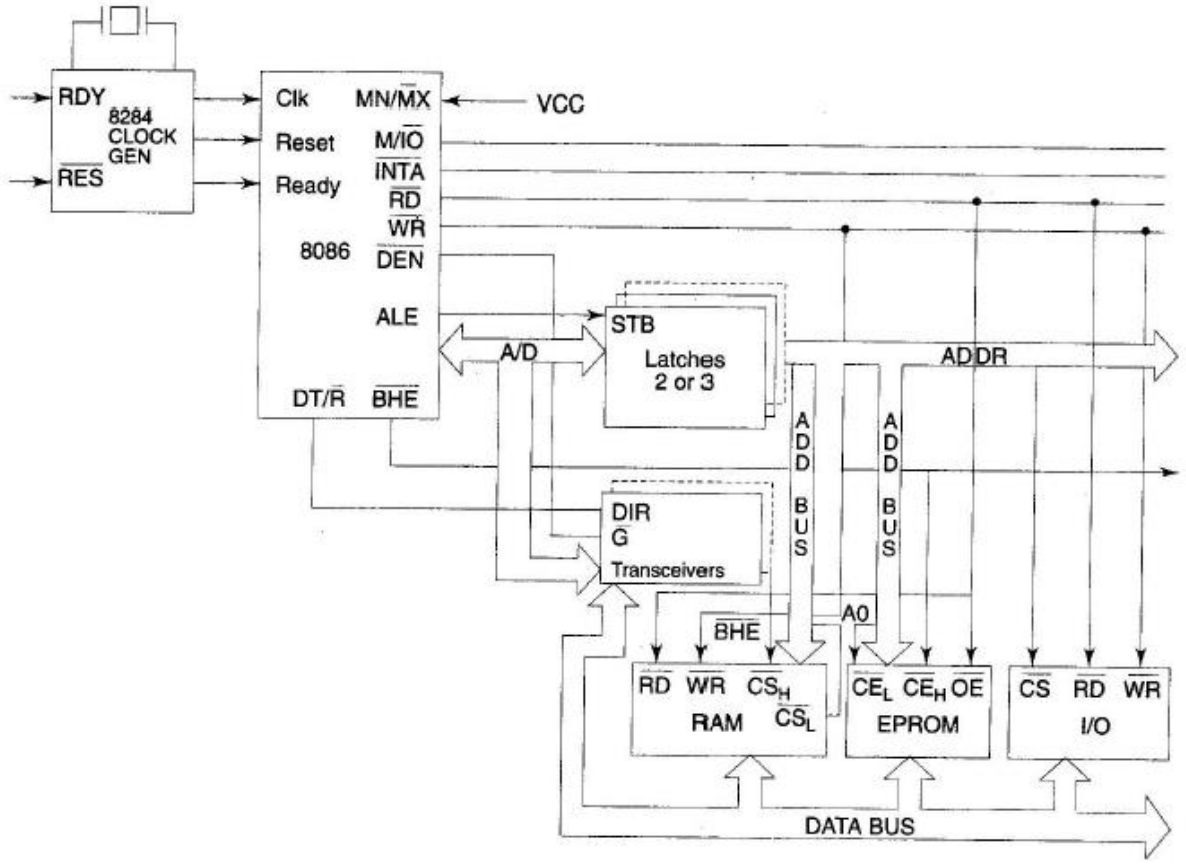

Figure 2.8: Minimum Mode 8086 System

The working of the minimum mode configuration system can be better described in terms of The timing diagrams rather than qualitatively describing the operations. The opcode fetch and read

cycles are similar. Hence the timing diagram can be categorized in two parts) the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal and also M/IO signal. During the negative going edge of this signal, the valid address is latched on the local bus. The BHE and A0 signals address low, high or both bytes. From T1 to T4, the M/IO signal indicates a memory or I/O operation. At T2, the address is removed from the local bus and is sent to the output. The bus is then tristated. The read (RD) control signal is also activated in T2. The read (RD) signal causes the addressed device to enable its data bus drivers. After RD goes low, the valid data is available on the data bus. The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tristate its bus drivers.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO signal isagain asserted to indicate a memory or I/O operation. In Tg, after sending the address in T2, the processor sends the data to be written to the addressed location. The data remains on the bus untill middle of T4 state. The WR becomes active at the beginning of T2 (unlike RD is somewhat delayed in T2 to provide time for floating).

The BHE and AO signals are used to select the proper byte or bytes of memory or I/O word to be read or written as already discussed in the signal description section of this chapter.

The M/IO, RD and WR signals indicate the types of data transfer as specified in Table 2.5.

Table 2.5

M/IO	RD	WR	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory read

Figure 2.9(a): Shows the read cycle while the Figure 2.9(b) shows the write cycle.

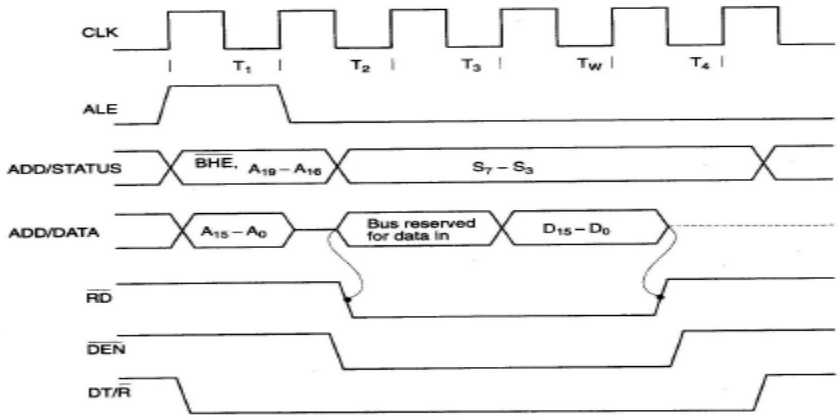

Figure 2.9(a): Read Cyde Timing Diagram for Minimum Mode

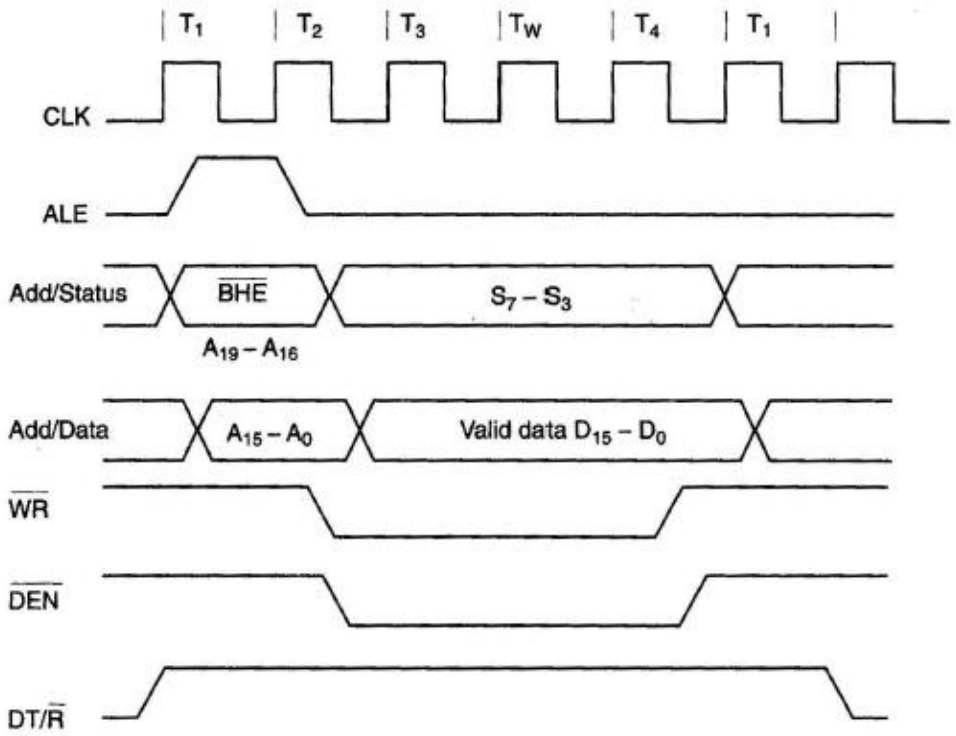

Figure 2.9(b): Write Cycle Timing Diagram for Minimum Operation

Hold response Sequence

The HOLD pin is checked at leading edge of each clock pulse. If it is received active by the processor before T4 of the previous cycle or during T1 state of the current cycle, the CPU activates HLDA in the next clock cycle and for the succeeding bus cycles, the bus will be given

to another requesting master. The control of the bus is not regained by the processor until the requesting master does not drop the HOLD pin low. When the request is dropped by the requesting master, the HLDA is dropped by the processor at the trailing edge of the next clock, as shown in Figure 2.9(c). The other conditions have already been discussed in the signal description section for the HOLD and HLDA signals.

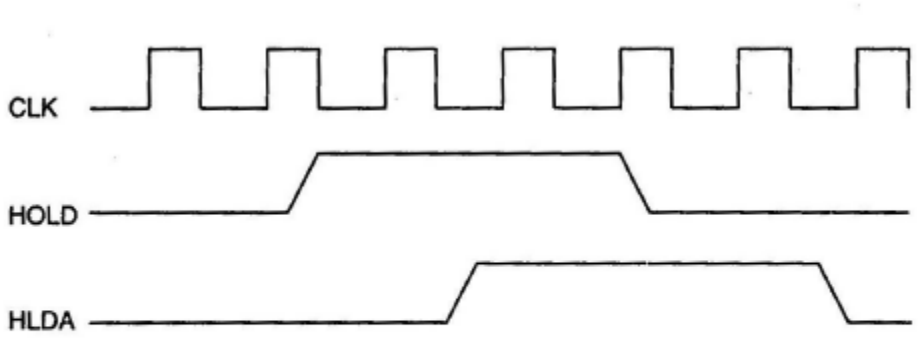

Figure 2.9(c): Bus Request and Bus Grant Timings in Minimum Mode System

The Processor 8088

The launching of the processor 8086 is seen as a remarkable step in the development of high speed computing machines. Before the introduction of 8086 most of the circuits required for the different applications in computing and industrial control fields were already designed around the 8-bit processor 8085. The 8086 imparted tremendous flexibility in the programming as compared to 8085. So naturally, after the introduction of 8086, there was a search for a microprocessor chip which has the programming flexibility like 8086 and the external interface like 8085, so that all the existing circuits built around 8085 can work as before, with this new chip. The chip 8088 was a result of this demand. The microprocessor 8088 has all the programming facilities that 8086 has, along with some hardware features of 8086, like 1Mbyte memory addressing capability, operating modes (MN/MX), interrupt structure etc. However 8088, unlike 8086, has 8-bit data bus. This feature of 8088 makes the circuits, designed around 8085, compatible with 8088, with little or no modification.

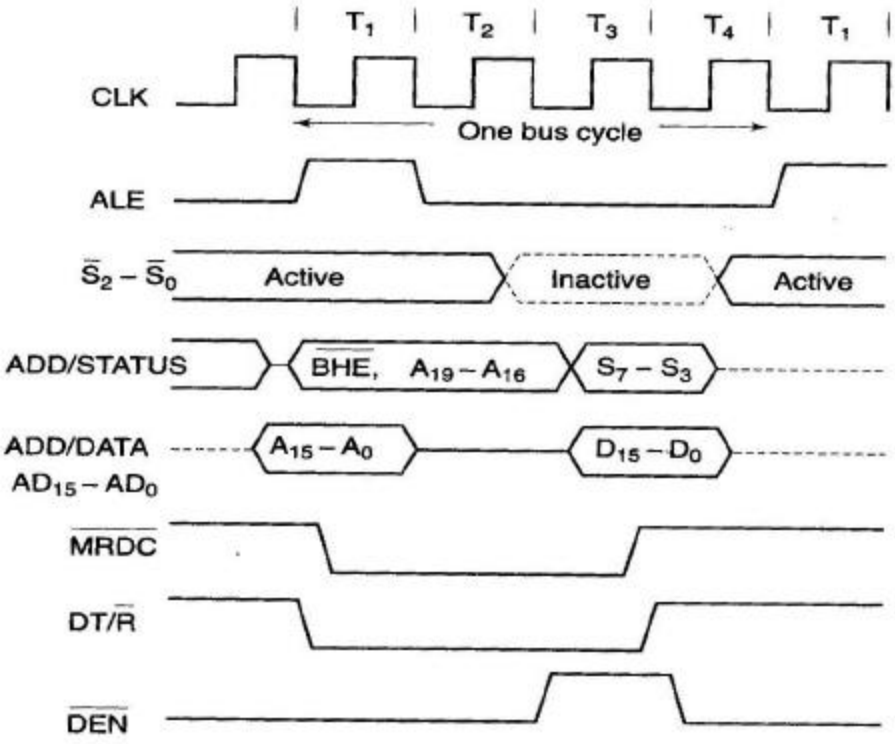

Figure 2.10(a): Memory Read Timing in Maximum Mode

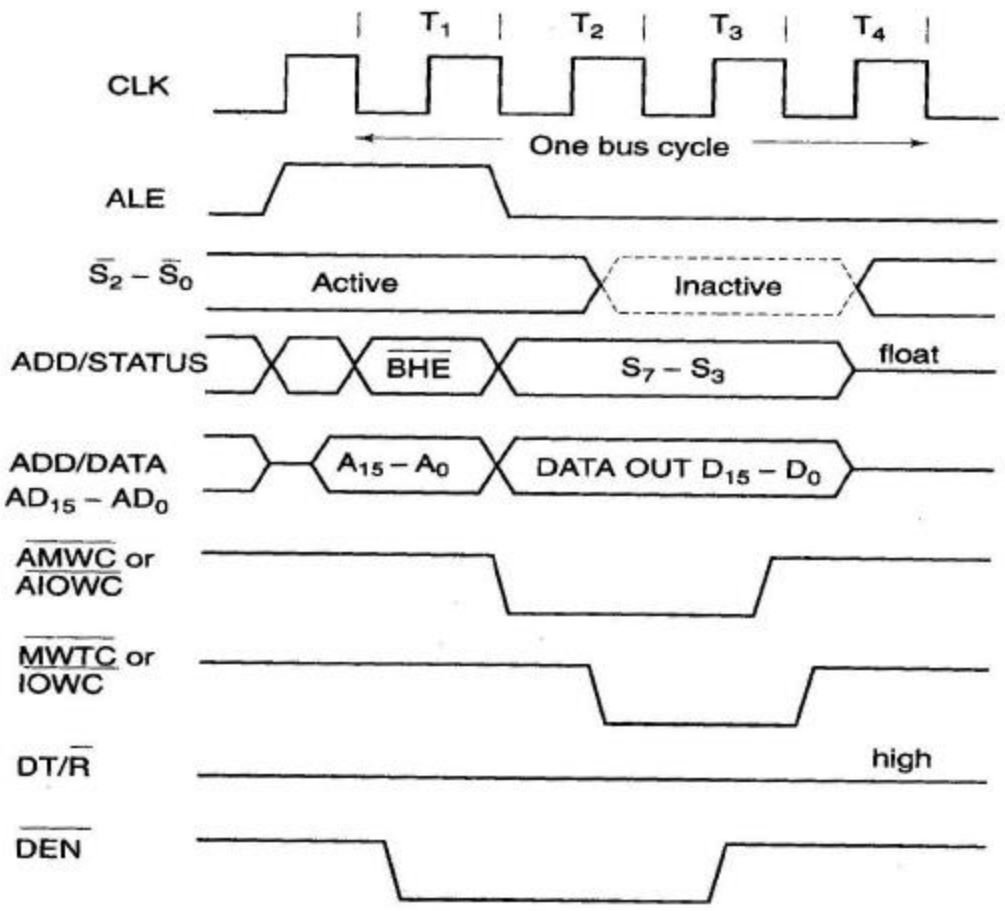

Figure 2.10(b): Memory Write Timing in Maximum Mode

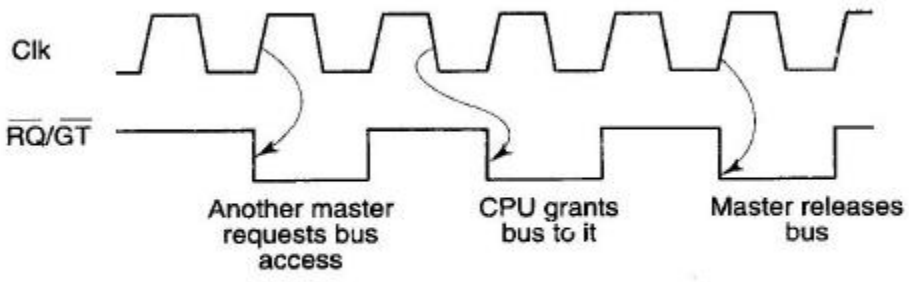

Figure 2.10(c): RQ/GT Timings in Maximum Mode

All the peripheral interfacing schemes with 8088 are the same as those for the 8-bit processors. The memory and I/O addressing schemes are now exactly similar to 8085 schemes except for the increased memory (1Mbyte) and I/O (64Kbyte) capabilities. The architecture shows the developments in 8088 over 8086. Number of abilities and limitations of 8088 are same as 8086.

In this section, we will discuss those properties of 8088 which are different from that of 8086 in some respects.

Architecture 8088

The register set of 8088 is exactly the same as in to 8086. The architecture of 8088 is also similar to 8086 except for two changes; a) 8088 has 4-byte instruction queue and b) 8088 has 8-bit data bus. The function of each block is the same as in 8086. Figure 2.11 shows the 8088 architecture.

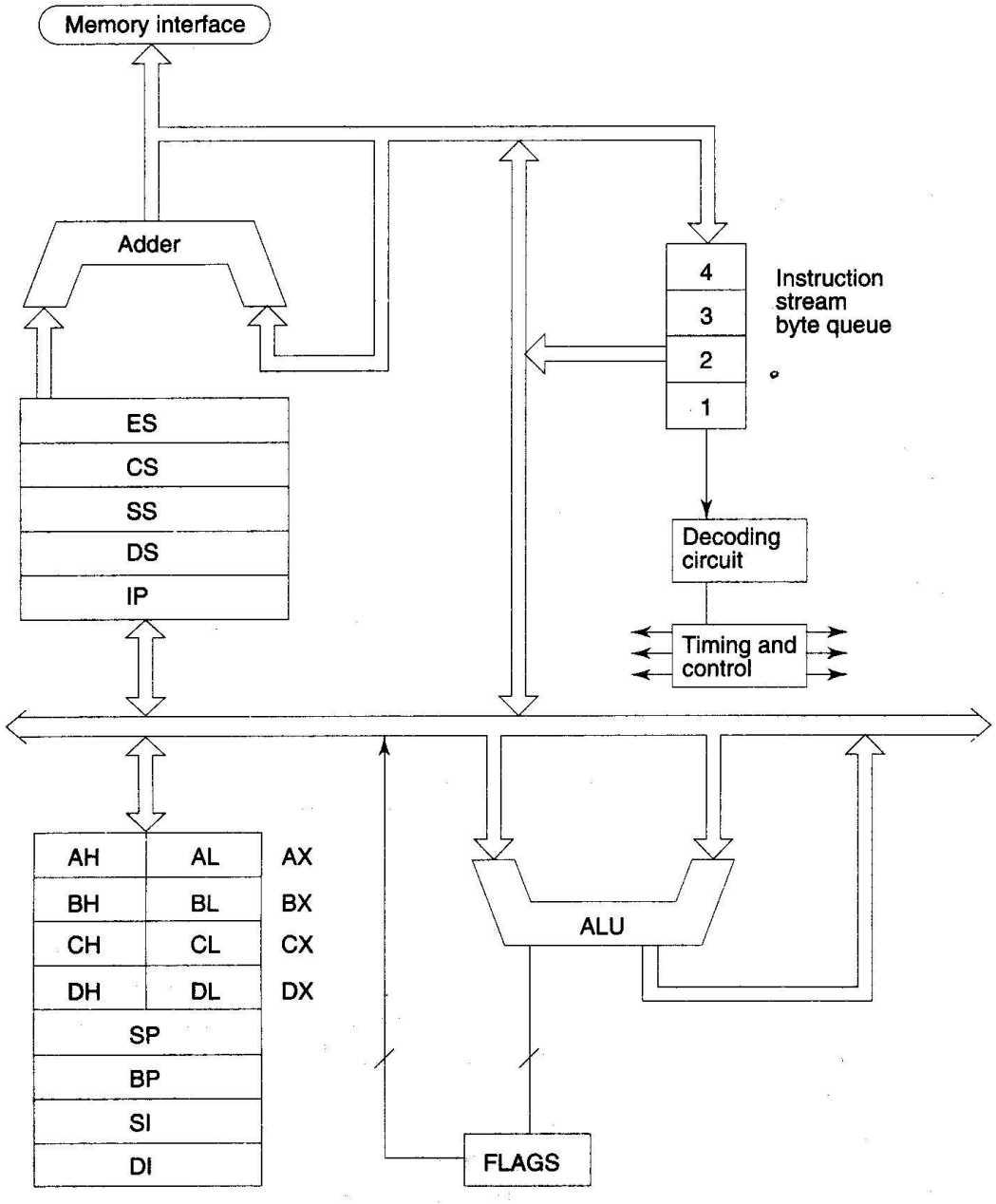

Figure 2.11 Architecture 8088

The addressing capability of 8088 is 1Mbyte, therefore, it needs 20 address bits, i.e. 20 addressing lines.

While handling this 20-bit address, the segmented memory scheme is used and the complete physical address forming procedure is the same as explained in case of 8086. The memory organization and addressing methods of 8088. While physically interfacing memory to 8088, there is nothing like an even address bank or odd address bank. The complete memory is homogeneously addressed as a bank of 1Mbyte memory locations using the segmented memory scheme. This change in hardware is completely transparent to software. As a result of the modified data bus, the 8088 can access only a byte at a time. This fact reduces the speed of operation of 8088 as compared to 8086, but the 8088 can process the 16-bit data internally. On account of this change in bus structure, the 8088 has slightly different timing diagrams than 8086.

The pin diagram of 8088 is shown in Figure 2.12. Most of the 8088 pins and their functions are exactly similar to the corresponding pins of 8086. Hence the pins that have different functions or timings are discussed in this section. Amongst them are the pins that have a common function in minimum and maximum mode.

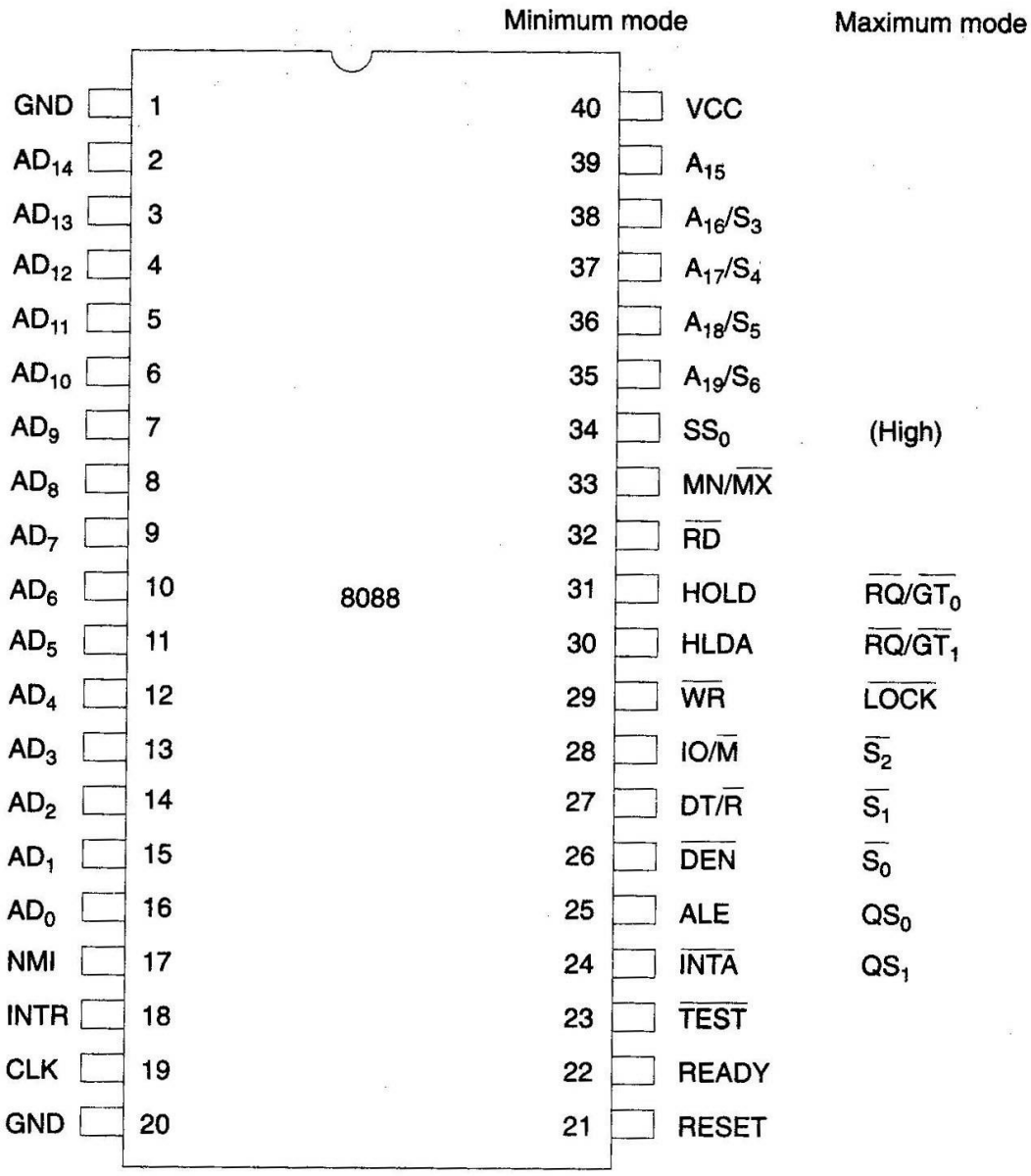

Figure 2.12: Pin Diagram of 8088

AD7-AD0 (Address/Data): These lines constitute the address/data time multiplexed bus. During T1 the bus is used for conducting addresses and during T2, T3, Tw and T4 states these lines are used for conducting data. These are tristate during 'hold acknowledge' and 'interrupt acknowledge' cycles.

A15-A8 (Address Bus): These lines provide the address bits A8 to A15 in the entire bus cycle. These need not be latched for obtaining a stable valid address. These are active high and are

tristated during the 'acknowledge' cycles. Note that, as the 8088 data bus is only of 8 bits, there is no need of the BHE signal.

SS0: A new pin SS0 is introduced in 8088 instead of BHE pin in 8086. In minimum mode, the pin 880 is logically equivalent to the S8 in maximum mode.

IO/M: This pin is similar to M/IO pin of 8086, but it offers an 8085 compatible, memory/IO bus interface.

The signals SS0, DT/R, IO/M can be decoded to interpret the activities of the microprocessor as given in Table 2.6.

Table 2.6

IO/M	DT/R	SS_0	Operation/Interpretation
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O port
1	1	0	Write I/O port
1	1	1	HALT
0	0	0	Code Access
0	0	1	Read memory
0	1	0	Wrtie memory
0	1	1	Passive

In the maximum mode, the pin 880 is permanently high. The functions and timings of other pins of 8088 are exactly similar to 8086. Due to the difference in the bus structure, the timing diagrams are some what different. The minimum and maximum mode systems are also similar to the respective 8086 systems. The 8088 systems require only one data buffer due to the 8-bit data bus. The minimum and maximum mode systems of 8088 are shown in Figure 2.13(a) and (b) respectively.

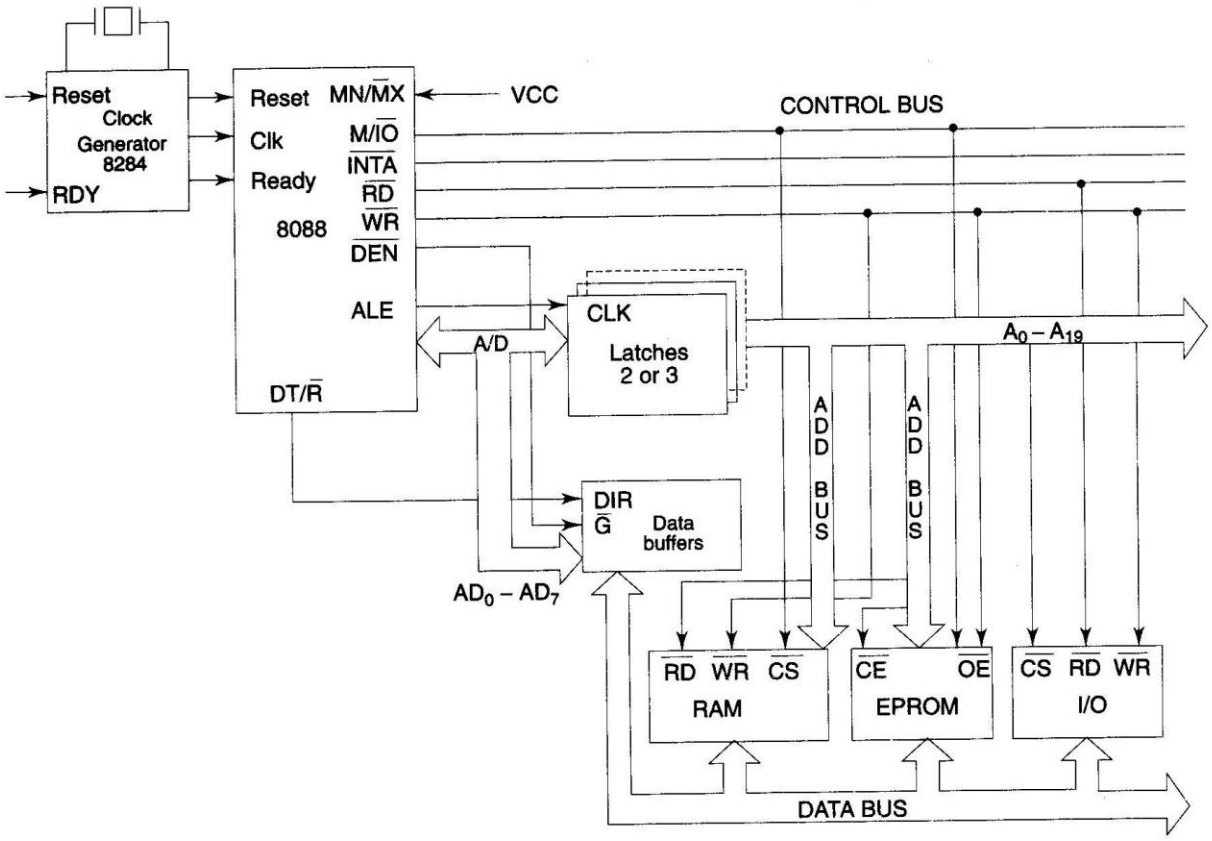

Figure 2.13(a): Minimum Mode 8088 System

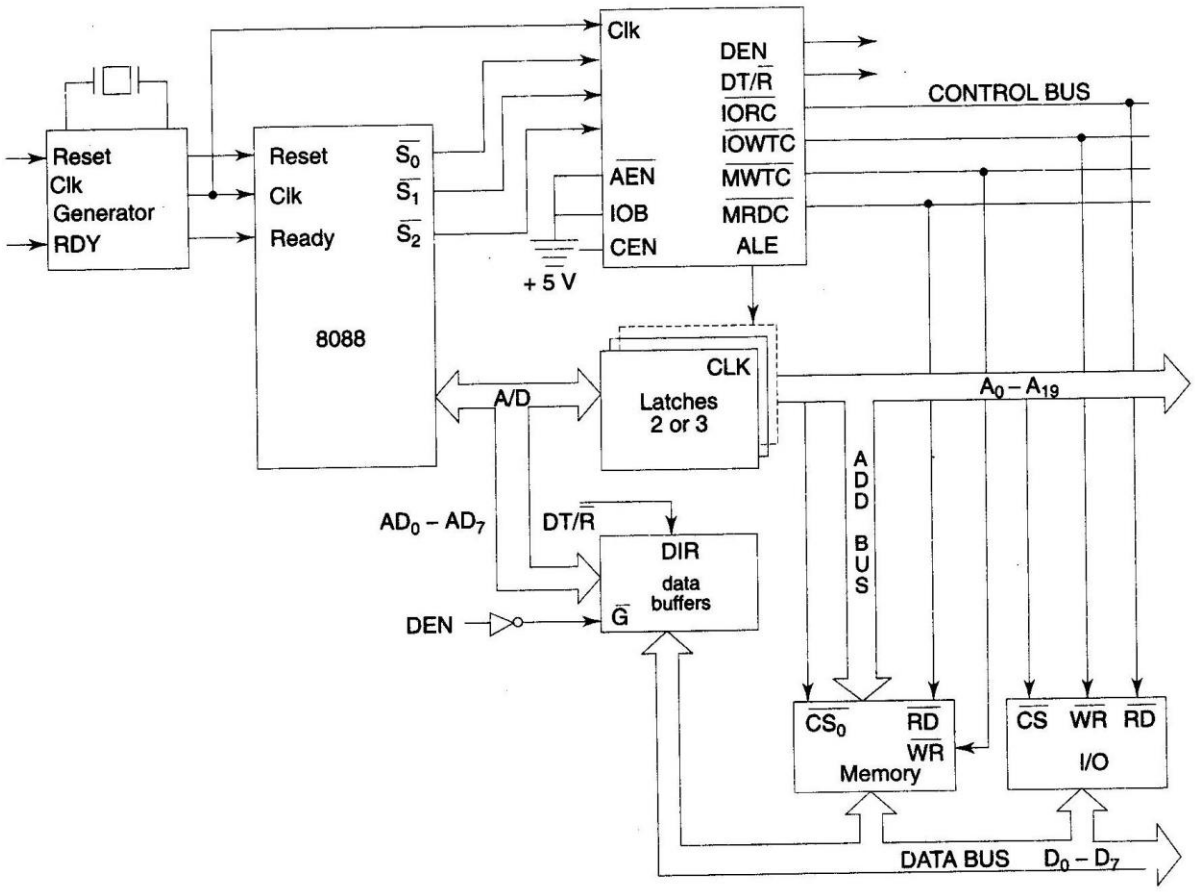

Figure 2.13(b): Maximum Mode 8088 System

General 8088 System Timing Diagram

The 8088 address/data bus is divided in three parts (a) the lower 8 address/data bits, (b) the middle 8 address bits, and (c) the upper 4 address/status bits. The lower 8 lines are time multiplexed for address and data.

The upper 4 lines are time multiplexed for address and status. Each of the bus cycles contains T1, T2, T3, Tw and T4 states. The ALE signal goes high for one clock cycle in T1. The trailing edge of ALE is used to latch the valid addresses available on the multiplexed lines. They remain valid on the bus for the next cycle (T2). The middle 8 address bits are always present on the bus throughout the bus cycle. The lower order address bus is tristated after T2 to change its direction for read data operation. The actual data transfer takes place during T3 and T4. Hence the data lines are valid in T3 or T4. The multiplexed bus is again

tristated to be ready for the next bus cycle. The status lines are valid over the multiplexed address/status bus for T2, T3 and T4 clock cycles.

In case of write cycle, the timing diagram is similar to the read cycle except for the validity of data. In write cycle, the data bits are available on the bus for T2, T3, Tw, and T4. At the end of 14, the bus is tristated. The other signals RD, WR, INTA, DT/R, DEN and READY are similar to the 8086-timing diagram. Figure 2.14 shows the details of read and write bus cycles of 8088.

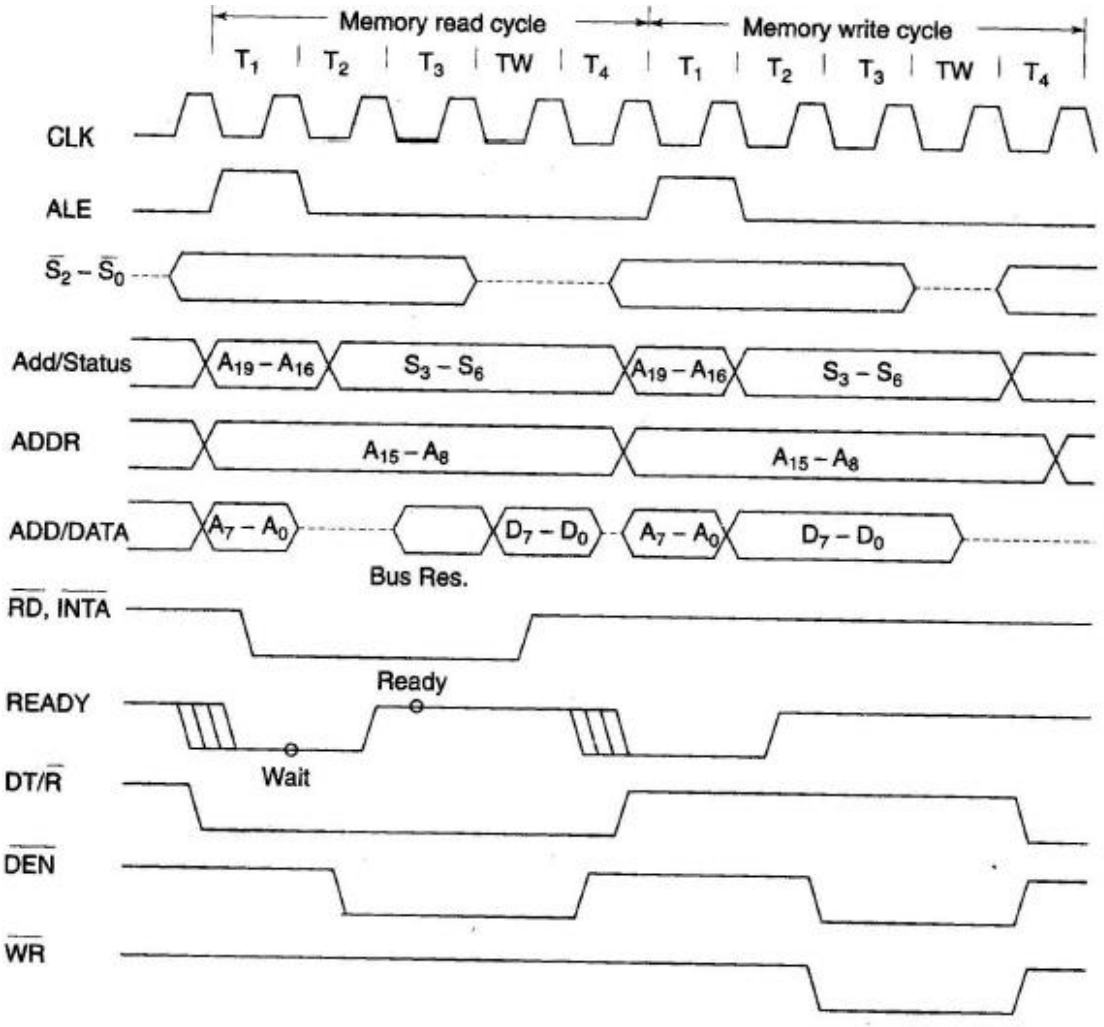

Figure 2.14: Read and Write Cycle Timing Diagram of 8088

Comparison between 8086 and 8088

The 8088, with an 8-bit external data bus, has been designed for internal 16-bit processing capability.Nearly all the internal functions of 8088 are identical to 8086. The 8088 uses the external bus in the same way as 8086, but only 8 bits of external data are accessed at a time.

While fetching or writing the 16-bit data, the task is performed in two consecutive bus cycles. As far as the software is concerned, the chips are identical, except in case of timings. The 8088, thus may take more time for execution of a particular task ascompared to 8086.

All the changes in 8088 over 8086 are directly or indirectly related to the 8-bit, 8085 compatible data and control bus interface.

1. The predecoded code queue length is reduced to 4 bytes in 8088, whereas the 8086 queue contains 6 bytes. This was done to avoid the unnecessary prefetch operations and optimize the use of the bus by BIU while prefetching the instructions.
2. The 8088 bus interface unit will fetch a byte from memory to load the queue each time, if at least 1 byte is free. In case of 8086, at least 2 bytes should be free for the next fetch operation.
3. The overall execution time of the instructions in 8088 is affected by the 8-bit external data bus. All the 16-bit operations now require additional 4 clock cycles. The CPU speed is also limited by the speed of instruction fetches.

The pin assignments of both the CPUs are nearly identical, however, they have the following functional changes.

1. A8-A15 already latched, all time valid address bus.
2. BHE has no meaning as the data bus is of 8-bits only.
3. SS0 provides the S0 status information in minimum mode.
4. IO/M has been inverted to be compatible with 8085 bus structure

Summary

In this chapter, we have presented the internal architecture and signal descriptions of 8086. The functional details of the architecture, like, register set, flags and segmented memory organization are also discussed in significant details. Further, general bus cycle operations have been described with the help of timing diagrams. Then minimal 8086 systems have been presented for the minimum and maximum modes of operation. A software compatible processor-8088 has been discussed in the light of the modifications in it over 8086. To conclude with, the basic bus cycle operations and the timing diagrams of 8088 were discussed along with its comparison with 8086. This chapter is aimed at elaborating the architectural and functional concepts of the processors 8086 and 8088. The instruction set and programming techniques have been discussed in the unit 5.