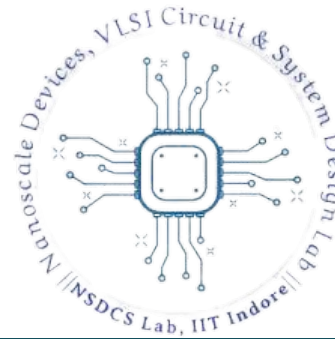


# REPORT ON 4x4 SRAM ARRAY



NSDCS Lab,  
Indian Institute of Technology Indore

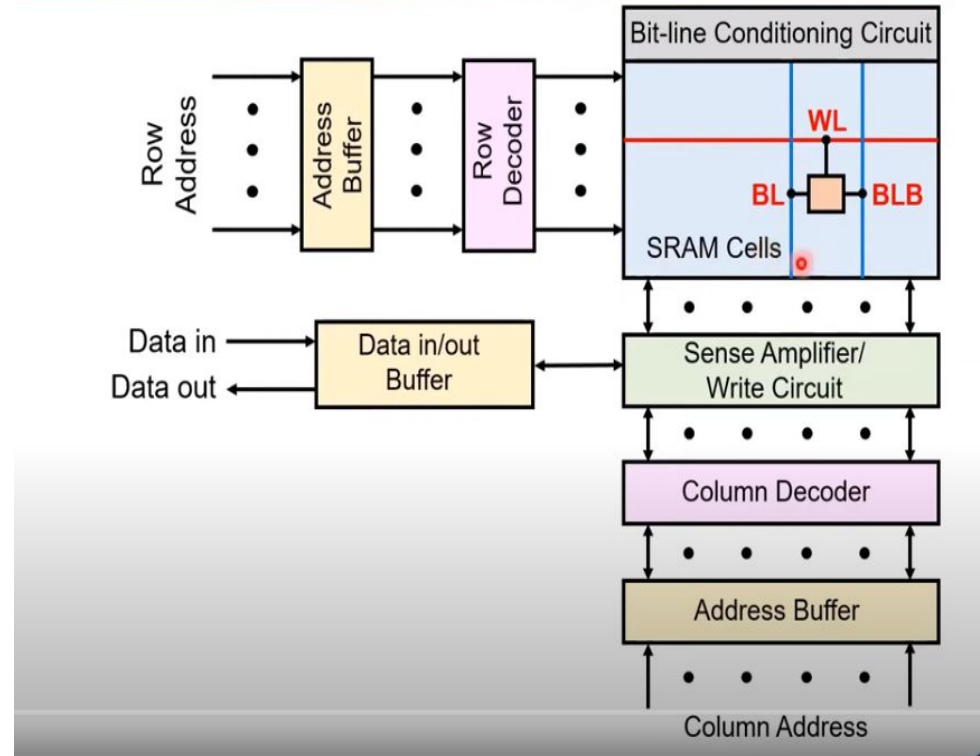
Lab In-Charge: Prof. Santosh Kumar Vishvakarma

Presented by: Akash Pandey  
(2302102035)

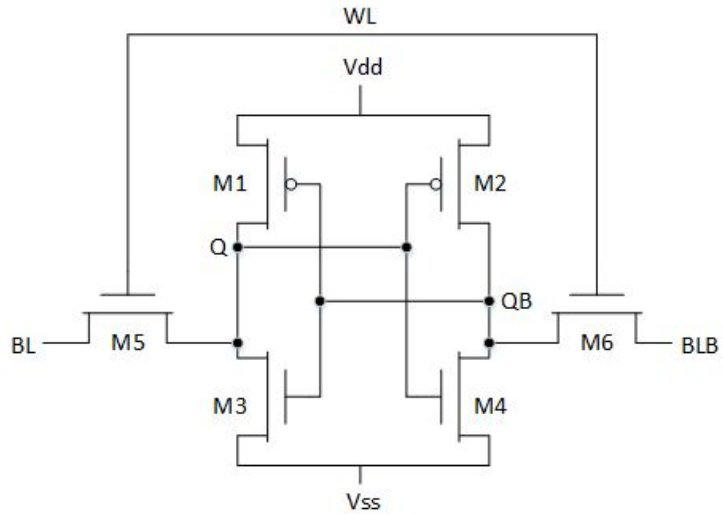
# Report on 4x4 SRAM Array Design

- **Basic Building Blocks:**

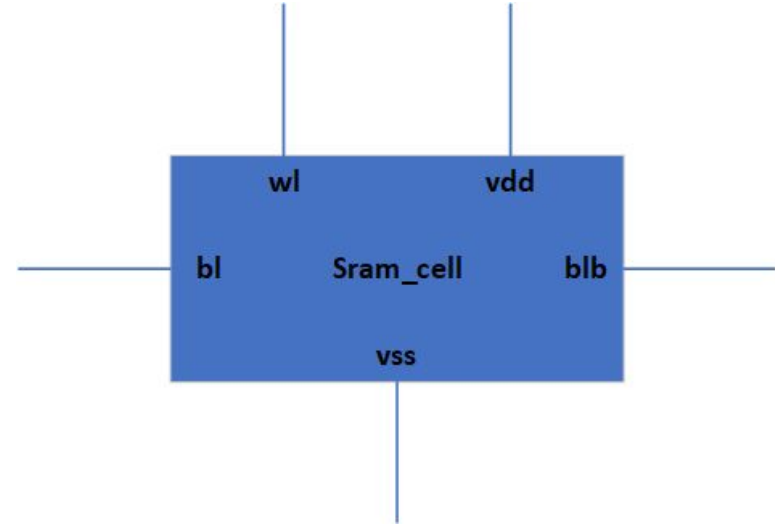
- 6T SRAM cell
- Sense Amplifier
- Write Driver
- Pre-charge circuit
- Row Decoder
- Column mux



Reference: [Lecture 39: SRAM Architecture & Sense Amplifier | MOS VLSI Design](#)  
[Dr. Ambika Prasad Shah | IIT Jammu - YouTube](#)



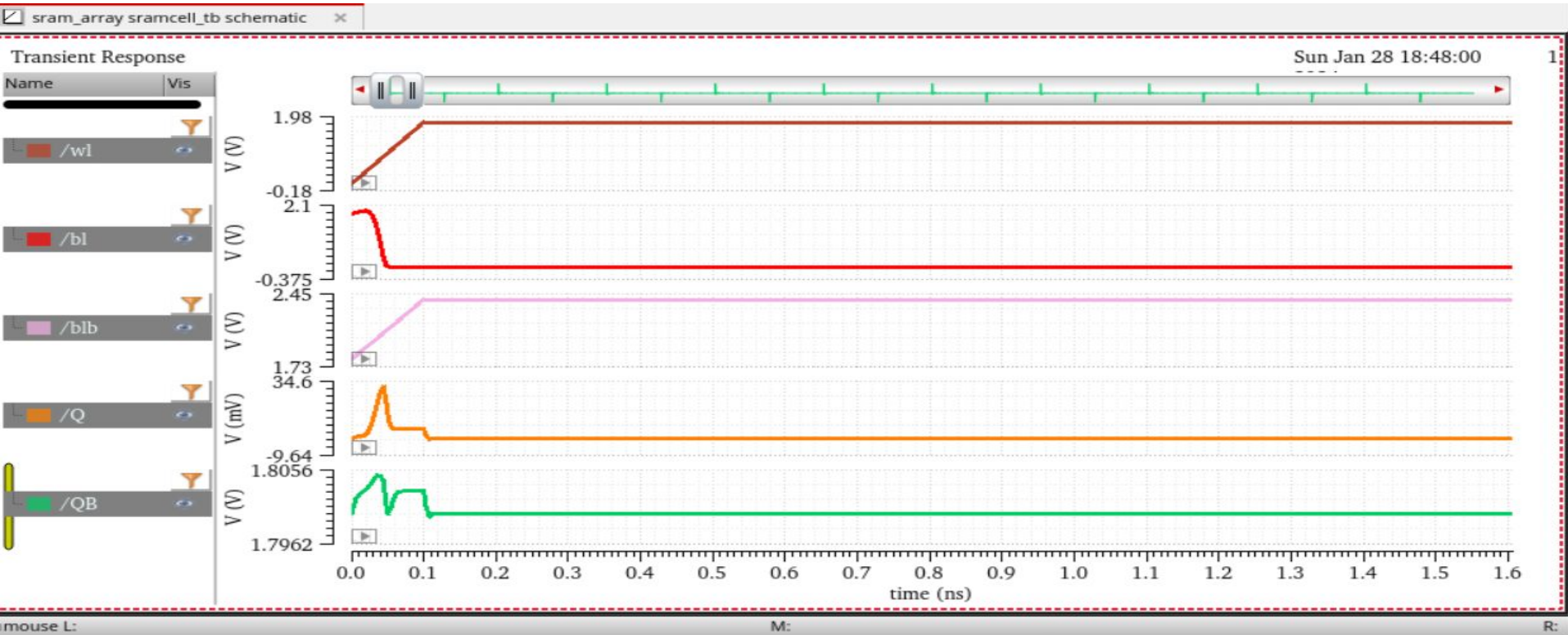
6T SRAM Schematic



6T SRAM Symbol



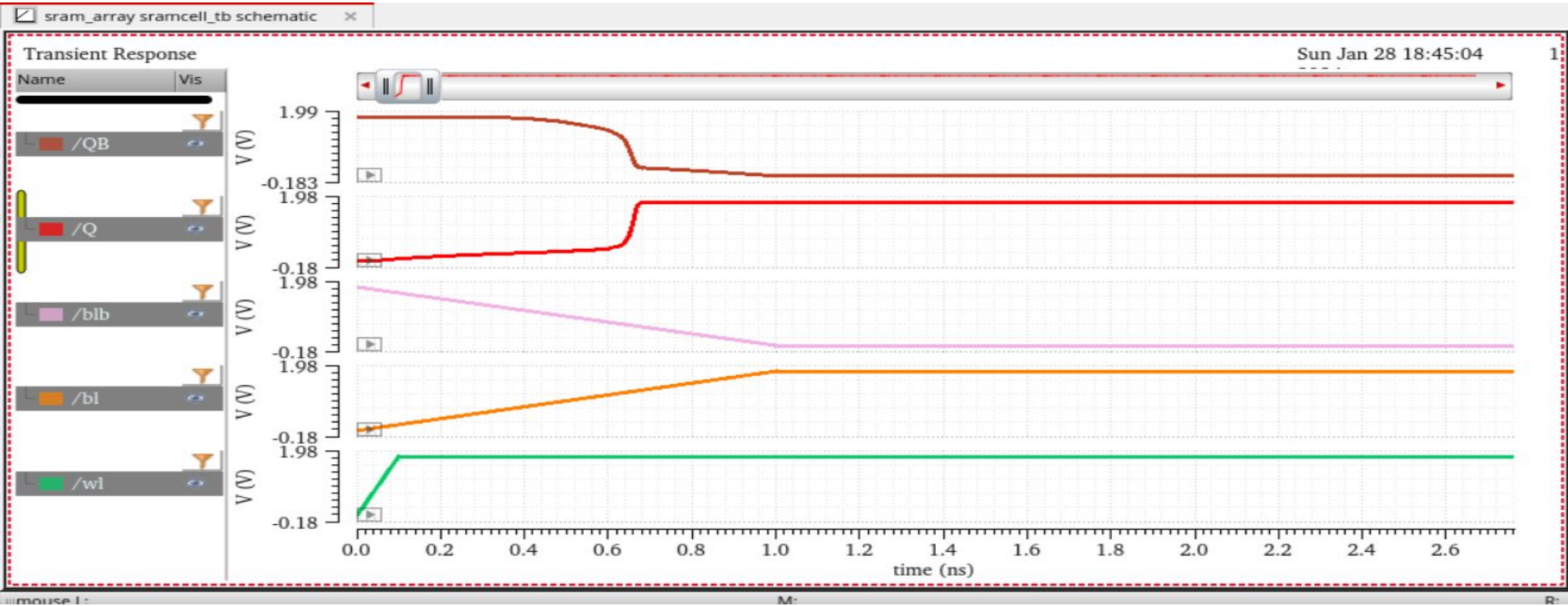
- 1 Bit 6T SRAM Read, Write Operation



Read-0 operation

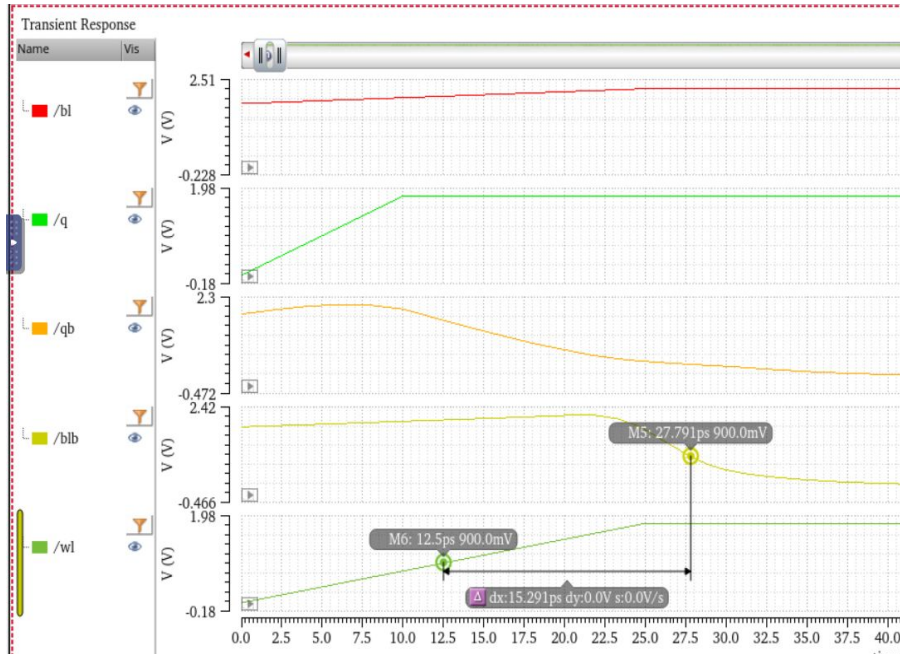


- 1 Bit 6T SRAM Read, Write Operation

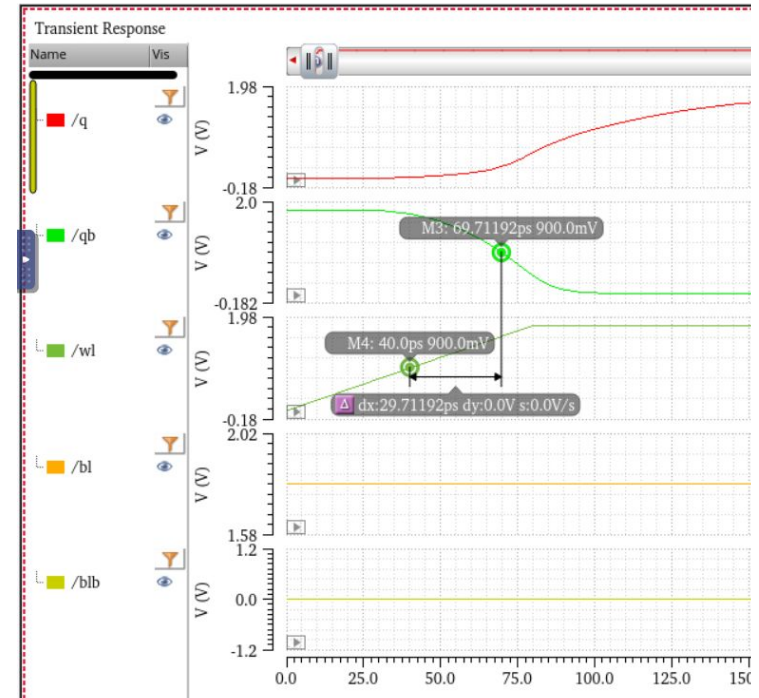


Write-1 operation

- 1 Bit 6T SRAM Read, Write Operation delay

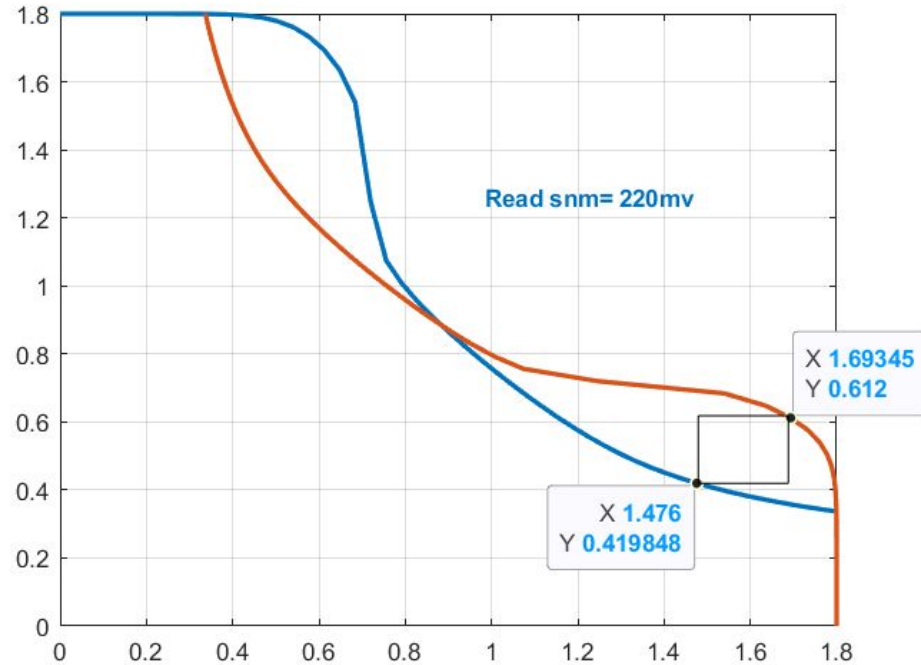


Read Delay



Write Delay

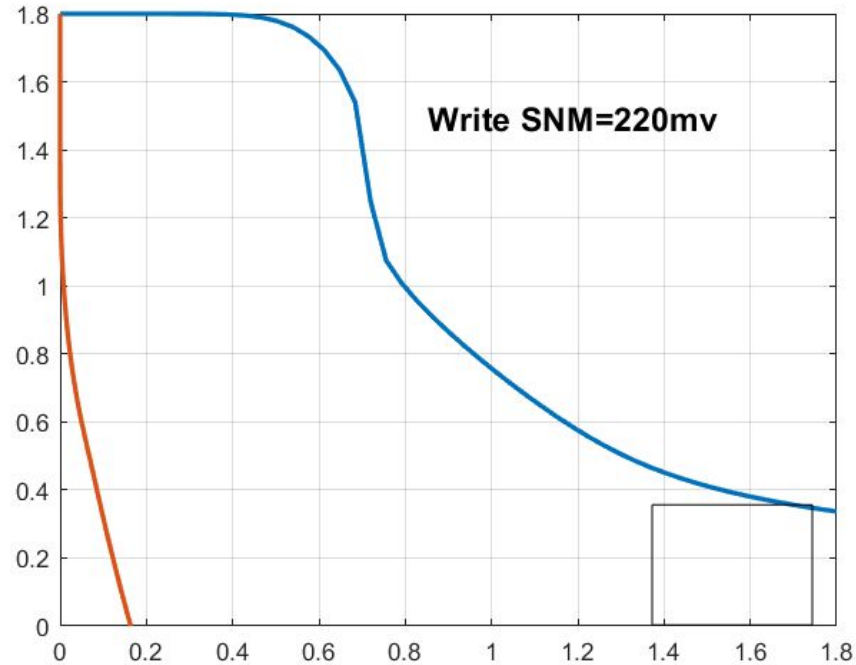
- 1 Bit 6T SRAM Read SNM in Matlab



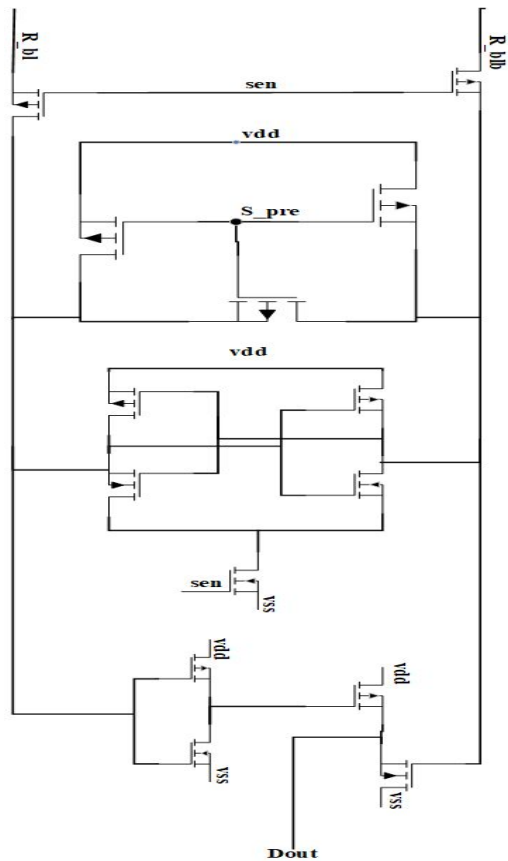
Read SNM



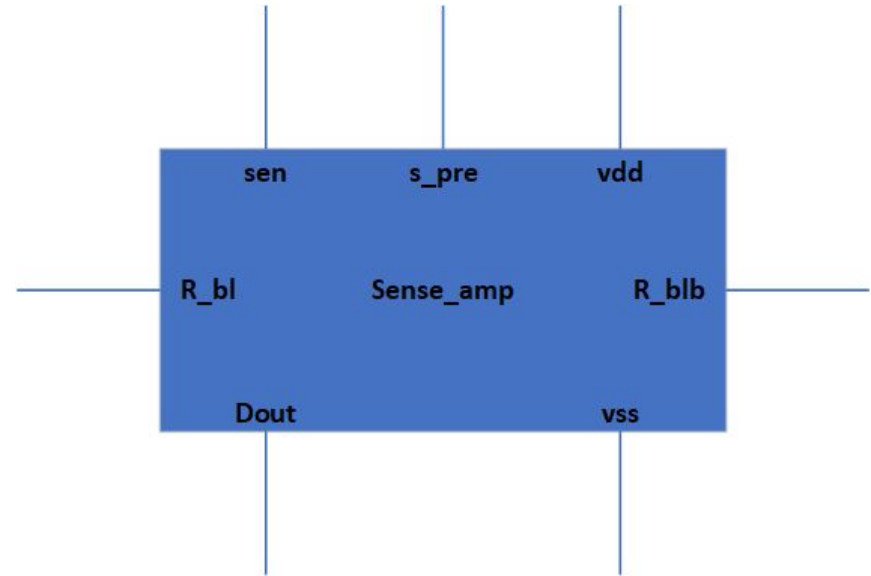
- 1 Bit 6T SRAM Write SNM in Matlab



WriteSNM

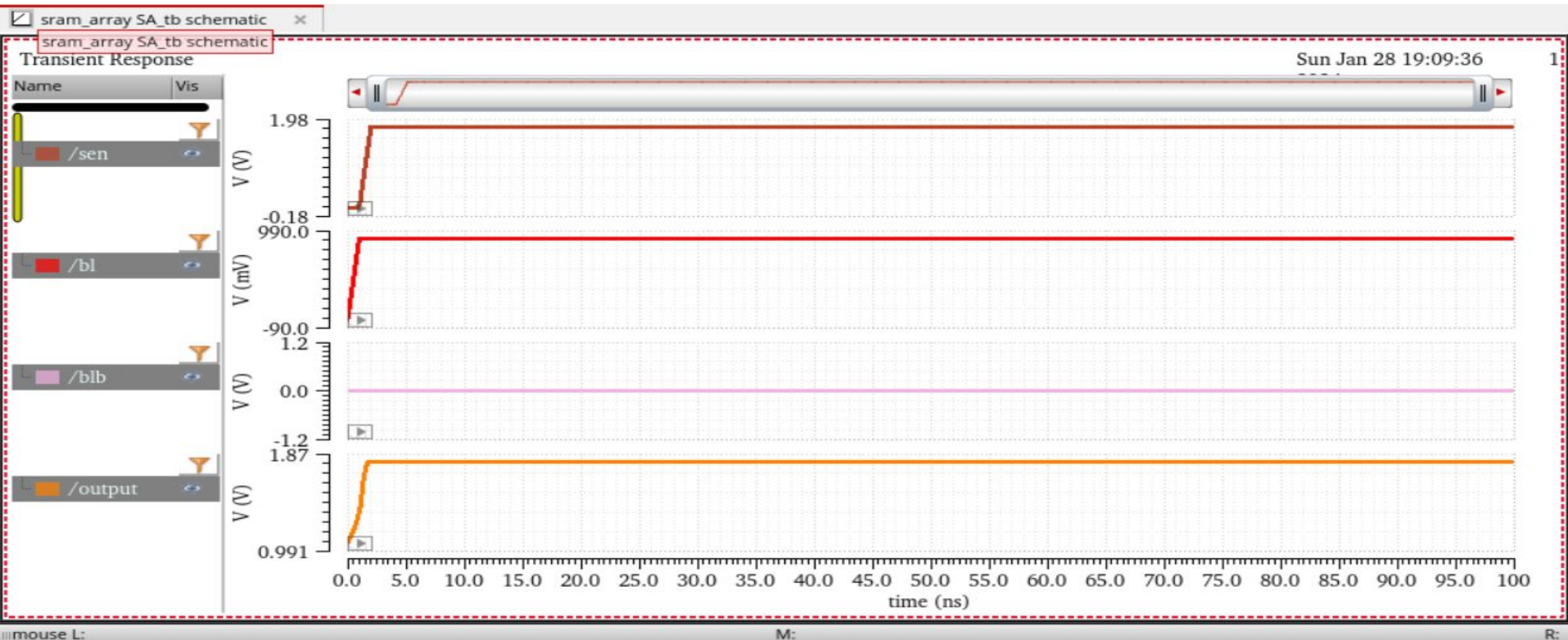


Latch based Sense amplifier Schematic

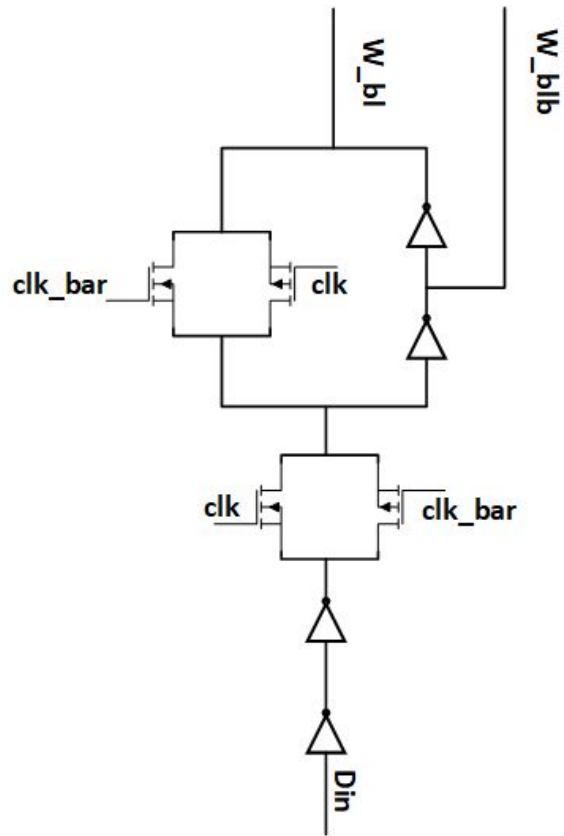


Latch based Sense amplifier symbol

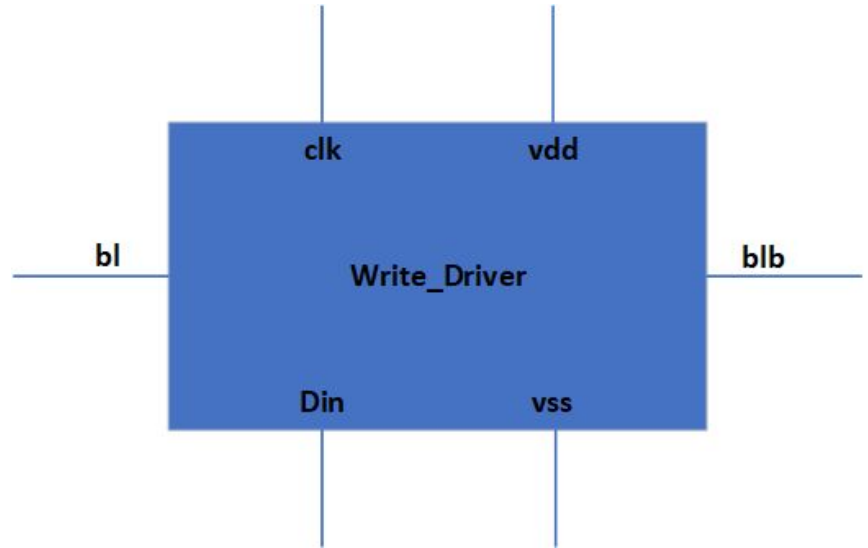
- Sense amplifier Operation



Read-1 operation

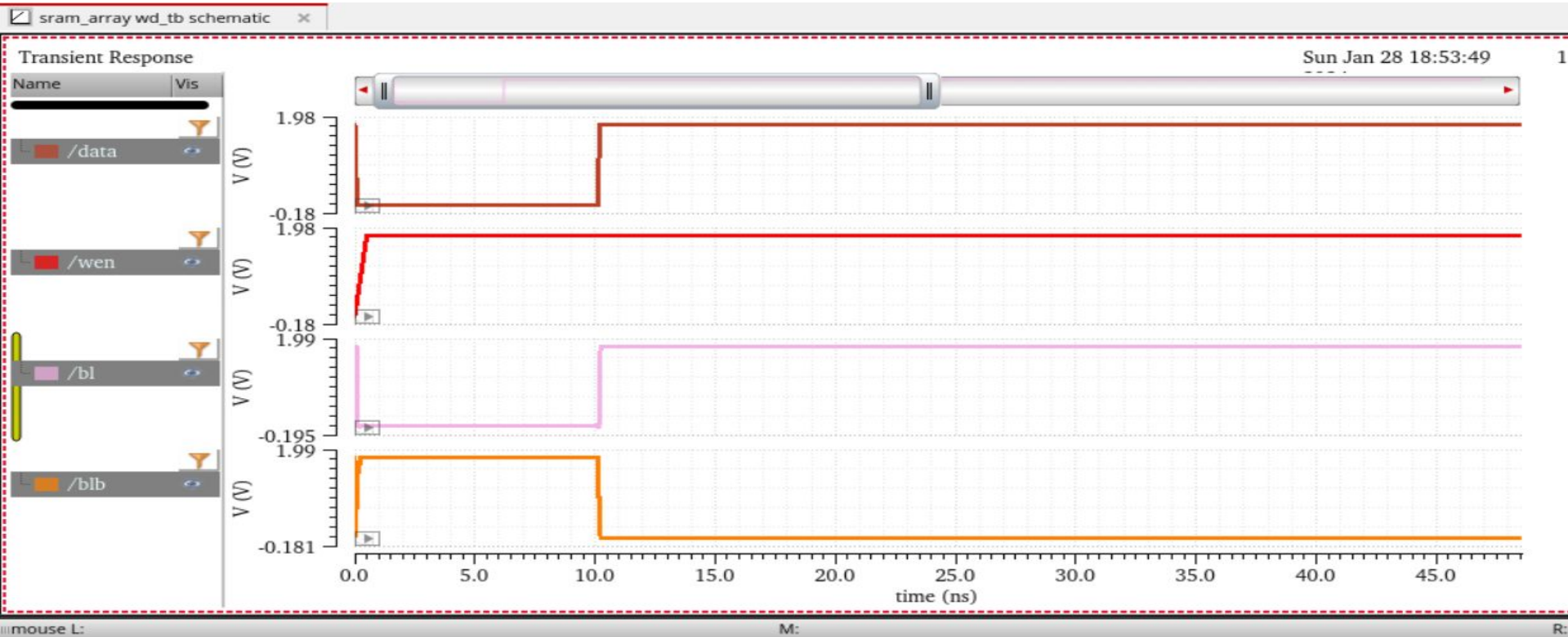


Write Driver schematic



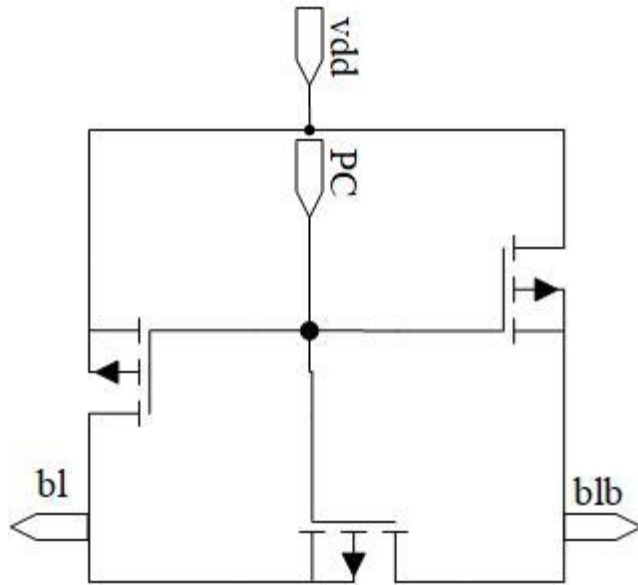
Write Driver symbol

- Write driver Operation

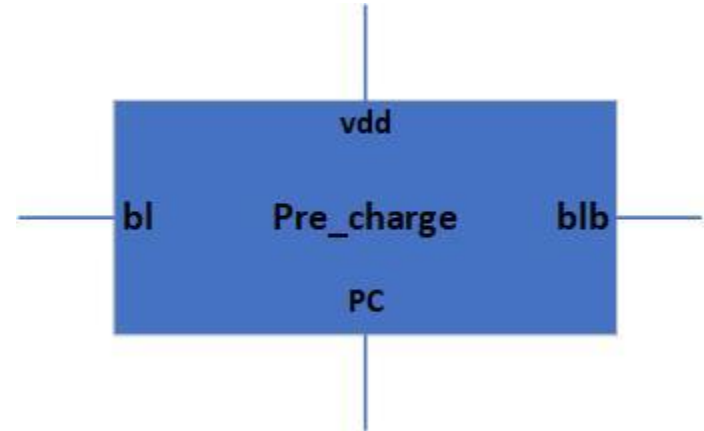


Write operation

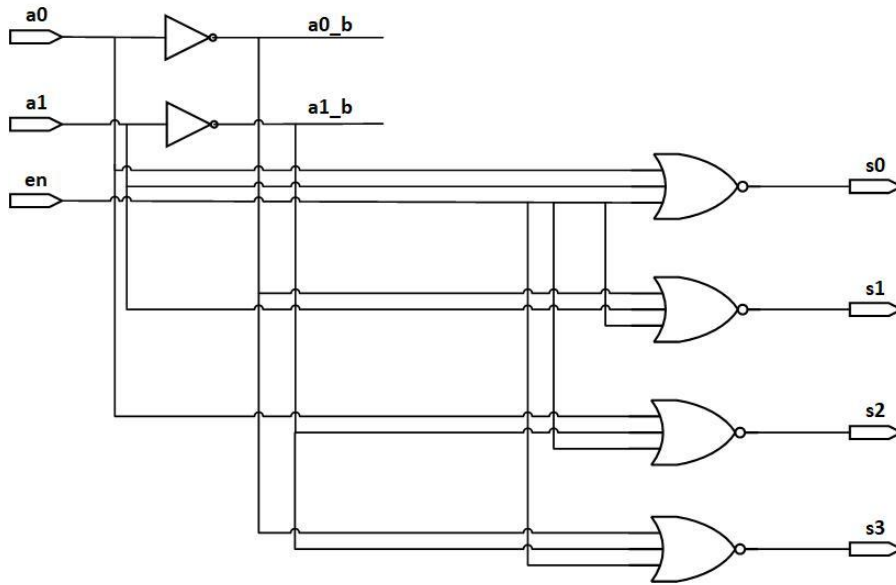




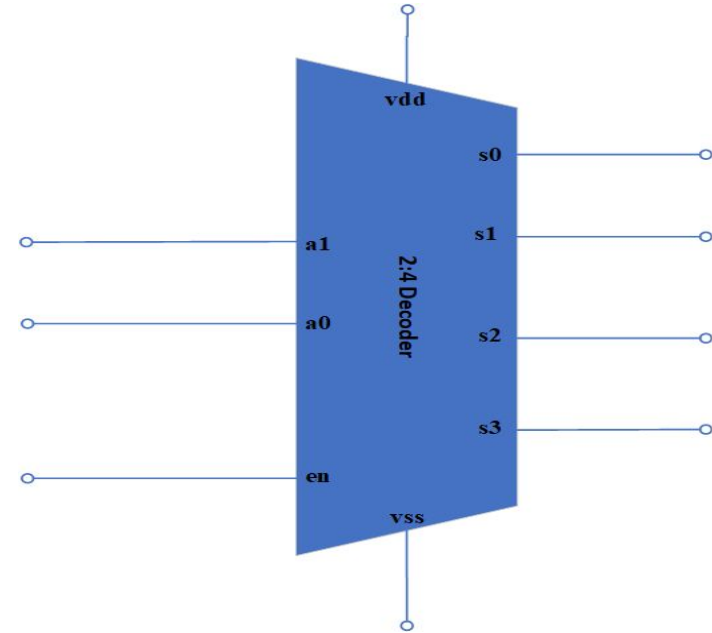
Pre-charge circuit schematic



Pre-charge circuit symbol

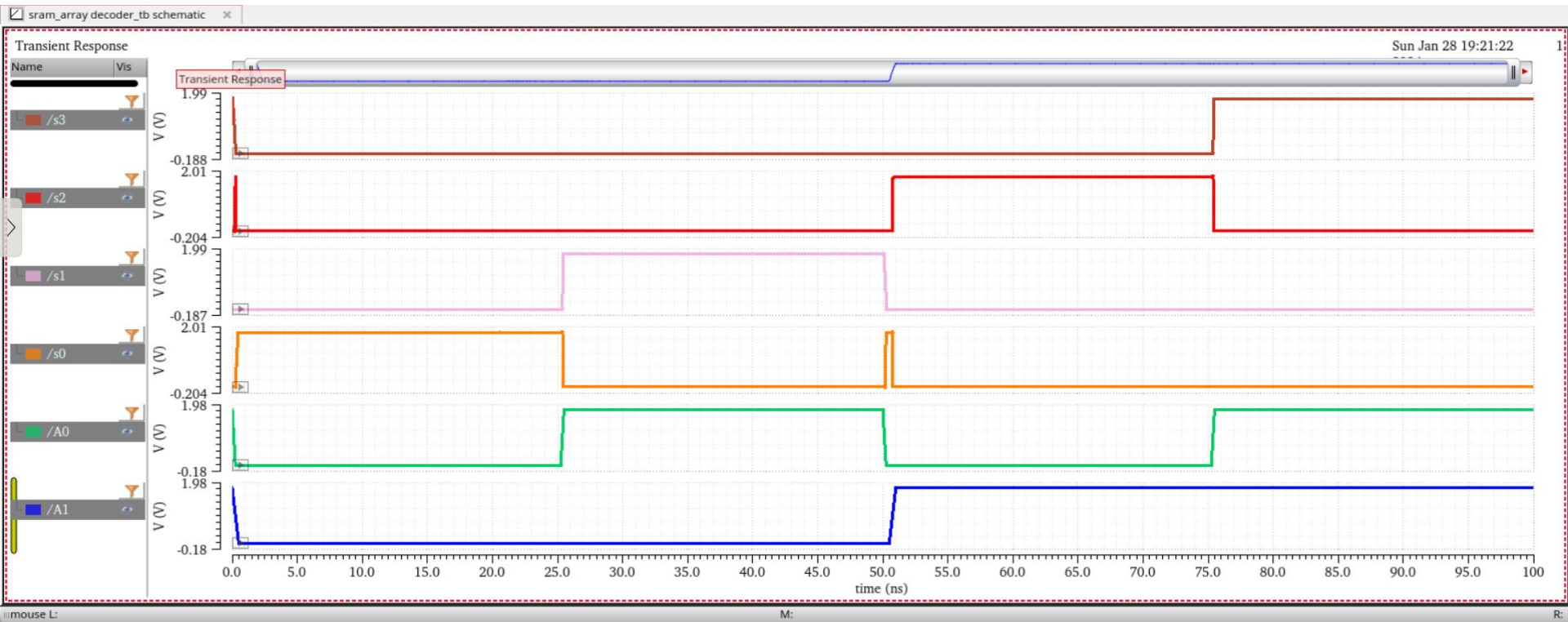


2:4 Decoder schematic

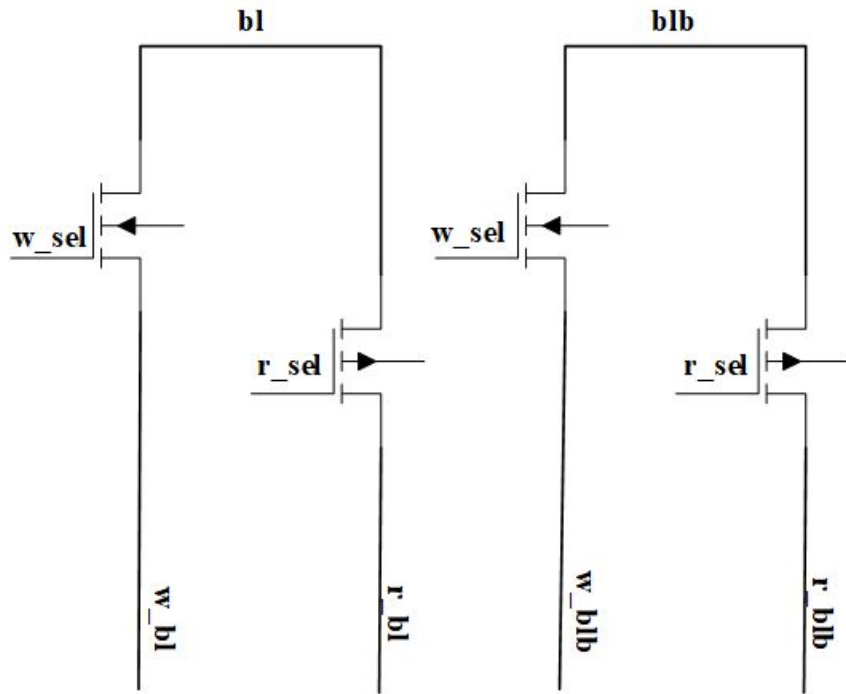


2:4 Decoder symbol

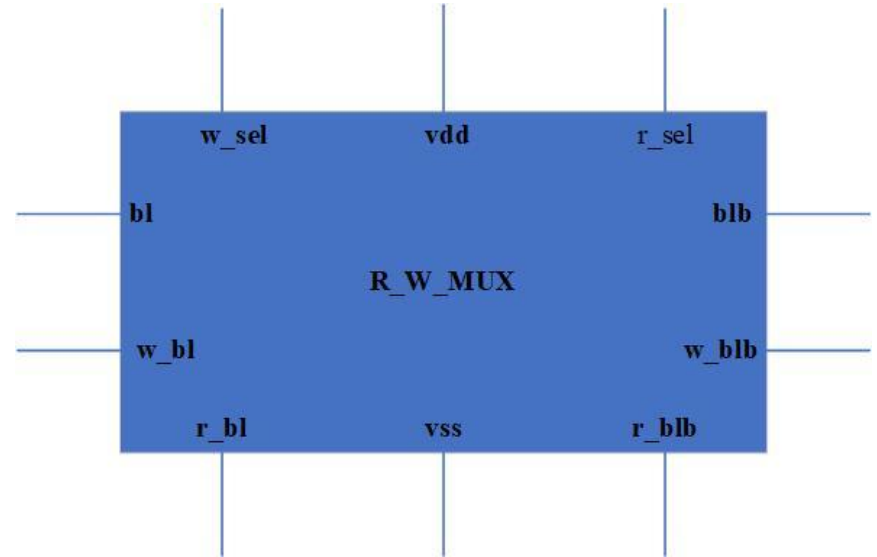
- **2:4 decoder operation**



## 2:4 Decoder operation



Column mux schematic



Column mux symbol



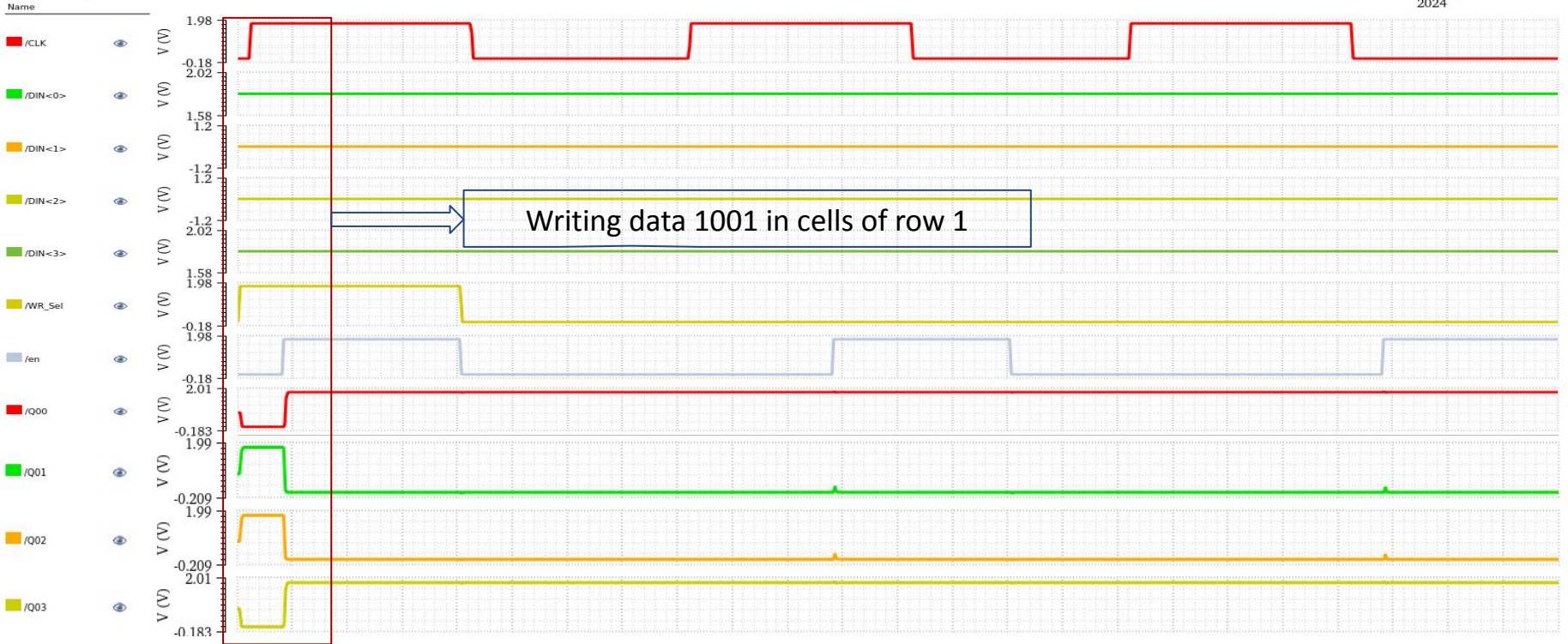


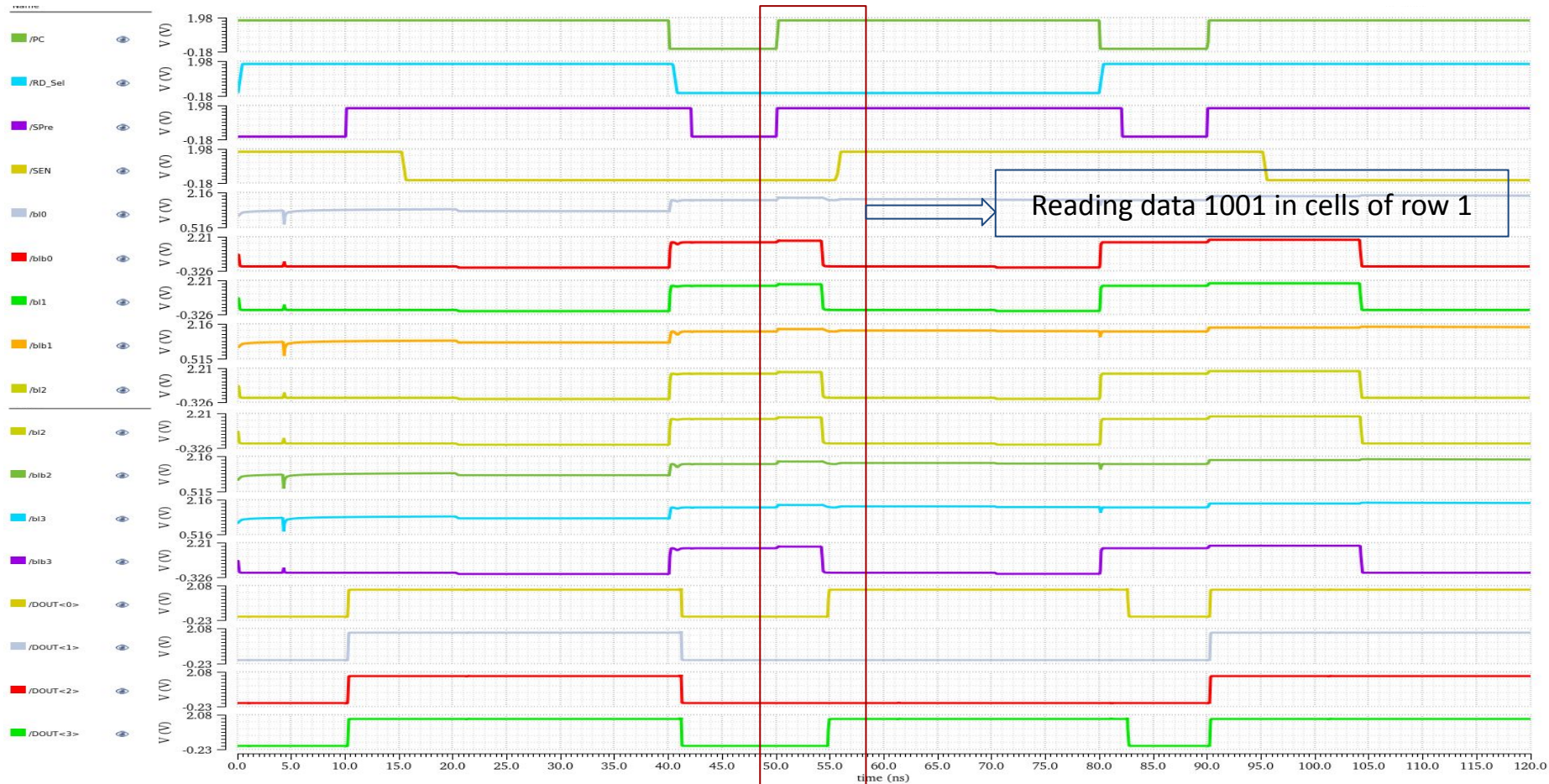
# ● 4x4 Sram array operation

Transient Response

Wed Apr 3 15:28:14  
2024

1





# Thank you