Vrushabh Vakhare

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ASIC PHYSICAL DESIGN ENGINEER

ASIC Design Expertise: Skilled in designing and optimizing integrated circuits, with proficiency in complex chip blocks, floor planning, power optimization, and timing closure. Proven ability to deliver high-quality designs on schedule, ensuring performance and manufacturability.

PROFESSIONAL SKILLS

Operating Systems	Windows/Linux
Scripting Language	TCL, Shell, Perl, Make
Place and Route	Synopsys ICC2, Synopsys Fusion Compiler
Static-Timing Analysis	Synopsys Prime Time
RC Extraction	Synopsys Star-RC
IR Analysis	Ansys Redhawk-SC
Physical Verification	Siemens calibre

PROFESSIONAL EXPERIENCE

Einfochips (An Arrow Company)
ASIC Physical Design Engineer Aug 2021 – Present

- More than 3 years of experience in ASIC Physical Design implementation.
- Skilled in working with TSMC 5nm and 7nm technology nodes.
- Familiar with all phases of Physical Design Implementation such as Floor planning & Memory placement, Power Planning, Placement, Clock Tree Synthesis, Static Timing Analysis, Physical Verification, and Formal Verification.
- Successfully completed tape-out of several designs in 5nm and 7nm technologies.
- Coordinated with the RTL design team and DFT team to comprehend design requirements and ensure that design objectives for Power, Performance, and Area (PPA) were achieved.
- Consistently demonstrated an extraordinary level of dedication, giving 200% effort to ensure project goals were not just met, but exceeded.

Einfochips (An Arrow Company)
ASIC Physical Design Engineer Trainee Jan 2021 – July 2021

- Assisted physical design engineers with floor planning, power planning, and the placement of digital blocks.
- Learned to implement timing, power, and area constraints under the guidance of experienced team members.
- Worked on two training projects on 90nm technology.

PROJECT DETAILS

PROJECT 1	Networking Chip (DPU)
Technology	7 nm TSMC, 16 Metal Layers
Role	Physical Design and Signoff
Design Complexity	Multimillion Instance count, Timing, Congestion, Memory dominant blocks
Max Clock Freq.	~1.2 GHz.
Tools	ICC2 Compiler, Calibre, Synopsys Prime-Time

- Responsible and handling 3 blocks along with channel block activities from Netlist to GDSII with flow enhancement and block closure.
- Responsibilities include.
    - Netlist checks, Floorplan, Placement & optimization, Clock Tree Synthesis, Routing and optimization, extraction, Static Timing Analysis and closure, Formal verification, Physical verification, flow, and script improvements.
    - Checking timing, and congestion and resolved the overflow and timing issue.
    - Running signoff flow and fixing the timing, antenna, EM, IR, DRC, LVS, LEC.
- Challenges faced and resolved:
    - Efficiently managed the placement of 180-200 macros in high-density blocks, strategically positioning memory banks to optimize for signal fan-in and fan-out requirements.
    - Identified and resolved an issue with a high fanout register in the netlist, which was affecting 30% of the logic. This was accomplished based on feedback provided to the RTL design team, resulting in a 15% improvement in overall Timing.
    - Nail Down critical design timing operating at a frequency of 2 GHz within a 7.5-track cell height.

PROJECT 2	Networking Chip (DPU)
Technology	5nm TSMC, 18 Metal Layers
Role	Physical Design and Signoff
Design Complexity	Multimillion Instance count, Timing, Congestion, Memory dominant blocks
Max Clock Freq.	~1.2 GHz.
Tools	Fusion Compiler, Calibre, Synopsys Primetime

- Led physical design and signoff activities for High-Performance Computing ASICs, utilizing cutting-edge 5nm TSMC process technology with 18 metal layers.
- Oversaw the complete design flow for six blocks, from Netlist to GDSII implementation.
- Worked on a high-performance design with a focus on maximizing clock frequency, achieving a maximum frequency of approximately 1.2 GHz.
- Responsibilities included:
    - Netlist checks, Floorplan, Placement & optimization, Clock Tree Synthesis, Routing and optimization, Extraction, Static Timing Analysis and closure, Formal verification, Physical verification, Flow, and script improvements.
    - Implemented rigorous DRC and congestion management strategies to meet stringent design requirements.
    - Collaborated with methodology experts to adapt the 7nm Prime-Time/Star-RC flow to the 5nm.
    - Collaborated closely with a team of 5 designers to meet interface timing, achieving this goal 20% earlier than usual in the Place and Route (PNR) phase.

EDUCATION & CERTIFICATIONS

Bachelor's in engineering - Power Electronics- Vishwakarma Government Engineering College
Diploma in Engineering - Power Electronics - Dr. S & S.S. Ghandhy College
VLSI Training - Physical Design - eInfochips Training & Research Academy Ltd

APPRECIATIONS

Awarded Core Value Award for Continues learning.
Awarded Best Team of the Year for collaboration and contribution to project tap-out.

PUBLICATIONS

- "Power Analysis in 7nm Technology Node", Published on Design & Reuse, 2023