**Computer Architecture (2)**

**Rubric - Project Final Submission (Functionality)**

Please fill in the 2nd column of the following table:

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| --- | --- |
| Project title | FLOATING POINT ARITHMETIC PIPELINE SYSTEM |
| Group Members | Group Number {1}  >>Mariam Mourad 20210798  >>Taima Darwish 20200415 |
| Total number of Pipeline Stages | 6 stages |
| Correctness of the design checked (compared to a software implementation)? Yes/No | Its giving correct results  (tested manually) |
| Design is implemented in Verilog? Fully/Partially | Fully |
| Simulations show:  1-only partial results of stages  2- only final results  3- Both partial and final results | Both partial and final results |
| Simulations show cycle by cycle results? Yes/No | Stage by stage results |
| Number of simulated clock cycles? | Some test benches included up to 5 results and some have 2 results |
| Design is compared (analytically/experimentally) with single-cycle implementation? Yes/No | Non-pipelined execution=6\*Tn=36\*Tp  Pipelined execution=(6+(6-1))\* Tp=11\*Tp  SpeedUp = (16∗Tp) /(7∗Tp) = 36/11 ns  = 3.27273 ns |