Princess Sumaya University for Technology
King Abdullah II Faculty of Engineering
Electrical Engineering Department

Princess Sumaya جامعـــة
University الأميـرة سميّـة
for Technology للتكنولوجيا

MICROPROCESSORS 22344

MIDTERM HARDWARE PROJECT

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1/15/2024

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Introduction

Objectives

Design an 8088-microprocessor based system to transmit and receive data. The data received should be displayed on 16x2 LCD display. The system includes a 4x4 keypad, through which, the user can enter numeric values to be sent serially.

Theory

components

1. 8086 - 16-BIT MICROPROCESSOR

   8086 Microprocessor is an enhanced version of 8085 Microprocessor. It is a 16-bit Microprocessor having 20 address lines and 16 data lines that provides up to 1MB storage. In the digital computer's stored-program concept, microprocessors serve as the CPU. Its responsibility is to create all system timing signals and to synchronize data transfers between memory, I/O, and itself.

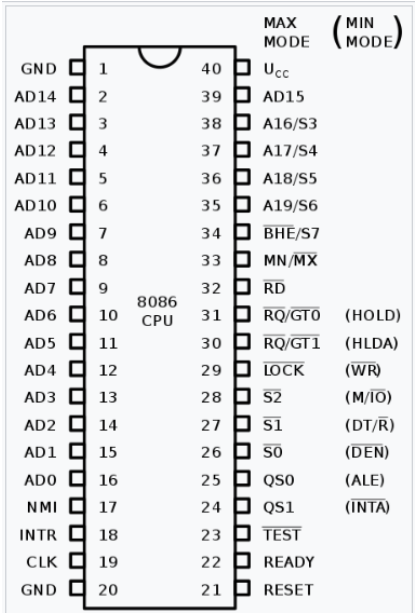


Figure 1: 8086 Pin Configuration

2. 8251A – USART

8251 universal synchronous asynchronous receiver transmitter (USART) acts as a mediator between microprocessor and peripheral to transmit serial data into parallel form and vice versa.

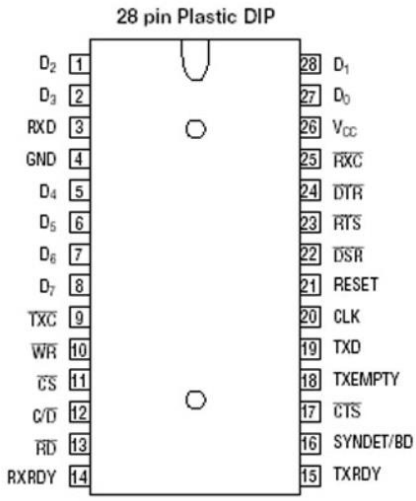


Figure 2:8251 Pin Configuration

3. 8255A – Programmable Peripheral Interface

The 8255A is a common parallel, programmable input-output device. It can transfer data under a variety of conditions, ranging from basic input-output to interrupt input-output.

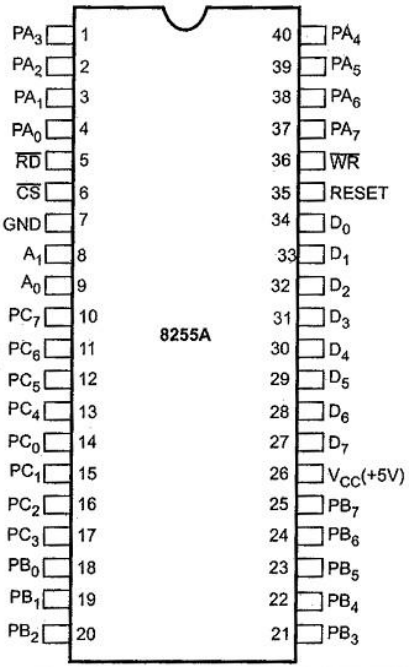


Figure 3: 8255 Pin Configuration

- The 8255 can operate in 3 I/O modes, we used mode 0:
- Mode 0:

  -Ports A, B, and C can be individually programmed as input or output ports

  -Port C is divided into two 4-bit ports which are independent from each other

  - in our project we programmed it as:

  A[0..3] Input from keypad.

  B[0..7] output to LCD.

  C[0..3] output from 8255 to keypad.

4. Octal D- Latch (transceiver)

It's used to separate data from the addresses.

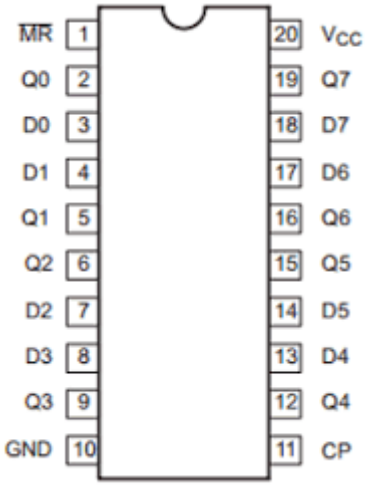


Figure 3:74ALS245 Pin configuration

5. 74HC373 Octal D-type transparent latch

It's used to separate addresses from the data.

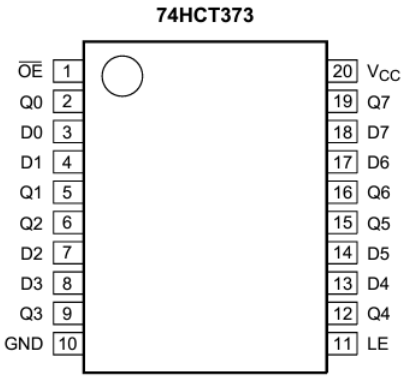


Figure 4:74HC373 Pin Configuration 1

6. LM016L LCD

Electronic display module that uses liquid crystal to produce a visible image.
we will be using it to display the pressed key.

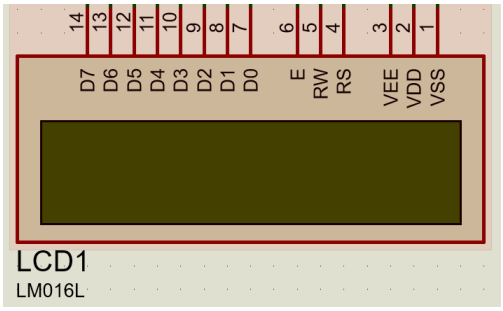
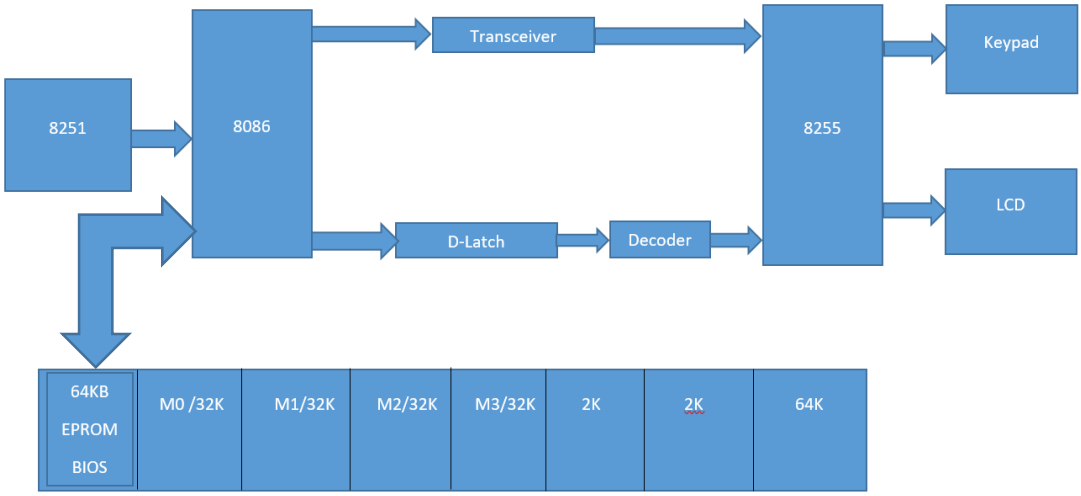


Figure 5: 16x2 liquid crystal display

Block Diagram



Implementation

Programming the 8255

Decoding circuit of 8255

Giving the 8255 address of (0x6000H).
A0 and A1 will pick which port are we communicating with

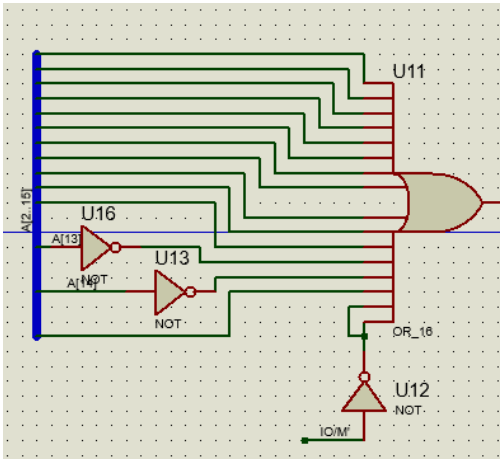


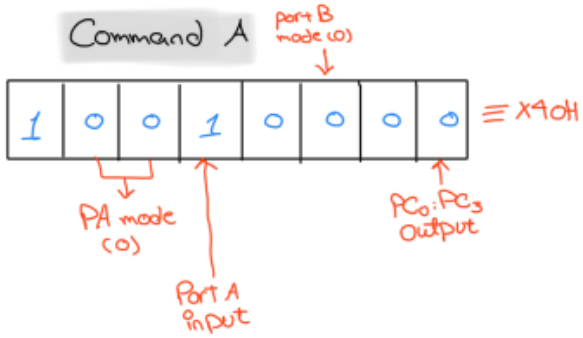
Figure 6:Decoding circuit of 8255

Port	A[15…2]	A1 A0	Address
PORT A	0110 0000 00	00	0x6000H
PORT B	0110 0000 00	01	0x6001H
PORT C	0110 0000 00	10	0x6002H
CMND	0110 0000 00	11	0x6003H

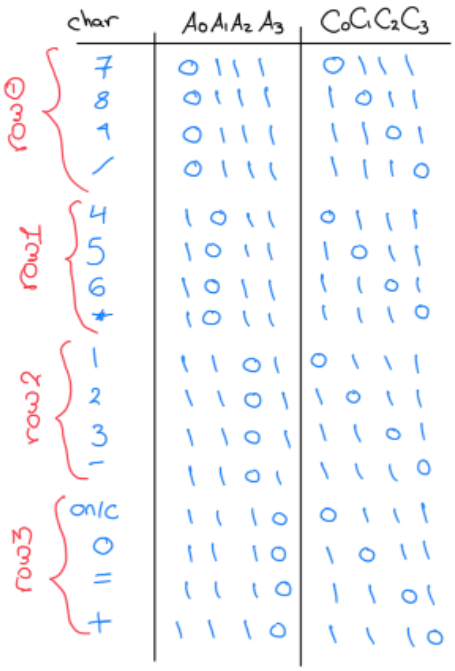
We used MODE (0) to meet the desired functionality of the chip:

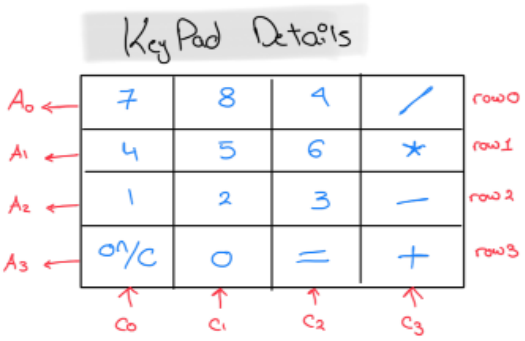
- **Ports A** as an input port (input from keypad t 8255)
- **Port B** as an output (from 8255 to LCD)
- Lower part of **Port C[0..3]** as an output (to send the walking Zero)

Command A = 0x90H



Keypad Decoding:





Programming the 8251

Decoding circuit of 8251

Giving the 8251 address of (0x5000H).
A0 will pick which port (data / command) we are communicating with

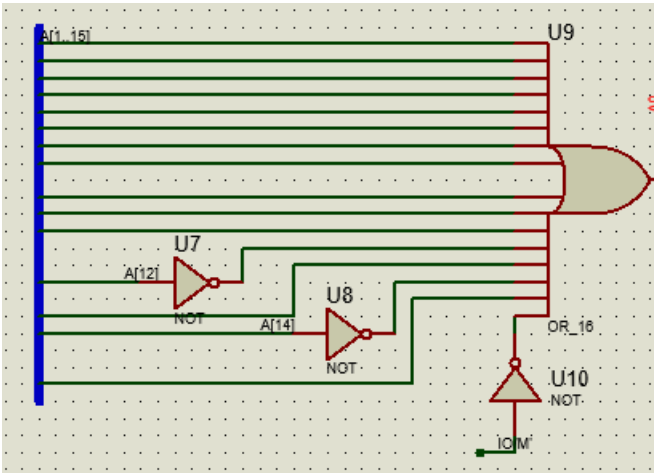


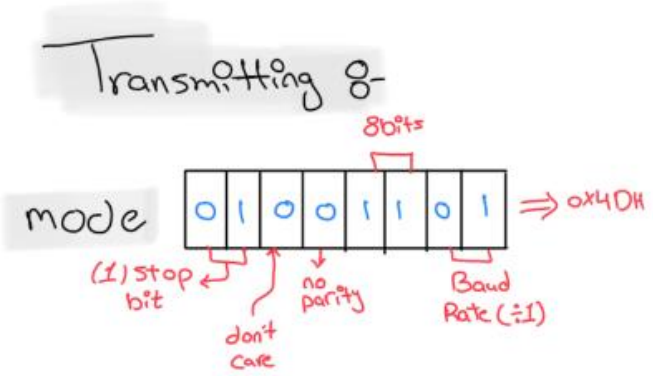
Figure 7:Decoding circuit of 8251

Port	A[15…1]	A0	Address
dataPort	0101 0000 000	0	0x5000H
CMND	0101 0000 000	1	0x5001H

Programming 8251 is split into two parts, first for setting it up for Transmitting the other one is for Receiving

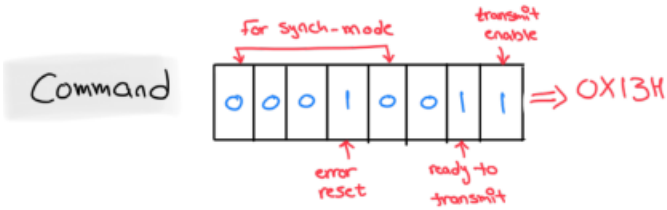
Mode register = 0x4DH , such that

Boud rate: clk divided by (1)
char length: 8 bits
parity is disabled , parity type (don't care)
and finally (1) stop bit.
These things must be agreed on from both sides before transmitting/receiving data



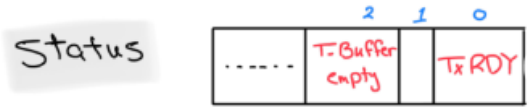
Command register = 0x13H , such that

TxE is enabled , DTR IS READY
RxE is disabled , SBRK IS DON'T CARE
ER IS 1 , RTS IS disabled
IR MUST BE ZERO and EH IS DON'T CARE



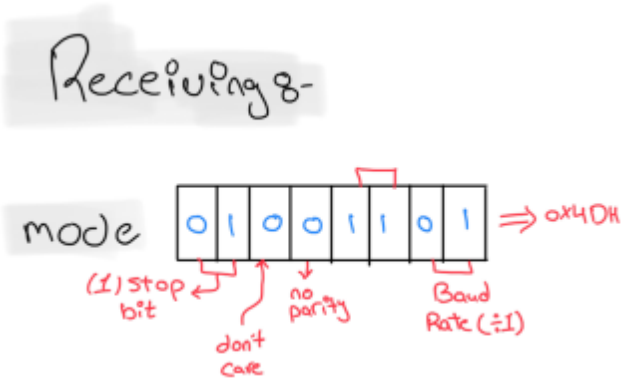
Status register:

We will be checking bit[0] and bit[1] before Transmitting To see if ready to transmit and buffer is empty to accept data



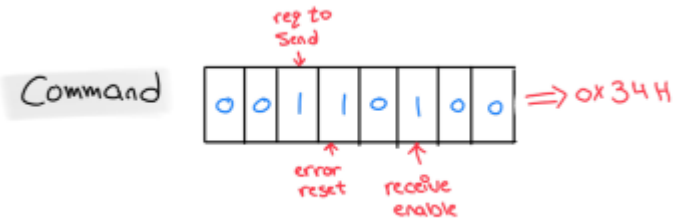
Mode register = 0x4DH, such that

Baud rate: clk divided by (1)
char length: 8 bits
parity is disabled, parity type (don't care)
and finally (1) stop bit.
These things must be agreed on from both sides before transmitting/receiving data



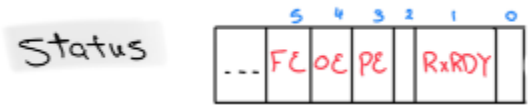
Command register = 0x34H , such that

TxE is disabled, DTR disabled
RxE is enabled, SBRK IS DON'T CARE
ER IS 1, RTS IS READY
IR MUST BE ZERO and EH IS DON'T CARE



Status register:

We will be checking bit[1] to see if ready to receive
Bit[3], bit[4] and bit[5] to detect errors

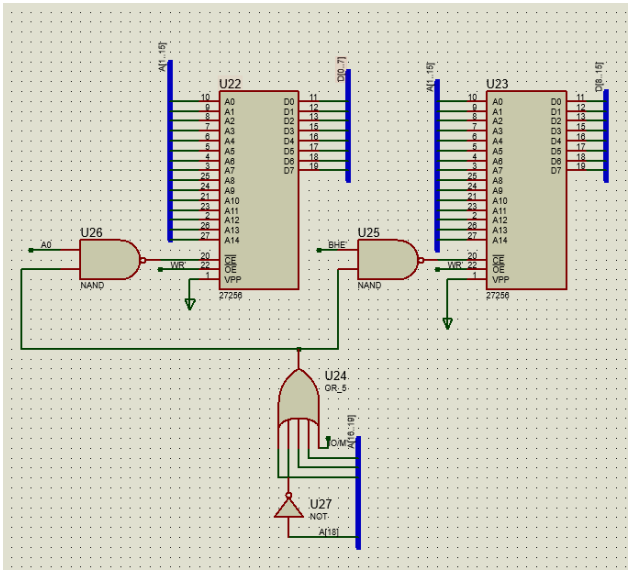


MEMORY:

ROM(BIOS) 64KB

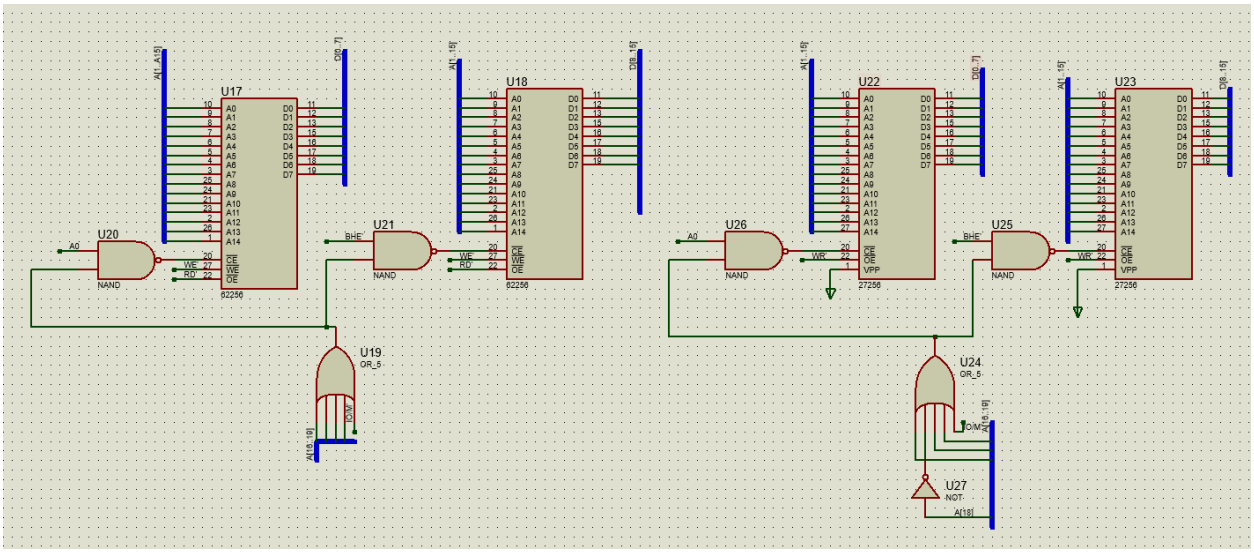
Start address: 40000H

End address: 4FFFFH

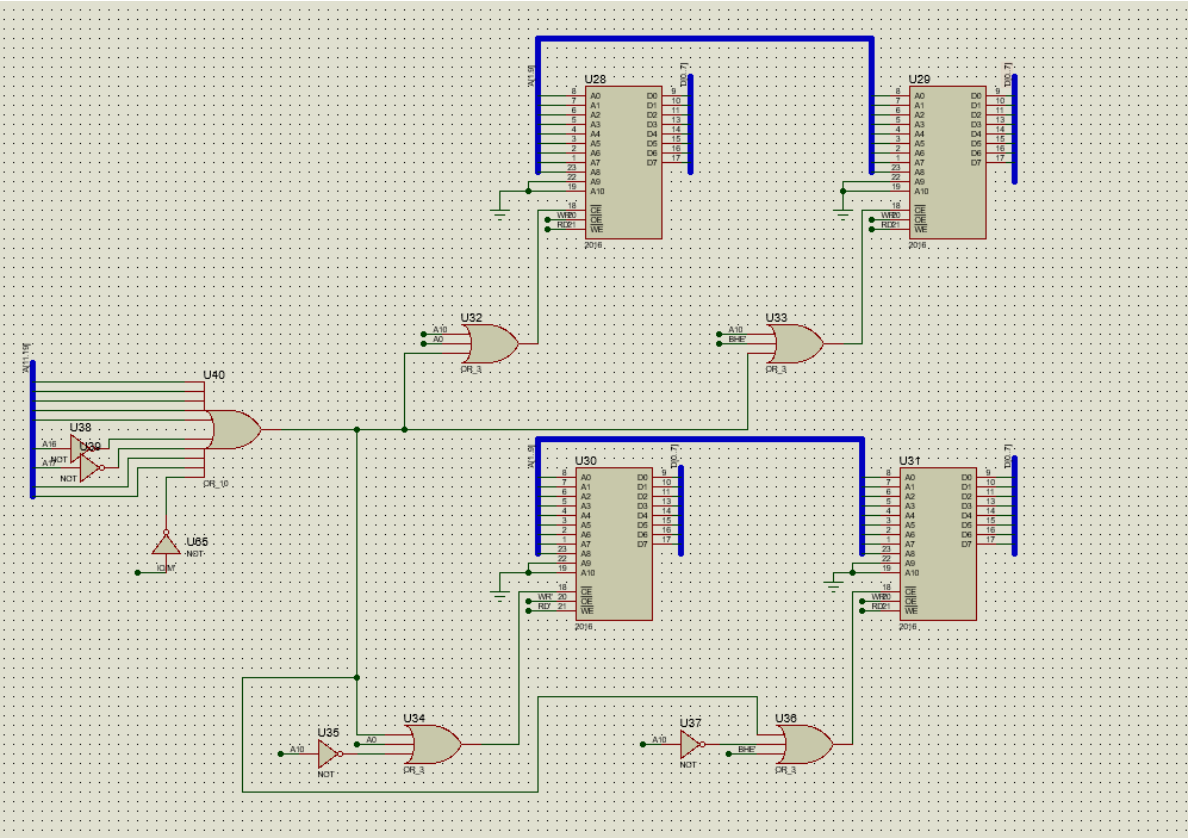


- 64K RAM

  Start address: 00000H
  End address: 0FFFFH



- 2k memory:
  Start address: 30000H
  End address:307FFH
  Divided into:
  1K MEMORY (for reading): [30000H:303FFH]
  1K MEMORY (for writing): [30400H:307FFH]



- 128KB RAM

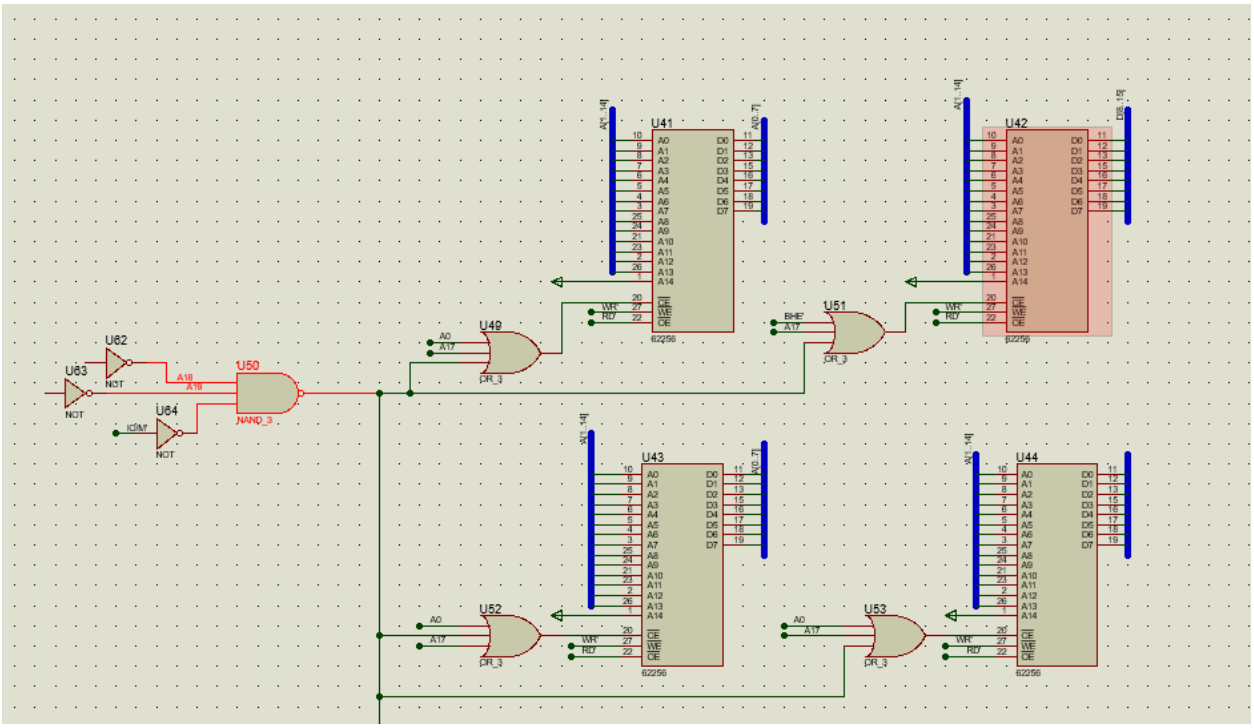
  Divided into:

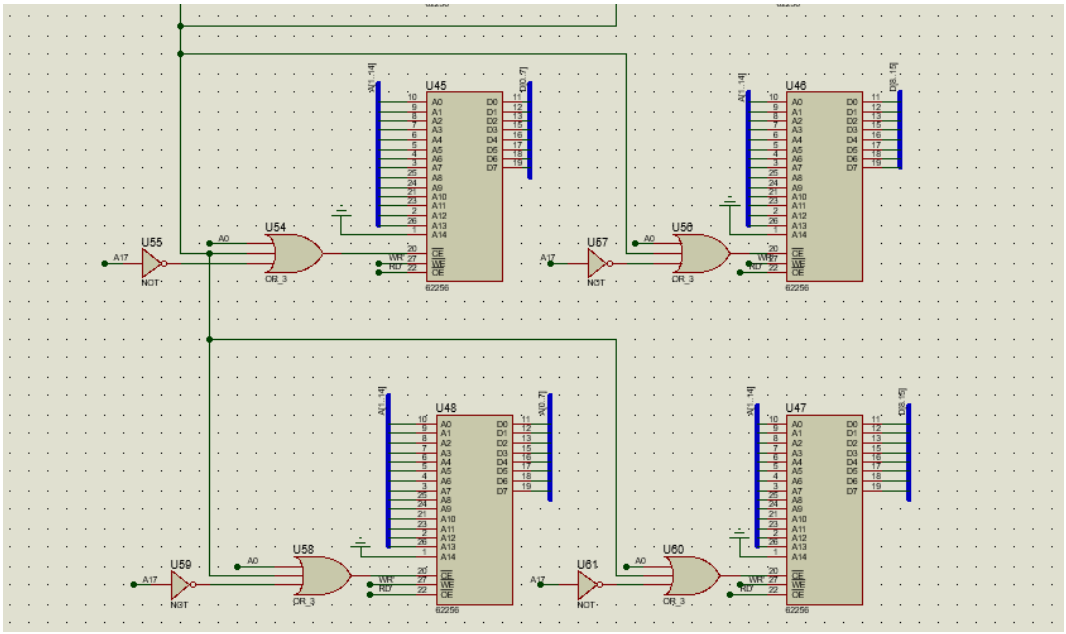
  M0: [10000H:17FFFH]

  M1: [18000H:1FFFFH]

  M2: [20000H:27FFFH]

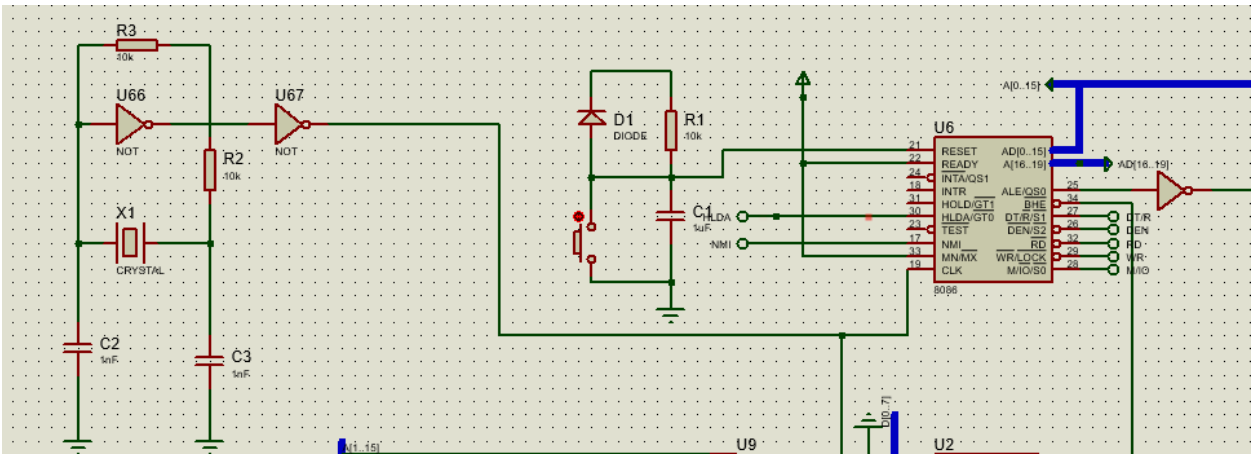
  M3: [28000H:2FFFFH]



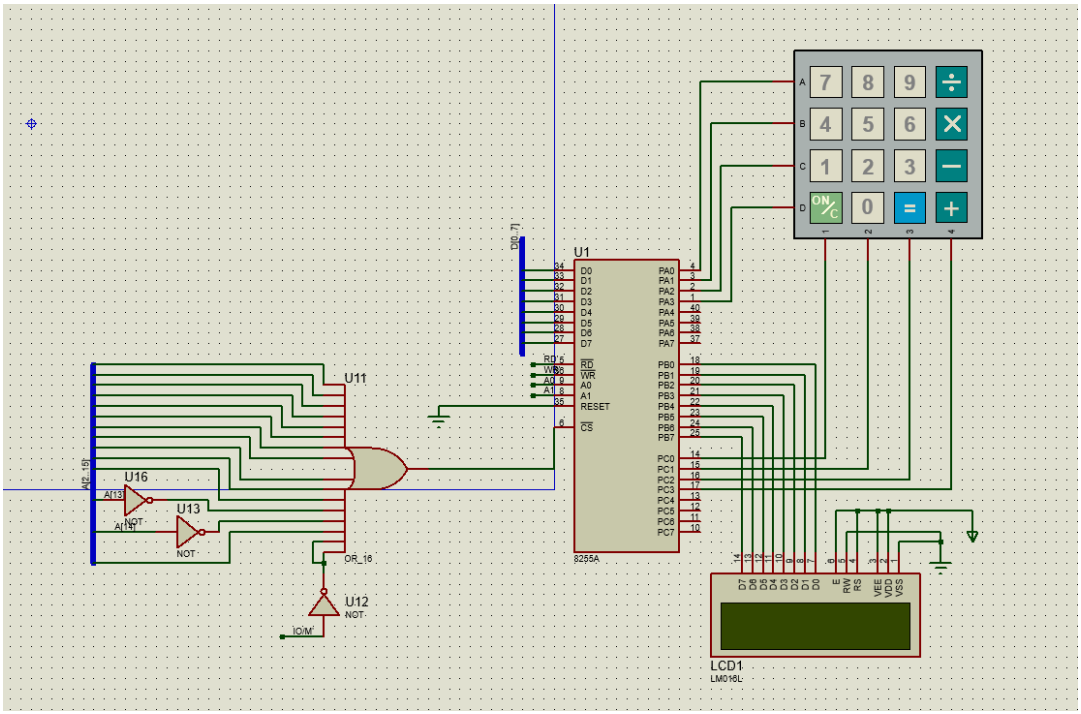


Screenshots:

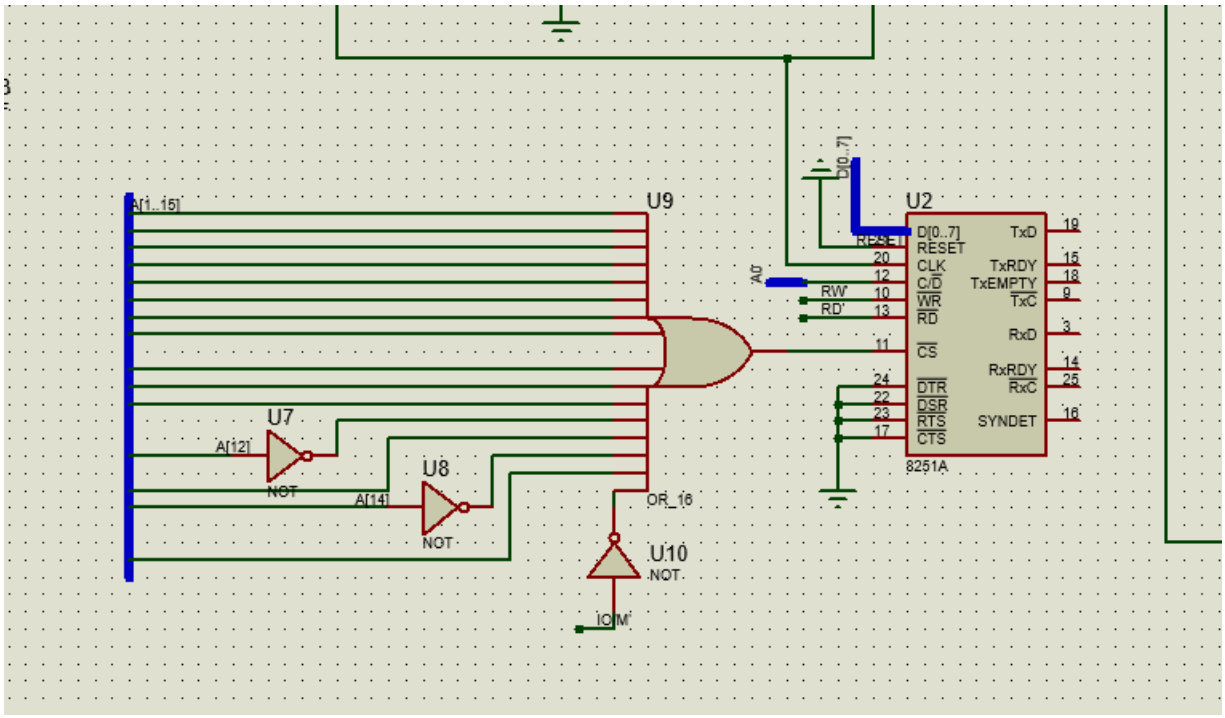
- 8086 connections [1]:



- 8255, Keyboard & LCD connection:



- 8251


A[1..15]
U9
U2
D[0..7]
RESET
CLK
C/D
WR
RD
CS
DTR
DSR
RTS
CTS
TxD
TxRDY
TxEMPTY
TxC
RxD
RxRDY
RxC
SYNDET
8251A
A0
RW'
RD'
U7
A[12]
NOT
U8
A[14]
NOT
OR_16
U10
NOT
IO/M'

References

[1] https://eepower.com/technical-articles/introduction-to-quartz-crystal-oscillators/