Tell40 for VELO

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Input links.

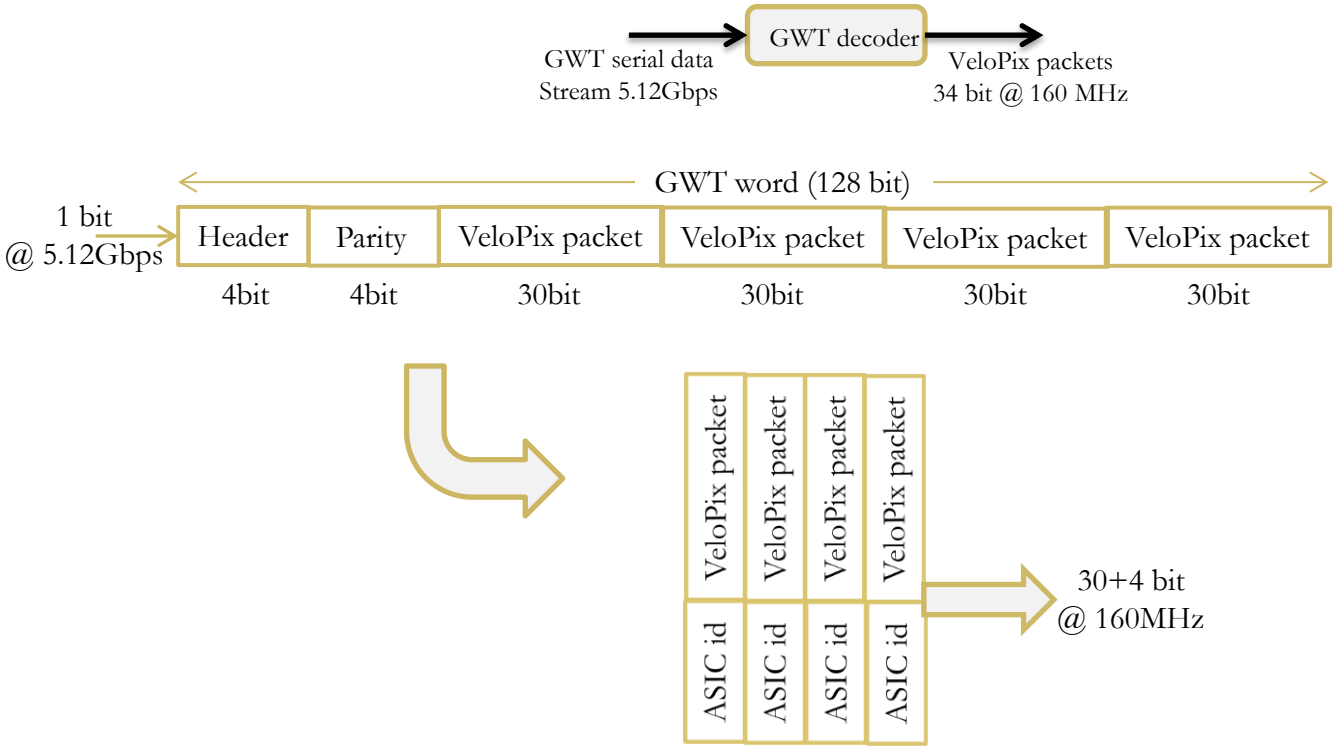
- Velo upgrade will have 52 modules.
- We will need 1 Tell40 per module : 52 total.
- 20 input links per Tell40:
  - Average occupancy of links is varying between 3.8 and 1.6 Gbit/s.
  - Aggregate peak input data rate for hottest module= 61.2 Gbit/s.
  - Well below PCIx 100Gbit/s output rate.
  - Some data reduction is foreseen (remove bcid), but very small.

- Not : TDR is out of date on number of links & Tell40!

Velo is not using GBT.

- Velo datalinks are not using standard or wide bus GBT.
  - Cannot use GBTx components: input link speed (320MHz)is too low.
  - The serializers must be integrated in front end asics.
    - 15 Gbit/s is peak data rate for hottest asic !
    - 4 high speed links per asic are required.
    - Need to optimise for power !
- Velo adopted GWT ("Giga Wire Transmitter) serializer:
  - See TWEPP 2014 for presentation.
  - Link speed is 5.12 Gbit/s.
  - GWT frame size is 128 bit : 8 header and 120 user bits.
    - User bandwidth = 4.8 Gbit/s
  - Simple ! Fixed header, fixed length, fixed alignment in GWT frame

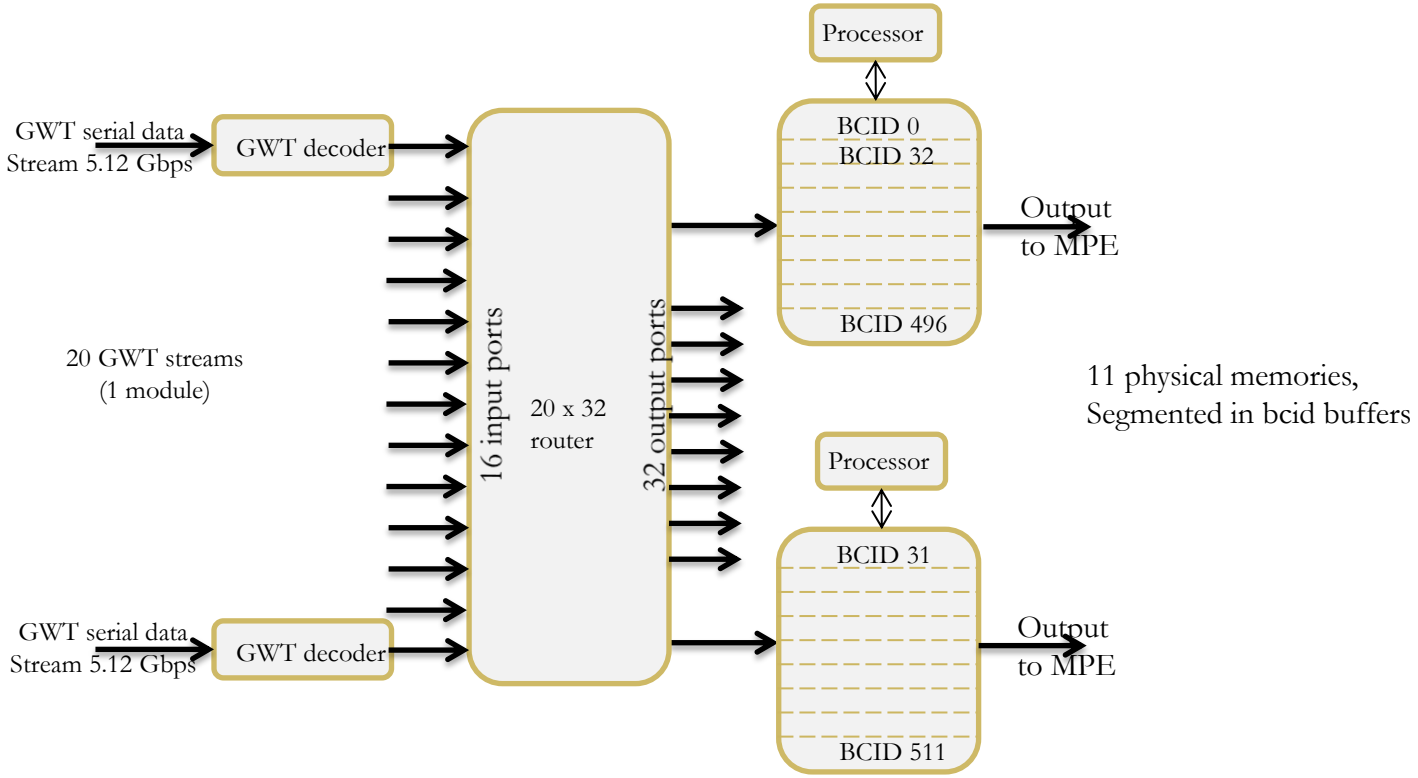
GWT format and decoding



- Decoder must extract fixed length (30 bit) and fixed position VeloPix packets from 128 bit GWT words. Add a 4 bit ASIC identifier.
- This is integrated in the LLI of the AMC40 framework.
  - That code is implemented an working.
  - FPGA Ressource usage is comparable to GBT widebus decoding.

'Time reordering'.

- Velopix packets are not chronological : random in time.
- Reorder or regroup in time: based on a packet router. All VeloPix packets with the same BCID are collected in one BCID or event buffer. The routing destination is based on the 9 bit BCID contained in the packet.



‘Time reordering’.

- Two option of the router are implemented and simulated.
- Still trying to optimize design for highest clock speed. Aiming at 320 MHz.

- Ressource usage:
  - 45K ALM, 150K registers and 17Mbit memory.
  - Arria10: 10% ALM, ‚30% memory

Next steps:

- Interface with TFC and MEP building.