EE4012 VLSI System Design—Homework 1

1. Design an 8-bit two-level carry lookahead adder (CLA). Draw the gate-level diagram of the two-level CLA. (4 points)

2. Figure 1 shows an n-bit serial-parallel multiplexer-based adder. Design a 4-bit serial-parallel multiplexer-based adder and verify the adder using Hspice. Measure the worst-case delay and power of the adder by applying exhaustive stimuli. Also, report the total area of the adder in terms of $\sum_{i=0}^{n-1} W_i Li$, where W_i and L_i denote the width and length of the ith transistor in the adder. Design objective is to minimize the product of delay and power. (6 points) (Metrics of grade: energy and area)

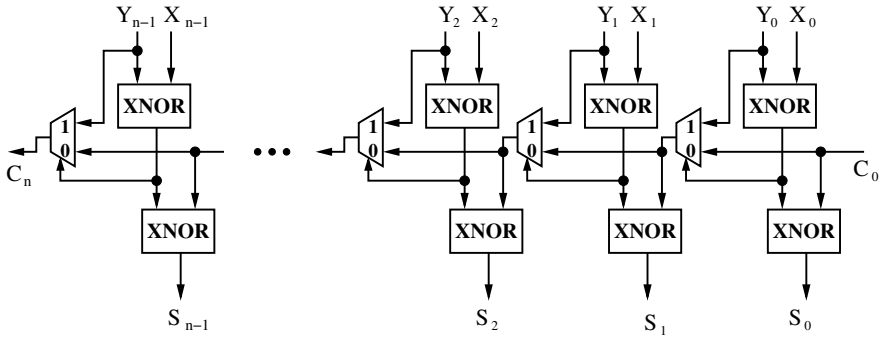

Figure 1: Block diagram of an n-bit multiplexer-based adder.