EE4012 VLSI System Design—Homework 4

1. Design a fully associative cache with 64 128-bit cache lines using Verilog. Fig. 1 shows the block diagram of the cache. Verify your design by showing two simulation cases: cache hit and cache miss. In the hit case, the output data of cache should be shown. (10 ponits)

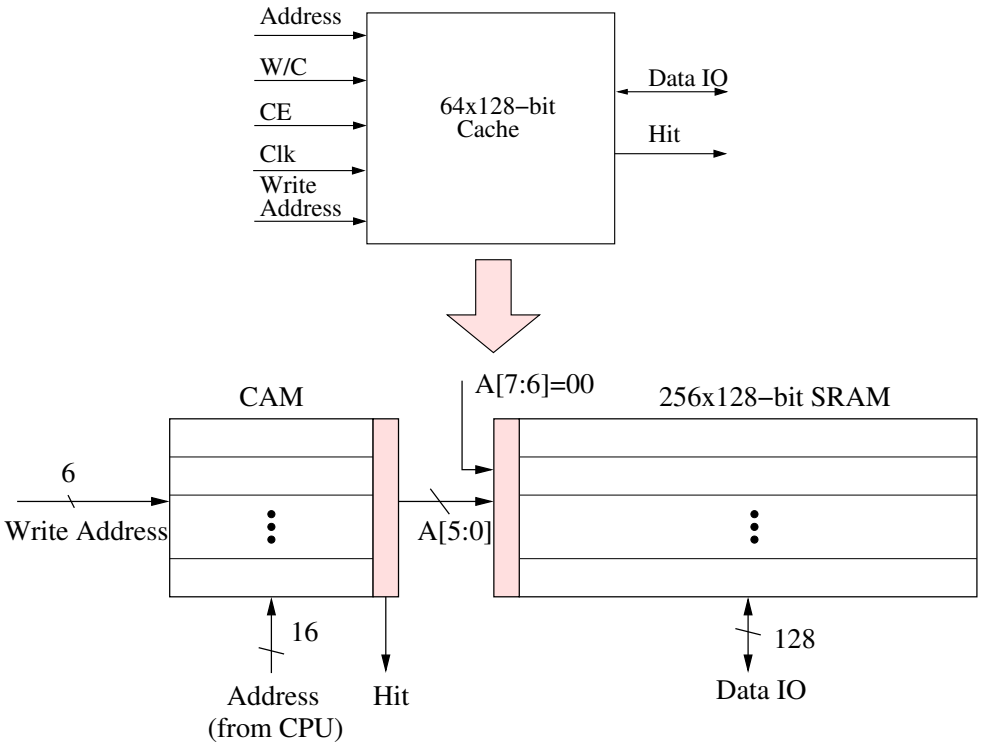

Figure 1: Block diagram of a cache with 64 128-bit cache lines.