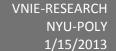
2013

HOW TO: ML507 DESIGN TEST WITH ETHERNET

TUTORIAL





ML507 DESIGN TEST WITH INTERNET

- 1. We are running in GMII/MII Mode: Set the jumper J22 and J23 across ENET and MODE.
- 2.We need 125Mhz clock for Ethernet PHY interface: Set the SW behind the FPGA to 00111010.
- 3. Set Up Host: HOST IP Address is 1.2.3.9 Subnet 255.255.0. Flow control--> Auto; Speed & Duplex-->Auto
- 4. Set Up ARP: Open cmd window as an administrator: arp -s 1.2.3.5 00-0a-35-01c9-58

IF problem: type the command netsh interface ip delete arpcache and execute. Then set the arp cache for xilinx.

- 5 Open wireshark, ping 1.2.3.5--> See output; The IP addresses will not be changed but source and mac addresses will be changed.
- 6. Run SIP inspector.
- 7. UART trouble shooting still at large. Current Baud Rate 38400

HOW TO: ML507 DESIGN TEST WITH ETHERNET

FPGA JUMPERS

SET JUMPERS J22 and J23 across ENET and MODE [To run EMAC in GMII/MII mode].

FPGA SWITCHES

Set the SW behind the FPGA to 00111010. [To generate 125MHz for Ethernet PHY].

HOST PC SETUP

Go to "Network and Sharing Center" --> "Change Adapter Settings"--> LAN-->"Properties"--> Click "Internet Protocol Version 4".

Set the HOST IP Address to 1.2.3.9 and SUBNET 255.255.255.0

In Advanced Properties set: "Flow control"--> Auto and "Speed & Duplex"-->Auto.

Open a cmd window as an administrator: arp -s 1.2.3.5 00-0a-35-01-c9-58 (Xilinx Device MAC ID)

Program the Design to FPGA. If you don't see RX and TX LED Blink, press PHY_RESET button, the Ethernet PHY should start working.

Open wireshark, ping 1.2.3.5--> See output; The IP addresses will not be changed but source and mac addresses will be changed

