LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII v11.2

DS264 January 18, 2012 **Product Specification**

Introduction

The LogiCORE™ Ethernet 1000BASE-X PCS/PMA or Serial Gigabit Media Independent Interface (SGMII) core provides a flexible solution for connection to an Ethernet Media Access Controller (MAC) or other custom logic. It supports two standards of operation that can be dynamically selected:

- 1000BASE-X Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) operation, as defined in the *IEEE 802.3-2008* standard
- Gigabit Media Independent Interface (GMII) to Serial-GMII (SGMII) bridge or SMGII to GMII bridge, as defined in the Serial-GMII specification (ENG-46158)

Features

- Supported physical interfaces for 1000BASE-X and SGMII standards:
  - Integrated transceiver interface using one of the following:
    - Virtex®-7 and Kintex™-7 Field Programmable Gate Array (FPGA) GTX Transceiver
    - Virtex-6 FPGA GTX Transceiver
    - Virtex-5 FPGA RocketIO™ GTP or GTX Transceiver
    - Virtex-4 FPGA RocketIO Multi-Gigabit Transceiver (MGT)
    - Spartan®-6 FPGA GTP Transceiver
  - Parallel Ten-Bit-Interface (TBI) for connection to external SERDES. See Voltage Requirements.
  - Support for SGMII over Select Input/Output (I/O) Low Voltage Differential Signaling (LVDS) in Virtex-6 FPGA -2 and faster devices
- Configured and monitored through the serial Management Data Input/Output (MDIO) Interface (MII Management), which can optionally be omitted from the core
- Supports 1000BASE-X Auto-Negotiation for information exchange with a link partner, which can optionally be omitted from the core
- Supports SGMII Auto-Negotiation for communication with the external Physical-Side Interface (PHY) device
- Internal or external GMII to MAC or custom logic. See Voltage Requirements.
- Available under terms of the Xilinx End User License Agreement

LogiCORE IP Facts Table						
Core Specifics						
Supported Device Family[1]	Virtex-7, Kintex-7, Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3, Spartan-3E, Spartan-3A/3A DSP					
Supported User Interfaces	GMII					
Resources[2]						
Slices	**GTs**	**LUTs**	**FFs**	**DCM**	**BUFG**	**Block RAMs**
140–1100	0-1	170–1090	180–940	0-3	2-4	0-2
Provided with Core						
Documentation	Product Specification User Guide					
Design Files	VHSIC Hardware Description Language (VHDL_ and Verilog, Native Generic Circuit (NGC) Netlist					
Example Designs	1000BASE-X PCS/PMA using a transceiver 1000BASE-X PCS with Ten-Bit Interface[3] GMII to SGMII Bridge for all supported interfaces[3]					
Test Bench	Demonstration Test Bench					
Constraints File	User Constraints File (.ucf)					
Simulation Model	Verilog and VHDL					
Tested Design Tools						
Design Entry Tools	Integrated Software Environment (ISE®) v13.4 design suite					
Simulation[4]	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator Synopsys Verilog Compiled Simulator (VCS) and VCS MX					
Synthesis Tools	Xilinx Synthesis Technology (XST) 13.4					
Support						
Provided by Xilinx, Inc.@ www.xilinx.com/support						
Voltage Requirements[3]						

1. For a complete listing of supported devices, see the release notes for this core. For supported family configurations see Table 9. For supported speed grades see Speed Grades.
2. The precise number depends on user configuration; see Table 10.
3. See Voltage Requirements.
4. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide. Also see Simulation for more information.

Applications

Typical applications for the Ethernet 1000BASE-X PCS/PMA or SGMII core include the following:

- Ethernet 1000BASE-X
- Serial-GMII

Ethernet 1000BASE-X

Figure 1 illustrates a typical application for the Ethernet 1000BASE-X PCS/PMA or SGMII core with the core operating to the 1000BASE-X standard using a device-specific transceiver to provide the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayers for 1-Gigabit Ethernet.

- The PMA is connected to an external off-the-shelf Gigabit Interface Converter (GBIC) or Small Form-Factor Pluggable (SFP) optical transceiver to complete the Ethernet port.
- The GMII of the Ethernet 1000BASE-X PCS/PMA is connected to an embedded Ethernet Media Access Controller (MAC), for example, the Xilinx® Tri-Mode Ethernet MAC core.

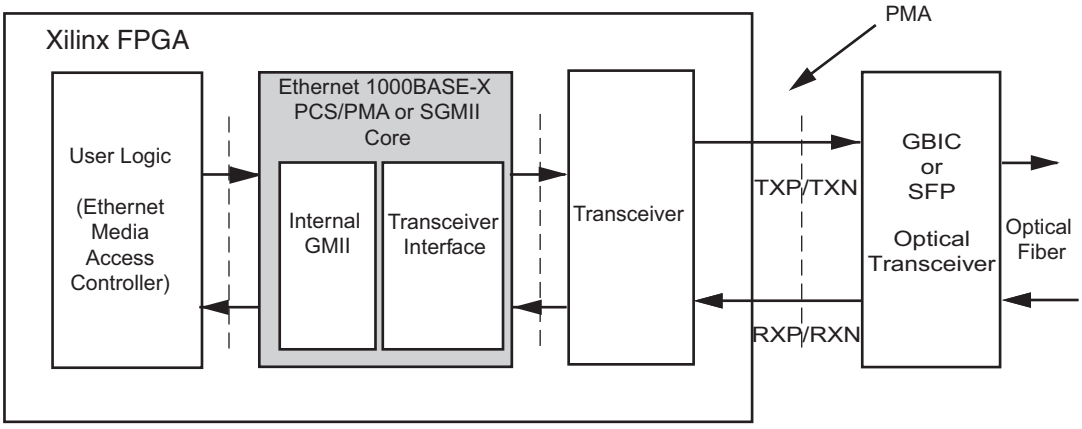


Figure 1: **Typical 1000BASE-X Application**

Serial-GMII

Ethernet 1000BASE-X PCS/PMA or SGMII core can operate in two modes as shown in the following subsections.

GMII to SGMII Bridge

Figure 2 illustrates a typical application for the Ethernet 1000BASE-X PCS/PMA or SGMII core, which shows the core providing a GMII to SGMII bridge using a device-specific transceiver to provide the serial interface.

- The device-specific transceiver is connected to an external off-the-shelf Ethernet PHY device that also supports SGMII. (This can be a tri-mode PHY providing 10BASE-T, 100BASE-T, and 1000BASE-T operation.)
- The GMII of the Ethernet 1000BASE-X PCS/PMA or SGMII core is connected to an embedded Ethernet MAC, for example, the Xilinx Tri-Mode Ethernet MAC core.

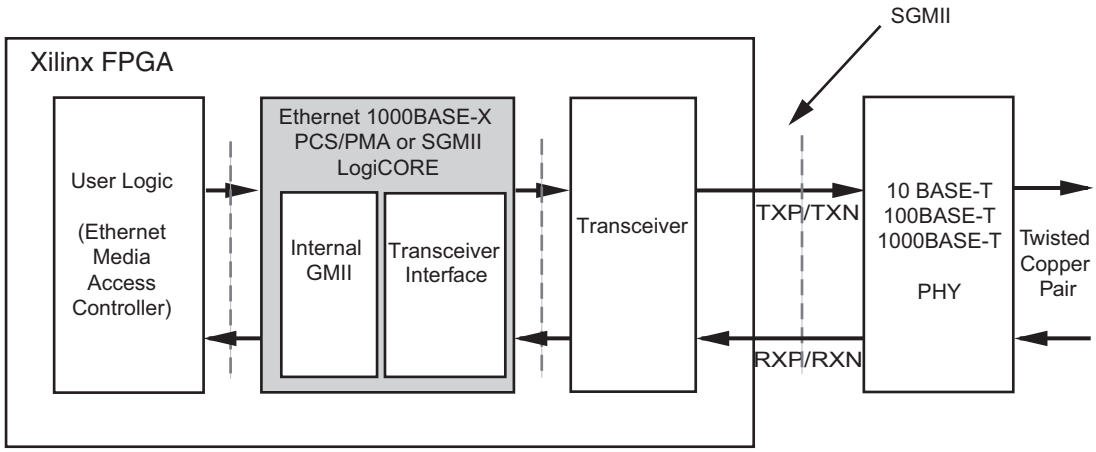


Figure 2: **Typical Application for GMII to SGMII Bridge Mode**

SGMII to GMII Bridge

Figure 3 illustrates a typical application for the Ethernet 1000BASE-X PCS/PMA or SGMII core, which shows the core providing a SGMII to GMII bridge using a device-specific transceiver to provide the serial interface.

- The device-specific transceiver is connected to an external off-the-shelf Ethernet MAC device that also supports SGMII. (This can be a tri-mode MAC providing 10/100/1000 Mb/s operation, for example, the Xilinx Tri-Mode Ethernet MAC core connected to 1000BASE-X PCS/PMA or SGMII core operating in GMII to SGMII Mode)
- The GMII of the Ethernet 1000BASE-X PCS/PMA or SGMII core is connected to a tri-mode PHY providing 10BASE-T, 100BASE-T, and 1000BASE-T operation.

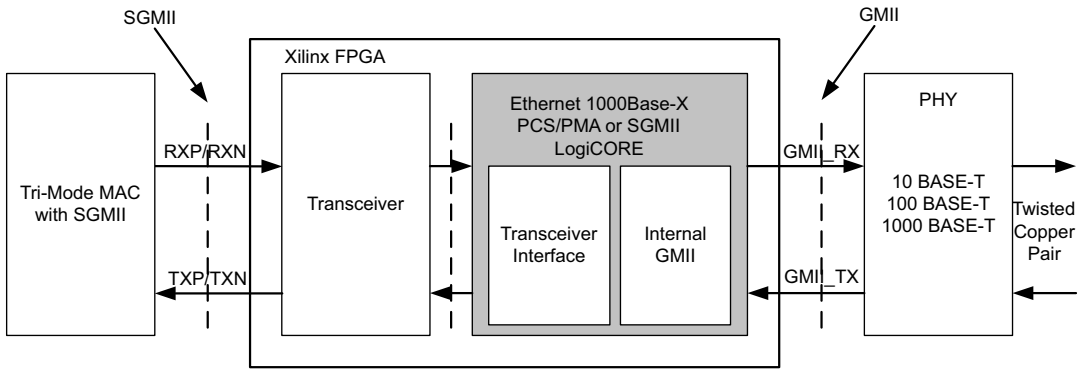


Figure 3: **Typical Application for SGMII to GMII Bridge Mode**

Overview of Ethernet Architecture

Figure 4 illustrates the 1-Gigabit Ethernet PCS and PMA sublayers provided by this core, which are part of the Ethernet architecture. The part of this architecture, from the MAC to the right, is defined in the *IEEE 802.3-2008* specification. This figure also shows where the supported interfaces fit into the architecture.

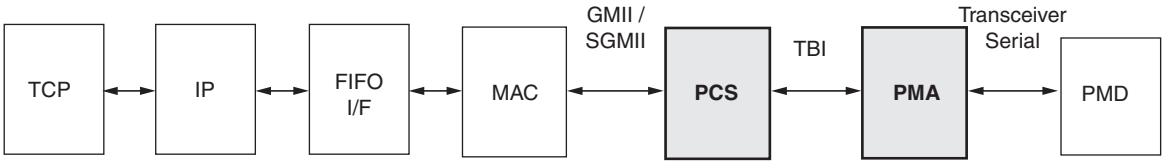


Figure 4: **Overview of Ethernet Architecture**

MAC

The Ethernet Media Access Controller (MAC) is defined in *IEEE 802.3-2008*, clauses 2, 3, and 4. A MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can connect to, any type of physical layer device.

GMII / SGMII

The Gigabit Media Independent Interface (GMII), a parallel interface connecting a MAC to the physical sublayers (PCS, PMA, and PMD), is defined in *IEEE 802.3-2008*, clause 35. For a MAC operating at a speed of 1 Gigabit per second (Gb/s), the full GMII is used; for a MAC operating at a speed of 10 Mb/s or 100 Mb/s, the GMII is replaced with a Media Independent Interface (MII) that uses a subset of the GMII signals.

The Serial-GMII (SGMII) is an alternative interface to the GMII/MII that converts the parallel interface of the GMII/MII into a serial format capable of carrying traffic at speeds of 10 Mb/s, 100 Mb/s, and 1 Gb/s. This radically reduces the I/O count and for this reason is often preferred by Printed Circuit Board (PCB) designers. The SGMII specification is closely related to the 1000BASE-X PCS and PMA sublayers, which enables it to be offered in this core.

PCS

The Physical Coding Sublayer (PCS) for 1000BASE-X operation is defined in *IEEE 802.3-2008*, clauses 36 and 37, and performs these operations:

- Encoding (and decoding) of GMII data octets to form a sequence of ordered sets
- 8B/10B encoding (and decoding) of the sequence ordered sets
- 1000BASE-X Auto-Negotiation for information exchange with the link partner

Ten Bit Interface

The Ten-Bit-Interface (TBI), defined in *IEEE 802.3-2008* clause 36 is a parallel interface connecting the PCS to the PMA and transfers the 8B/10B encoded sequence-ordered sets. The TBI should be used with an external SERDES device to implement the PMA functionality.

Physical Medium Attachment

The Physical Medium Attachment (PMA) for 1000BASE-X operation, defined in *IEEE 802.3-2008* clause 36, performs the following:

- Serialization (and deserialization) of code-groups for transmission (and reception) on the underlying serial Physical Medium Dependent (PMD)
- Recovery of the clock from the 8B/10B-coded data supplied by the PMD

The device-specific transceivers provide the serial interface required to connect the PMD.

Physical Medium Dependent

The PMD sublayer is defined in *IEEE 802.3-2008* clause 38 for 1000BASE-LX and 1000BASE-SX (long and short wavelength laser). This type of PMD is provided by the external GBIC or SFP optical transceivers. An alternative PMD for 1000BASE-CX (short-haul copper) is defined in *IEEE 802.3-2008* clause 39.

Core Overview

Ethernet 1000BASE-X PCS/PMA or SGMII Support Using a Device Specific Transceiver

Using the Ethernet 1000BASE-X PCS/PMA or SGMII core with the device-specific transceiver provides the functionality to implement the 1000BASE-X PCS and PMA sublayers. Alternatively, it can be used to provide a GMII to SGMII bridge.

The core interfaces to a device-specific transceiver, which provides some of the PCS layer functionality such as 8B/10B encoding/decoding, the PMA Serializer/Deserializer (SERDES), and clock recovery. Figure 5 illustrates the remaining PCS sublayer functionality and the major functional blocks of the core. A description of the functional blocks and signals is provided in subsequent sections.

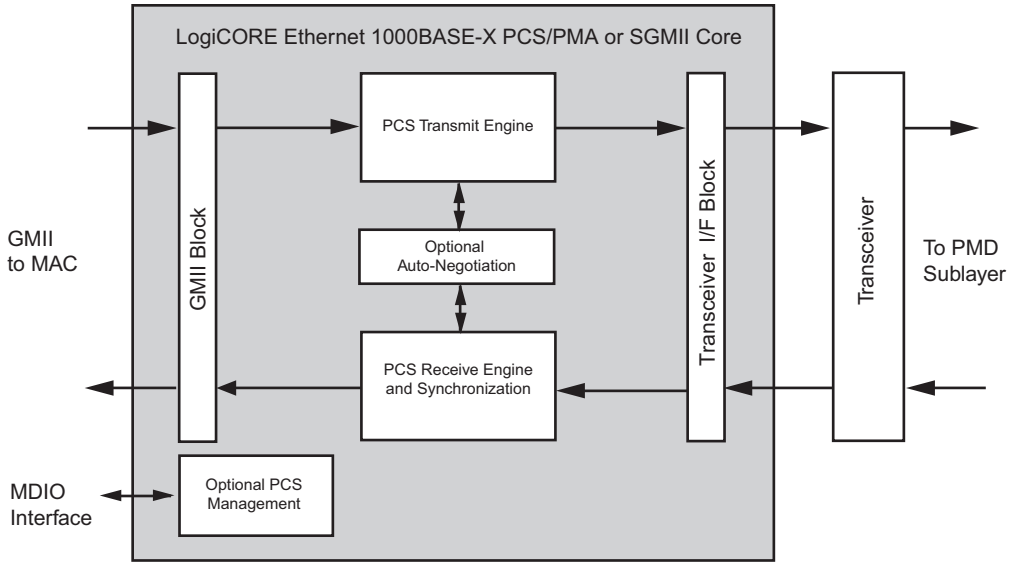


Figure 5: **Ethernet 1000BASE-X PCS/PMA or SGMII Core Using a Device-Specific Transceiver**

GMII Block

The core provides a client-side GMII. This can be used as an internal interface for connection to an embedded MAC or other custom logic. Alternatively, the core GMII can be routed to device Input/Output Blocks (IOBs) to provide an off-chip GMII.

Virtex-7 devices support GMII at 3.3 V or lower only in certain parts and packages; see the *7 Series FPGAs SelectIO Resources User Guide*. Virtex-6 devices support GMII at 2.5 V only; see the *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*. Kintex-7, Spartan-6, Virtex-5, Virtex-4 and Spartan-3 devices support GMII at 3.3 V or lower.

PCS Transmit Engine

The PCS transmit engine converts the GMII data octets into a sequence of ordered sets by implementing the state diagrams of *IEEE 802.3-2008* (Figures 36-5 and 36-6).

PCS Receive Engine and Synchronization

The synchronization process implements the state diagram of *IEEE 802.3-2008* (Figure 36-9). The PCS receive engine converts the sequence of ordered sets to GMII data octets by implementing the state diagrams of *IEEE 802.3-2008* (Figures 36-7a and 36-7b).

Optional Auto-Negotiation Block

IEEE 802.3-2008 clause 37 describes the 1000BASE-X Auto-Negotiation function that allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (link partner), and to detect corresponding operational modes that the link partner might be advertising. Auto-Negotiation is controlled and monitored through the PCS Management registers.

Optional PCS Management Registers

Configuration and status of the core, including access to and from the optional Auto-Negotiation function, is performed with the 1000BASE-X PCS Management registers as defined in *IEEE 802.3-2008* clause 37. These registers are accessed through the serial Management Data Input/Output Interface (MDIO), defined in *IEEE 802.3-2008* clause 22, as if it were an externally connected PHY.

An additional configuration interface is provided to program Control register (Register 0) and Auto-Negotiation advertisement (Register 4) independent of the MDIO interface.

The PCS Management registers can be omitted from the core when the core is performing the 1000BASE-X standard. In this situation, configuration and status is made possible by using additional configuration vector and status signals. When the core is performing the SGMII standard, PCS Management registers become mandatory and information in the registers takes on a different interpretation. See the *LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII User Guide*.

Transceiver Interface Block

The interface block enables the core to connect to a device-specific transceiver.

Ethernet 1000BASE-X PCS/PMA or SGMII Support with Ten-Bit Interface

When used with the TBI, the Ethernet 1000BASE-X PCS/PMA or SGMII core provides the functionality to implement the 1000BASE-X PCS sublayer (or to provide SGMII support) with use of an external SERDES.

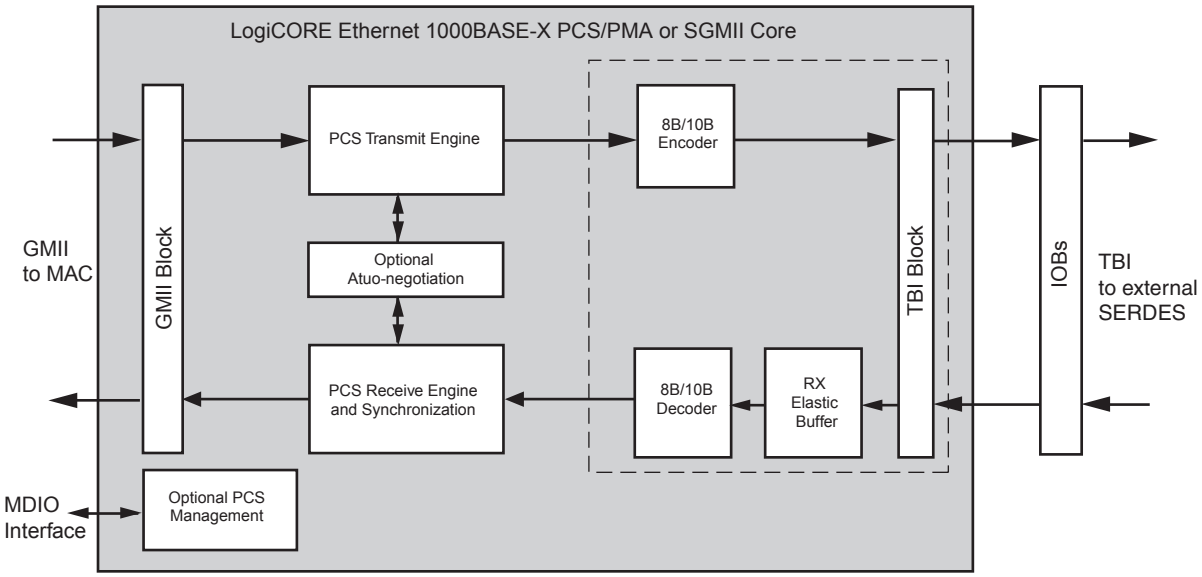


Figure 6: **Functional Block Diagram of the Ethernet 1000BASE-X PCS/PMA or SGMII Core with TBI**

The optional TBI is used in place of the device-specific transceiver to provide a parallel interface for connection to an external PMA SERDES device, allowing an alternative implementation for families without device-specific transceivers. In this implementation, additional logic blocks are required in the core to replace some of the device-specific transceiver functionality. These blocks are surrounded by a dashed line (see Figure 6). Other blocks are identical to those previously defined.

Virtex-7 devices do not support TBI. Virtex-6 devices support TBI at 2.5 V only; see the *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*. Kintex-7, Spartan-6, Virtex-5, Virtex-4 and Spartan-3 devices support TBI at 3.3 V or lower.

8B/10B Encoder

8B/10B encoding, as defined in *IEEE 802.3-2008* (Tables 36-1a to 36-1e and Table 36-2), is implemented in a block SelectRAM™ memory, configured as ROM, and used as a large look-up table.

8B/10B Decoder

8B/10B decoding, as defined in *IEEE 802.3-2008* (Tables 36-1a to 36-1e and Table 36-2), is implemented in a block SelectRAM memory, configured as ROM, and used as a large look-up table.

Receiver Elastic Buffer

The Receiver Elastic Buffer enables the 10-bit parallel TBI data, received from the PMA sublayer synchronously to the TBI receiver clocks, to be transferred onto the core internal 125 MHz clock domain.

The Receiver Elastic Buffer is an asynchronous First In First Out (FIFO) implemented in internal RAM. The operation of the Receiver Elastic Buffer attempts to maintain a constant occupancy by inserting or removing Idle sequences as necessary. This causes no corruption to the frames of data.

TBI Block

The core provides a TBI interface, which should be routed to device IOBs to provide an off-chip TBI. See the *LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII User Guide (UG155)*.

SGMII Support Using Asynchronous Oversampling over Virtex-6 FPGA LVDS

Virtex-6 devices, -2 speed grade or higher, can fully support SGMII using standard LVDS SelectIO™ technology logic resources. This enables direct connection to external PHY devices without the use of a Virtex-6 FPGA GTX transceiver.

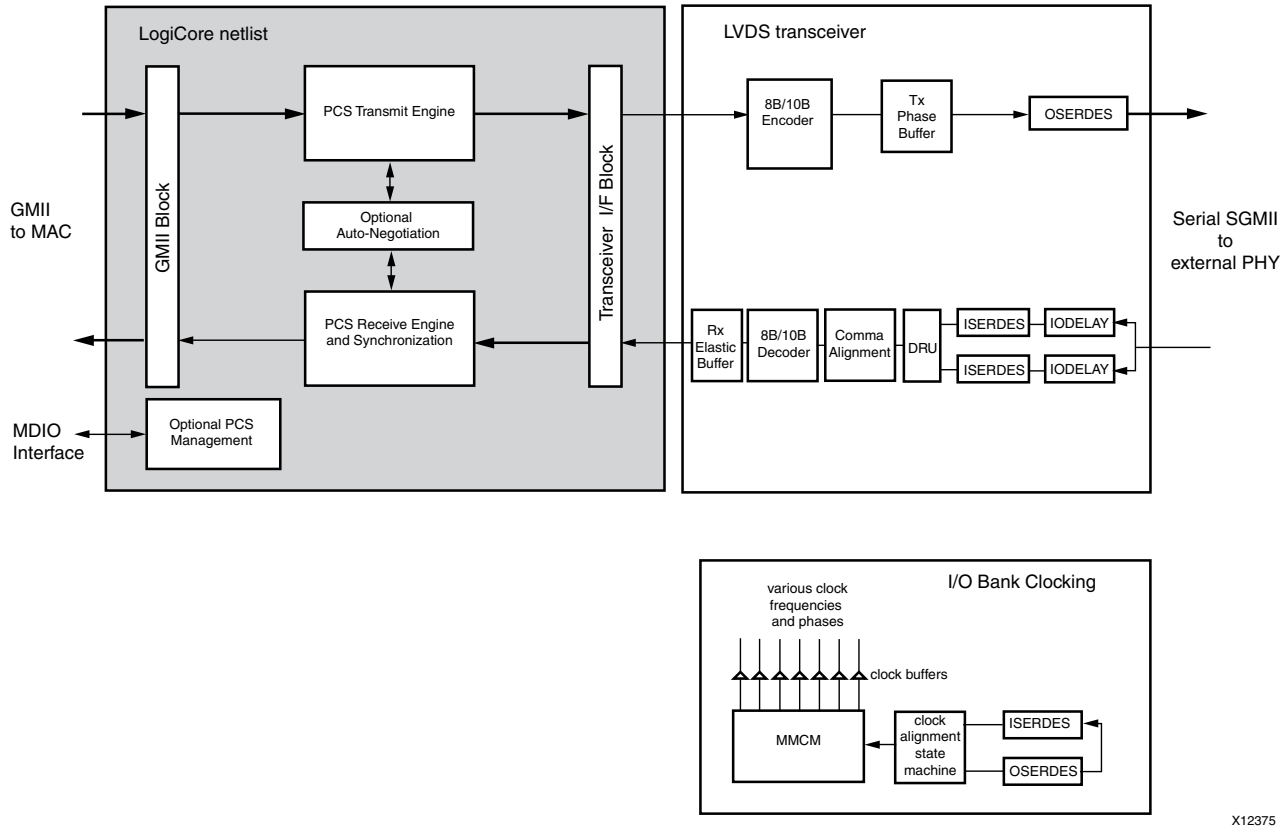


Figure 7: **Functional Block Diagram of the Core with Standard SelectIO Technology Support for SGMII**

This implementation is illustrated in Figure 7.

The core netlist in this implementation remains identical to that of Figure 5 and all core netlist blocks are identical to those described in Ethernet 1000BASE-X PCS/PMA or SGMII Support Using a Device Specific Transceiver.

As illustrated in Figure 7, the Hardware Description Language (HDL) example design for this implementation provides additional logic to form the "LVDS transceiver" block which fully replaces the functionality otherwise provided by a Virtex-6 FPGA GTX transceiver. The LVDS transceiver block contains IODELAY and ISERDES elements along with a Data Recovery Unit (DRU). This block uses the Virtex-6 FPGA ISERDES elements in a new asynchronous oversampling mode as described in XAPP881 *1.25Gbs 4x Asynchronous Oversampling over Virtex-6 LVDS*. The full transceiver functionality is then completed with Comma Alignment, 8B/10B Decoder and Rx Elastic buffer blocks.

Figure 7 also illustrates the inclusion of the "I/O Bank Clocking." This block creates all of the clock frequencies and clock phases that are required by the LVDS transceiver block. As the name of the block suggests, this logic can be shared across a single Virtex-6 FPGA I/O bank. This I/O bank can be used for multiple instances of the core with LVDS I/O to create several independent SGMII ports.

See the *LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII v11.2 User Guide (UG155)* for a detailed description of the LVDS SelectIO technology SGMII implementation. The following four subsections describe design requirements.

SGMII Only

The interface implemented using this asynchronous oversampling method supports SGMII between the FPGA and an external PHY device; the interface cannot directly support 1000BASE-X.

Supported in Virtex-6 Devices, -2 Speed Grade or Faster

The SGMII LVDS implementation has only been characterized in the -2 speed grade and faster Virtex-6 devices.

Timing closure of this interface is challenging; perform the layout and placement steps described in "Layout and Placement" in the *LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII v11.2 User Guide (UG155)*.

Receiver UI Specification

The DRU must have at least two valid sampling points per data bit, requiring 0.5 UI of opening. The settings of the FPGA add 0.125 UI of requirement making a total opening requirement at the receiver of 0.625 UI.

Recommended for Chip-to-Chip Copper Implementations Only

This interface supports an SGMII link between the FPGA and an external PHY device across a single PCB; keep the SGMII copper signal lengths to a minimum.

Interface Descriptions

All ports of the core are internal connections in FPGA logic. An HDL example design, provided in both VHDL and Verilog, is delivered with the core. Where appropriate, the example design connects the core to a device-specific transceiver, LVDS transceiver logic and/or adds IBUFs, OBUFs, and IOB flip-flops to the external signals of the GMII and TBI. IOBs are added to the remaining unconnected ports to take the example design through the Xilinx implementation software. All clock management logic is placed in this example design, allowing for more flexibility in implementation; for example, in designs using multiple cores. For information about the example designs, see the *LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII v11.2 User Guide (UG155)*.

GMII Signal Definition

Table 1 defines the GMII-side interface signals common to all parameterizations of the core. These are typically attached to an Ethernet MAC, either off-chip or internally integrated. The HDL example design delivered with the core connects these signals to IOBs to provide a place-and-routable example.

Table 1: **GMII Interface Signal Pinout**

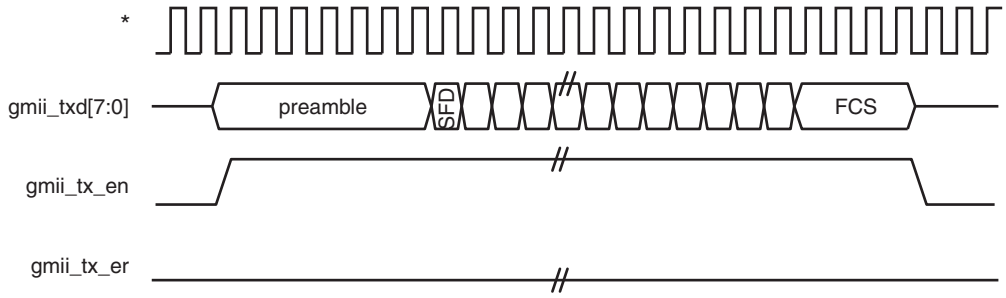
Signal	Direction	Clock Domain	Description
gmii_txd[7:0]	Input	See Note	GMII Transmit data from MAC
gmii_tx_en	Input		GMII Transmit control signal from MAC
gmii_tx_er	Input		GMII Transmit control signal from MAC
gmii_rxd[7:0]	Output		GMII Received data to MAC
gmii_rx_dv	Output		GMII Received control signal to MAC
gmii_rx_er	Output		GMII Received control signal to MAC
gmii_isolate	Output		IOB 3-state control for GMII Isolation. Only of use when implementing an External GMII as illustrated by the example design HDL.

Note: Signals are synchronous to the cores internal 125 MHz reference clock; `userclk2` when used with the device-specific transceiver, and `gtx_clk` when used with TBI.

GMII Usage Example

Standard Frame Transmission

Figure 8 illustrates the timing of normal outbound frame transfer. This figure shows that an Ethernet frame is preceded by an 8-byte preamble field and completed with a 4-byte frame check sequence (FCS) field (*IEEE 802.3-2008* clause 3). This is driven by the core transmitter client logic (usually a MAC connected to the other end of the GMII). The PCS treats any value placed on `gmii_txd[7:0]` within the `gmii_tx_en` assertion window as data.



* See note 1 in Table 1

Figure 8: **GMII Standard Frame Transmission**

Standard Frame Reception

Figure 9 illustrates the timing of a normal inbound frame transfer. This figure shows that Ethernet frame reception is preceded by a preamble field; the *IEEE 802.3-2008* specification allows for up to all of the seven preamble bytes that precede the Start of Frame Delimiter (SFD) to be lost (*IEEE 802.3-2008* clause 35). The SFD is always present in well-formed frames. This frame is presented by the core to the receiver client logic (usually a MAC connected to the other end of the GMII).

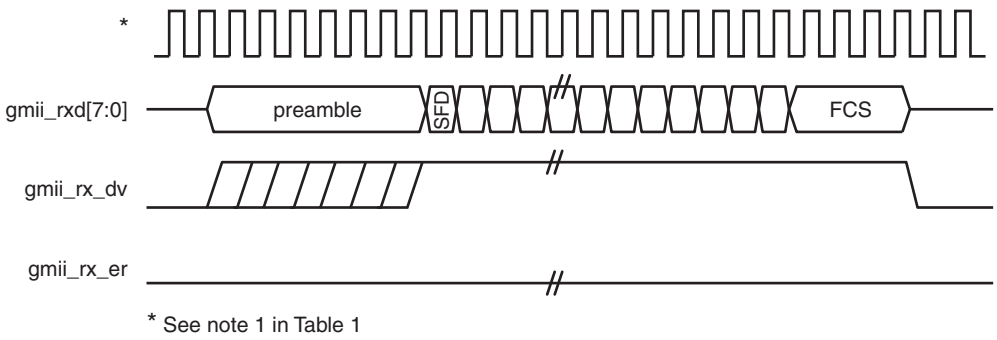


Figure 9: **GMII Standard Frame Reception**

Common Signal Definition

Table 2 defines the signals common to all parameterizations of the core.

Table 2: **Other Common Signals**

Signal	Direction	Clock Domain	Description
reset	Input	n/a	Asynchronous reset for the entire core. Active High.
signal_detect	Input	n/a	Signal direct from PMD sublayer indicating the presence of light detected at the optical receiver. If set to 1, this indicates that the optical receiver has detected light. If set to 0, this indicates the absence of light. If unused, this signal should be set to 1 to enable correct operation the core.
status_vector[15:0]	Output	See Note	• Bit[0]: **Link Status** This signal indicates the status of the link. When high, the link is valid: synchronization of the link has been obtained *and* Auto-Negotiation (if present and enabled) has successfully completed. When low, a valid link has not been established. Either link synchronization has failed or Auto-Negotiation (if present and enabled) has failed to complete. When auto-negotiation is enabled, this signal is identical to Status Register Bit 1.2: Link Status. When auto-negotiation is disabled, this signal is identical to status_vector Bit[1].
			• Bit[1]: **Link Synchronization** This signal indicates the state of the synchronization state machine (IEEE802.3 figure 36-9) which is based on the reception of valid 8B/10B code groups. This signal is similar to Bit[0] (Link Status), but is *not* qualified with Auto-Negotiation. When high, link synchronization has been obtained and in the synchronization state machine, sync_status=OK. When low, synchronization has failed.
			• Bit[2]: **RUDI(/C/)** The core is receiving /C/ ordered sets (Auto-Negotiation Configuration sequences).
			• Bit[3]: **RUDI(/I/)** The core is receiving /I/ ordered sets (Idles).
			• Bit[4]: **RUDI(INVALID)** The core has received invalid data while receiving/C/ or /I/ ordered set.
			• Bit[5]: **RXDISPERR** The core has received a running disparity error during the 8B/10B decoding function.
			• Bit[6]: **RXNOTINTABLE** The core has received a code group that is not recognized from the 8B/10B coding tables.
			• Bit[7]: **PHY Link Status (SGMII mode only)** When operating in SGMII mode, this bit represents the link status of the external PHY device attached to the other end of the SGMII link (high indicates that the PHY has obtained a link with its link partner; low indicates that is has not linked with its link partner). When operating in 1000BASE-X mode, this bit remains low and should be ignored.

Table 2: **Other Common Signals *(Cont'd)***

Signal	Direction	Clock Domain	Description
status_vector[15:0] (Continued)	Output	See Note	• Bit[9:8]: **Remote Fault Encoding** This signal indicates the remote fault encoding (IEEE802.3 table 37-3). This signal is validated by bit 13 of status_vector and is only valid when Auto-Negotiation is enabled. This signal has no significance when the core is in SGMII mode with PHY side implementation and indicates "00". In all the remaining modes, the signal indicates the remote fault encoding.
			• Bit [11:10]: **SPEED** This signal indicates the speed negotiated and is only valid when Auto-Negotiation is enabled. The signal encoding follows: Bit[11] Bit[10] 1 1 Reserved 1 0 1000 Mb/s 0 1 100 Mb/s 0 0 10 Mb/s
			• Bit[12]: **Duplex Mode** This bit indicates the Duplex mode negotiated with the link partner. 1 = Full Duplex 0 = Half Duplex
			• Bit[13] **Remote Fault** When this bit is logic one, it indicates that a remote fault is detected and the type of remote fault is indicated by status_vector bits[9:8]. ***Note:*** This bit is only deasserted when an MDIO read is made to status register (register 1). This signal has no significance in SGMII PHY mode.
			• Bits[15;14]: **Pause** These bits reflect the bits [8:7] of Register 5 (Link Partner Base AN Register) Bit[15] Bit[14] 0 0 No Pause 0 1 Symmetric Pause 1 0 Asymmetric Pause towards Link partner 1 1 Both Symmetric Pause and Asymmetric Pause towards link partner

Note: Signals are synchronous to the core internal 125 MHz reference clock; userclk2 when used with a device-specific transceiver; gtx_clk when used with TBI.

Optional Management I/F Signal Definition

Table 3 describes the optional MDIO interface signals of the core used to access the PCS Management registers. These signals are typically connected to the MDIO port of a MAC device, either off-chip or to an internally integrated MAC core.

Table 3: **Optional MDIO Interface Signal Pinout**

Signal	Direction	Clock Domain	Description
mdc	Input	n/a	Management clock (≤ 2.5 MHz)
mdio_in	Input	mdc	Input data signal
mdio_out	Output	mdc	Output data signal
mdio_tri	Output	mdc	Output 3-state driver for mdio_out. Active Low
phyad[4:0]	Input	n/a	Physical Address of the PCS Management register set. It is expected that this signal will be tied off to a logical value.

Configuration Vector Definition

Table 4 describes interfaces to program Registers 0 and 4 irrespective of optional MDIO.

Table 4: **Configuration Vectors**

Signal	Direction	Clock Domain	Description
configuration_vector[4:0]	Input	See Note	• Bit[0]: **Unidirectional Enable** When set to 1, Enable Transmit irrespective of state of RX (802.3ah). When set to 0, Normal operation • Bit[1]: **Loopback Control** When the core with a device-specific transceiver is used, this places the core into internal loopback mode. With the TBI version, Bit 1 is connected to ewrap. When set to 1, this signal indicates to the external PMA module to enter loopback mode. • Bit[2]: **Power Down** When the Virtex-7, Kintex-7, Virtex-6, Virtex-5 or Spartan-6 FPGA transceivers are used and set to 1, the device-specific transceiver is placed in a low-power state. A reset must be applied to clear. With the TBI version this bit is unused. • Bit[3] **Isolate** When set to 1, the GMII should be electrically isolated. When set to 0, normal operation is enabled. • Bit[4] **Auto-Negotiation Enable** This signal is valid only if the AN module is enabled through the CORE Generator™ tools Graphical User Interface (GUI). When set to 1, the signal enables the AN feature. When set to 0, AN is disabled.
configuration_valid	Input	See Note	This signal is valid only when the MDIO interface is present. The rising edge of this signal is the enable signal to overwrite the Register 0 contents that were written from the MDIO interface. For triggering a fresh update of Register 0 through configuration_vector, this signal should be deasserted and then reasserted.

Note: Signals are synchronous to the core internal 125 MHz reference clock; `userclk2` when used with a device-specific transceiver; `gtx_clk` when used with TBI.

Optional 1000BASE-X PCS/PMA (or SGMII) Using Transceiver Signal Definition

Table 5 defines the optional interface to the device-specific transceiver or to the LVDS SelectIO technology transceiver implementation. The core is connected to the chosen transceiver in the HDL example design delivered with the core. For a complete description of the device-specific transceiver interface, see the transceiver user guide specific to your device. (For user guide information, see [Ref 6], [Ref 7], and [Ref 8] at the end of this document.)

Table 5: **Optional Transceiver Interface Pinout**

Signal	Direction	Clock Domain	Description
mgt_rx_reset	Output	userclk2	Reset signal issued by the core to the device-specific transceiver receiver path. Connect to RXRESET signal of the transceiver.
mgt_tx_reset	Output	userclk2	Reset signal issued by the core to the device-specific transceiver transmitter path. Connect to TXRESET signal of transceiver.
userclk	Input	n/a	Also connected to TXUSRCLK and RXUSRCLK of the device-specific transceiver.
userclk2	Input	n/a	Also connected to TXUSRCLK2 and RXUSRCLK2 of the device-specific transceiver.
dcm_locked	Input	n/a	A Digital Clock Manager (DCM) can be used to derive userclk and userclk2. This is implemented in the HDL design example delivered with the core. The core uses this input to hold the device-specific transceiver in reset until the DCM obtains lock.
rxbufstatus[1:0]	Input	userclk2	Connects to transceiver signal of the same name.
rxchariscomma	Input	userclk2	
rxcharisk	Input	userclk2	
rxclkcorcnt[2:0]	Input	userclk2	
rxdata[7:0]	Input	userclk2	
rxdisperr	Input	userclk2	
rxnotintable	Input	userclk2	
rxrundisp	Input	userclk2	
txbuferr	Input	userclk2	
powerdown	Output	userclk2	
txchardispmode	Output	userclk2	
txchardispval	Output	userclk2	
txcharisk	Output	userclk2	
txdata[7:0]	Output	userclk2	
enablealign	Output	userclk2	Allows the transceivers to serially realign to a comma character. Connect to ENMCOMMAALIGN and ENPCOMMAALIGN of the device-specific transceiver.

Note: When the core is used with the device-specific transceiver, `userclk2` is used as the 125 MHz reference clock for the entire core.

Optional 1000BASE-X PCS with TBI Signal Definition

Table 6 defines the optional TBI signals that can be used as an alternative to the transceiver interfaces. The appropriate HDL example design delivered with the core connects these signals to IOBs to provide an external TBI suitable for connection to an off-chip PMA SERDES device.

Table 6: **Optional TBI Interface Signal Pinout**

Signal	Direction	Clock Domain	Description
gtx_clk	Input	n/a	Clock signal at 125 MHz. Tolerance must be within *IEEE 802.3-2008* specification.
tx_code_group[9:0]	Output	gtx_clk	10-bit parallel transmit data to PMA Sublayer (SERDES).
loc_ref	Output	n/a	Causes the PMA sublayer clock recovery unit to lock to pma_tx_clk. This signal is currently tied to Ground.
ewrap	Output	gtx_clk	When '1,' indicates to the external PMA SERDES device to enter loopback mode. When '0,' this indicates normal operation.
rx_code_group0[9:0]	Input	pma_rx_clk0	10-bit parallel received data from PMA Sublayer (SERDES). This is synchronous to pma_rx_clk0.
rx_code_group1[9:0]	Input	pma_rx_clk1	10-bit parallel received data from PMA Sublayer (SERDES). This is synchronous to pma_rx_clk1.
pma_rx_clk0	Input	n/a	Received clock signal from PMA Sublayer (SERDES) at 62.5 MHz.
pma_rx_clk1	Input	n/a	Received clock signal from PMA Sublayer (SERDES) at 62.5 MHz. This is 180 degrees out of phase with pma_rx_clk0.
en_cdet	Output	gtx_clk	Enables the PMA Sublayer to perform comma realignment. This is driven from the PCS Receive Engine during the Loss-Of-Sync state.

Note: When the core is used with the TBI, `gtx_clk` is used as the 125 MHz reference clock for the entire core.

Optional Auto-Negotiation Signal Definition

Table 7 defines the signals when the optional Auto-Negotiation is present.

Table 7: **Optional Auto-Negotiation Interface Signal Pinout**

Signal	Direction	Clock Domain	Description
link_timer_value[8:0]	Input	See Note	Used to configure the duration of the Auto-Negotiation function Link Timer. The duration of this timer is set to the binary number input into this port multiplied by 4096 clock periods of the 125 MHz reference clock (8 ns). It is expected that this signal will be tied off to a logical value. This port is replaced when using the dynamic switching mode.
an_adv_config_vector[15:0]	Input	See Note	In SGMII operating in MAC Mode, the AN_ADV register is hardwired internally to "0x4001" and this bus has no effect. For 1000BaseX and SGMII operating in PHY mode, the AN_ADV register is programmed by this bus as specified for the following bits. • Bit[0]: For 1000 BASEX-Reserved. For SGMII- Always 1 • Bits [4:1]: Reserved • Bit [5]: For 1000 BASEX- Full Duplex 1 = Full Duplex Mode is advertised 0 = Full Duplex Mode is not advertised For SGMII- Reserved • Bit [6]: Reserved • Bits [8:7]: For 1000 BASEX- Pause 0 0 No Pause 0 1 Symmetric Pause 1 0 Asymmetric Pause towards link partner 1 1 Both Symmetric Pause and Asymmetric Pause towards link partner For SGMII - Reserved • Bit [9]: Reserved • Bits [11:10]: For 1000 BASEX- Reserved For SGMII- Speed 1 1 Reserved 1 0 1000 Mb/s 0 1 100 Mb/s 0 0 10 Mb/s • Bits [13:12]: For 1000 BASEX- Remote Fault 0 0 No Error 0 1 Offline 1 0 Link Failure 1 1 Auto-Negotiation Error For SGMII- Bit[13]: Reserved

Table 7: **Optional Auto-Negotiation Interface Signal Pinout *(Cont'd)***

Signal	Direction	Clock Domain	Description
an_adv_config_vector[15:0] (Continued)	Input	See Note	Bit[12]: Duplex Mode 1 Full Duplex 0 Half Duplex • Bit [14]: For 1000 BASEX- Reserved For SGMII- Acknowledge • Bit [15]: For 1000 BASEX- Reserved For SGMII- PHY Link Status 1 Link Up 0 Link Down
an_adv_config_val	Input	See Note	This signal is valid only when the MDIO interface is present. The rising edge of this signal is the enable signal to overwrite the Register 4 contents that were written from the MDIO interface. For triggering a fresh update of Register 4 through an_adv_config_vector, this signal should be deasserted and then reasserted.
an_restart_config	Input	See Note	This signal is valid only when AN is present. The rising edge of this signal is the enable signal to overwrite Bit 9 or Register 0. For triggering a fresh AN Start, this signal should be deasserted and then reasserted.
an_interrupt	Output	See Note	When the MDIO module is selected through the GUI interface, this signal indicates an Active High interrupt for Auto-Negotiation cycle completion which needs to be cleared though MDIO. This interrupt can be enabled/disabled and cleared by writing to the appropriate PCS Management register. See the *Ethernet 1000BASE-X PCS/PMA or SGMII User Guide*. When the MDIO module is not selected, this signal indicates AN Complete, which is asserted as long as the Auto-Negotiation is complete and AN is not restarted and cannot be cleared.

Note: Signals are synchronous to the core internal 125 MHz reference clock, `userclk2` when the core is used with the device-specific transceiver, and `gtx_clk` when the core is used with TBI.

Optional Dynamic Switching Signal Pinout

Table 8 describes the additional signals present when the core is generated with the optional Dynamic Switching capability between 1000BASE-X and SGMII standards.

Table 8: **Optional Dynamic Standard Switching Signals**

Signal	Direction	Clock Domain	Description
link_timer_basex[8:0]	Input	userclk2	Used to configure the duration of the Auto-Negotiation Link Timer period when performing the 1000BASE-X standard. The duration of this timer is set to the binary number input into this port multiplied by 4096 clock periods of the 125 MHz reference clock (8 ns). It is expected that this signal will be tied off to a logical value.
link_timer_sgmii[8:0]	Input	userclk2	Used to configure the duration of the Auto-Negotiation Link Timer period when performing the SGMII standard. The duration of this timer is set to the binary number input into this port multiplied by 4096 clock periods of the 125 MHz reference clock (8 ns). It is expected that this signal will be tied off to a logical value.
basex_or_sgmii	Input	userclk2	Used as the reset default to select the standard. It is expected that this signal will be tied off to a logical value: '0' signals that the core will come out of reset operating as 1000BASE-X; '1' signals that the core will come out of reset operating as SGMII. The standard can be set following reset using the MDIO Management.

Core Latency

The standalone core does not meet all the latency requirements specified in *IEEE 802.3-2008* due to the latency of the Elastic Buffers in both TBI and device-specific transceiver versions. However, the core can be used for backplane and other applications where strict adherence to the IEEE latency specification is not a requirement.

Where strict adherence to the *IEEE 802.3-2008* specification is required, the core can be used with an Ethernet MAC core that is within the IEEE specified latency for a MAC sublayer. For example, when the core is connected to the Xilinx Tri-Mode Ethernet MAC core, the system as a whole is compliant with the overall *IEEE 802.3-2008* latency specifications.

For more information about latency, see the *Ethernet 1000BASE-X PCS/PMA or SGMII User Guide*.

Verification

The Ethernet 1000BASE-X PCS/PMA or SGMII core has been verified with extensive simulation and hardware verification.

Simulation

A highly parameterizable transaction-based test bench was used to test the core. The tests included the following:

- Register access
- Loss of synchronization
- Auto-negotiation and error handling
- Frame transmission and error handling
- Frame reception and error handling
- Clock compensation in the elastic buffers

Virtex-7, Kintex-7, Virtex-6, Virtex-5, Virtex-4 and Spartan-6 device designs incorporating a device-specific transceiver require a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed Hardware Description Language (HDL) license is required.

Hardware Verification

The core has been tested in a variety of hardware test platforms at Xilinx to represent a variety of parameterizations, including the following:

- The core used with a device-specific transceiver and performing the 1000BASE-X standard has been tested with the Xilinx Tri-Mode Ethernet MAC core, which follows the architecture shown in Figure 1. A test platform was built around these cores, including a back-end FIFO capable of performing a simple ping function, and a test pattern generator. Software running on the embedded PowerPC® processor provided access to all configuration and status registers. Version 3.0 of this core was taken to the University of New Hampshire Interoperability Lab (UNH IOL) where conformance and interoperability testing was performed.
- The core used with a device-specific transceiver and performing the SGMII standard has been tested with the LogiCORE Intellectual Property (IP) Tri-Mode Ethernet MAC core. This was connected to an external PHY capable of performing 10BASE-T, 100BASE-T, and 1000BASE-T, and the system was tested at all three speeds. This follows the architecture shown in Figure 2 and also includes the PowerPC-based processor test platform described previously.

Family Support

Table 9: **Family Support for the 1000BASE-X PCS/PMA or SGMII Core**

Device Family	LogiCORE IP Functionality						
	1000BASE-X		GMII to SGMII Bridge or SGMII to GMII Bridge			1000BASE-X and SGMII Standards with Dynamic Switching	
	With TBI	Using Device Specific Transceiver	With TBI	Using Device Specific Transceiver	Using LVDS SelectIO	With TBI	Using Device Specific Transceiver
Virtex-7	Not Supported	Supported	Not Supported	Supported	Not supported	Not Supported	Supported
Kintex-7	Supported	Supported	Supported	Supported	Not supported	Supported	Supported
Virtex-6	Supported	Supported	Supported	Supported	Supported in -2 speed grade and faster parts	Supported[1]	Supported
Virtex-5	Supported	Supported	Supported	Supported	Not supported	Supported	Supported
Virtex-4	Supported	Supported	Supported	Supported	Not supported	Supported	Supported
Spartan-6	Supported	Supported	Supported	Supported	Not supported	Supported	Supported
Spartan-3	Supported	Not supported	Supported	Not supported	Not supported	Supported	Not supported
Spartan-3E	Supported	Not supported	Supported	Not supported	Not supported	Supported	Not supported
Spartan-3A	Supported	Not supported	Supported	Not supported	Not supported	Supported	Not supported

1. Virtex-6 devices support TBI at 2.5 V only; see the Virtex-6 FPGA Data Sheet: DC and Switching Characteristics.

Device Utilization

Virtex-7, Kintex-7, Virtex-6, Virtex-5 and Spartan-6 device families contain six input LUTs; all other families contain four input LUTs. For this reason, the device utilization is listed separately. See one of the following for more information:

- Virtex-7, Kintex-7, Virtex-6, Virtex-5 and Spartan-6 Devices
- Other Device Families

Virtex-7, Kintex-7, Virtex-6, Virtex-5 and Spartan-6 Devices

Table 10 through Table 12 provide approximate utilization figures for various core options when a single instance of the core is instantiated in a Virtex-5 device.

Utilization figures are obtained by implementing the block-level wrapper for the core. This wrapper is part of the example design and connects the core to the selected physical interface.

BUFG Usage

- BUFG usage does not consider multiple instantiations of the core, where clock resources can often be shared.
- BUFG usage does not include the reference clock required for IDELAYCTRL. This clock source can be shared across the entire device and is not core specific.

1000BASE-X

Table 10: **Device Utilization for the 1000BASE-X Standard**

Parameter Values				Device Resources					
Physical Interface		MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	BUFGs	MMCMs
Transceiver	TBI								
Yes	No	Yes	Yes	330	370	470	0	1[2]	0[2]
Yes	No	Yes	No	190	215	240	0	1[2]	0[2]
Yes	No	No	N/A[1]	140	170	180	0	1[2]	0[2]
No	Yes	Yes	Yes	380	410	590	1	3[3]	0
No	Yes	Yes	No	230	280	370	1	3[3]	0
No	Yes	No	N/A[1]	190	230	315	1	3[3]	0

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. These figures are for use with GTP transceivers; GTX transceivers require three BUFGs and one DCM.
3. Only two BUFGs may be required (see the User Guide).

SGMII Bridge

Table 11: **Device Utilization for the GMII to SGMII or SGMII to GMII Bridge (Using Device Specific Transceivers or TBI)**

Parameter Values				Device Resources					
Physical Interface		MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	BUFGs	MMCMs
Transceiver	TBI								
Yes	No	Yes	Yes	430	435	665	1	1[2]	0[2]
Yes	No	Yes	No	310	330	500	1	1[2]	0[2]
Yes	No	No	N/A[1]	280	270	450	1	1[2]	0[2]
No	Yes	Yes	Yes	400	460	620	1	3[3]	0
No	Yes	Yes	No	290	360	460	1	3[3]	0
No	Yes	No	N/A[1]	240	320	410	1	3[3]	0

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. These figures are for use with GTP transceivers; GTX transceivers require three BUFGs and one DCM.
3. Only two BUFGs may be required (see the User Guide).

1000BASE-X and SGMII Standards with Dynamic Switching

Table 12: **Device Utilization for 1000BASE-X and SGMII Standards with Dynamic Switching**

Parameter Values				Device Resources					
Physical Interface		MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	BUFGs	MMCMs
Transceiver	TBI								
Yes	No	Yes	Yes	445	510	745	1	1[2]	0[2]
Yes	No	Yes	No	320	330	500	1	1[2]	0[2]
Yes	No	No	N/A[1]	280	285	440	1	1[2]	0[2]
No	Yes	Yes	Yes	405	530	700	1	3[3]	0
No	Yes	Yes	No	275	365	460	1	3[3]	0
No	Yes	No	N/A[1]	270	320	410	1	3[3]	0

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. These figures are for use with GTP transceivers; GTX transceivers require three BUFGs and one DCM.
3. Only two BUFGs may be required (see the User Guide).

Table 13: **Device Utilization for the GMII to SGMII or SGMII to GMII Bridge over Select I/O LVDS in Virtex-6 FPGAs**

Parameter Values			Device Resources					
Logical block	MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	Clock Buffers	MMCMs
I/O Bank clocking logic[2]	N/A		15	30	22	0	2 BUFIO 1 BUFR 3 BUFG	1
Per SGMII port	Yes	Yes	380	775	820	0	0	0
	Yes	No	310	640	660	0	0	0
	No	N/A[1]	265	590	615	0	0	0

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. The I/O Bank clocking logic is only required once for multiple SGMII cores that place their LVDS I/O in the same I/O Bank. Any SGMII ports that are required to be placed in additional I/O Banks require a new instantiation of the I/O Bank clocking logic for each I/O Bank utilized.

Other Device Families

Table 14 through Table 16 provide approximate utilization figures for various core options when a single instance of the core is instantiated in a Virtex-4 device. Other families have similar utilization figures, except as indicated. Utilization figures are obtained by implementing the block-level wrapper for the core. This wrapper is part of the example design and connects the core to the selected physical interface.

When the physical interface is a Virtex-4 FPGA RocketIO transceiver, utilization figures include GT11 Calibration blocks and GT11 initialization/reset circuitry.

BUFG Usage

BUFG usage does not consider multiple instantiations of the core, where clock resources can often be shared.

1000BASE-X

Table 14: **Device Utilization for the 1000BASE-X Standard**

Parameter Values				Device Resources					
Physical Interface		MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	BUFGs	DCMs
Rocket IO	TBI								
Yes	No	Yes	Yes	820	730	640	0	2[2]	0
Yes	No	Yes	No	490	500	420	0	2[2]	0
Yes	No	No	N/A[1]	430	440	360	0	2[2]	0
No	Yes	Yes	Yes	650	640	600	2	3[3]	1[4]
No	Yes	Yes	No	420	410	380	2	3[3]	1[4]
No	Yes	No	N/A[1]	350	360	330	2	3[3]	1[4]

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. For Virtex-4 devices, this includes the clock shared between the Calibration Blocks and the GT11 Dynamic Reconfiguration Port (DRP).
3. Only two BUFGs may be required (see the User Guide).
4. Spartan-3, Spartan-3E and Spartan-3A devices require two DCMs to meet TBI setup and hold times.

SGMII Bridge

Table 15: **Device Utilization for the GMII to SGMII or SGMII to GMII Bridge**

Parameter Values				Device Resources					
Physical Interface		MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	BUFGs	DCMs
Rocket IO	TBI								
Yes	No	Yes	Yes	970	780	860	1	2[2]	0
Yes	No	Yes	No	730	620	670	1	2[2]	0
Yes	No	No	N/A[1]	700	570	640	1	2[2]	0
No	Yes	Yes	Yes	800	970	630	2	3[3]	1[4]
No	Yes	Yes	No	610	830	470	2	3[3]	1[4]
No	Yes	No	N/A[1]	560	770	420	2	3[3]	1[4]

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. For Virtex-4 devices, this includes the clock shared between the Calibration Blocks and the GT11 Dynamic Reconfiguration Port (DRP).
3. Only two BUFGs may be required (see the user guide).
4. Spartan-3, Spartan-3E and Spartan-3A devices require two DCMs to meet TBI setup and hold times.

1000BASE-X and SGMII Standards with Dynamic Switching

Table 16: **Device Utilization for the 1000BASE-X and SGMII Standards with Dynamic Switching**

Parameter Values				Device Resources					
Physical Interface		MDIO Interface	Auto-Negotiation	Slices	LUTs	FFs	Block RAMs	BUFGs	DCMs
Rocket IO	TBI								
Yes	No	Yes	Yes	1100	900	940	1	2[2]	0
Yes	No	Yes	No	780	640	700	1	2[2]	0
Yes	No	No	N/A[1]	700	570	640	1	2[2]	0
No	Yes	Yes	Yes	910	1090	710	2	3[3]	1[4]
No	Yes	Yes	No	640	830	480	2	3[3]	1[4]
No	Yes	No	N/A[1]	560	770	420	2	3[3]	1[4]

1. Auto-negotiation is only available when the MDIO Interface is selected.
2. For Virtex-4 devices, this includes the clock shared between the Calibration Blocks and the GT11 Dynamic Reconfiguration Port (DRP).
3. Only two BUFGs may be required (see the User Guide).
4. Spartan-3, Spartan-3E and Spartan-3A devices require two DCMs to meet TBI setup and hold times.

Voltage Requirements

Virtex-7 devices support GMII at 3.3 V or lower only in certain parts and packages; see the 7 Series FPGAs SelectIO Resources User Guide. Virtex-6 devices support TBI or GMII at 2.5 V only; see the Virtex-6 FPGA Data Sheet: DC and Switching Characteristics. Kintex-7, Spartan-6, Virtex-5, Virtex-4 and Spartan-3 devices support TBI and GMII at 3.3 V or lower.

Speed Grades

Virtex-7, Kintex-7, Virtex-6, Virtex-5, Virtex-4 FPGAs support speed grade -1; Virtex-4 FPGA supports -10 speed grade; Spartan-6 FPGAs support -2 speed grade. All other supported Spartan devices support -4 speed grade.

References

To search for Xilinx documentation, go to http://www.xilinx.com/support/documentation/index.htm.

1. Virtex-6 FPGA User Guides
2. *Virtex-5 FPGA User Guide* (UG190)
3. *Virtex-4 FPGA User Guide* (UG070)
4. *Spartan-6 FPGA User Guide*
5. Spartan-3, Spartan-3E, Spartan-3A FPGA Data Sheets
6. *Virtex-6 FPGA GTX Transceivers, User Guide* (UG366)
7. *Virtex-4 FPGA RocketIO Multi-Gigabit Transceiver User Guide* (UG076)
8. *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* (UG196)
9. *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* (UG198)
10. *IEEE 802.3-2008* specification
11. *Serial-GMII specification*, revision 1.7

12. *1.25 Gbps 4x Asynchronous Oversampling over Virtex-6 LVDS (XAPP 881)*
13. *7 Series FPGAs SelectIO Resources User Guide (UG471)*
14. *7 Series FPGAs Transceivers User Guide (UG769)*
15. *LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII v11.2 User Guide (UG155)*

Support

For technical support, visit www.xilinx.com/support. Xilinx provides technical support for this product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation, if customized beyond that allowed in the product documentation, or if any changes are made in sections of design marked *DO NOT MODIFY*.

Ordering Information

This core is provided under the Xilinx End User License Agreement and can be generated using CORE Generator design tools v13.4 and higher. The CORE Generator tool is shipped with Xilinx ISE® Design Suite Series Development software.

This version of the Ethernet 1000BASE-X PCS/PMA or SGMII IP core does not require a license key. Contact your local Xilinx sales representative for pricing and availability of Xilinx LogiCORE IP modules and software. Information on additional LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

This table defines changes to the document.

Date	Version	Revision
9/24/04	5.0	Initial Xilinx release.
10/11/04	5.1	Document updated with corrections to Table 4 (configuration_vector[3:0] definition).
4/28/05	5.2	Updated core to v6.0, Xilinx tools v7.1i SP2, and ISE Foundation software v7.1i.
1/11/06	5.3	Updated core to v7.0, Xilinx tools v8.1i.
7/13/06	5.4	Updated core to version 7.1, Xilinx tools v8.2i.
10/23/06	5.5	Updated core to version 8.0, support for Virtex-5 LXT and Spartan 3-A devices.
2/15/07	5.6	Updated core to version 8.1, Xilinx tools 9.1i.
8/08/07	5.7	Updated core to version 9.0, Xilinx tools 9.2i.
3/24/08	5.8	Updated core to version 9.1, Xilinx tools 10.1.
4/24/09	5.9	Updated core to version 10.1, Xilinx tools 11.1, support for Virtex-5 TXT and Virtex-6 devices.
6/24/09	6.0	Updated core to version 10.2, Xilinx tools 11.2, support for Spartan-6 devices.
09/16/09	6.1	Updated core to version 10.3, Xilinx tools 11.3.
04/19/10	6.2	Updated core to version 10.4, Xilinx tools 12.1.

Date	Version	Revision
07/23/10	6.3	Updated core to version 10.5, Xilinx tools 12.2, support for SGMII in Virtex-6 devices using standard SelectIO technology logic resources.
03/01/11	6.4	Updated core to version 11.1, Xilinx tools 13.1. Added new material for Virtex-7 and Kintex-7 devices. Added SGMII PHY mode for SGMII to operate as a SGMII to GMII bridge. Additions to optional status_vector definition.
01/18/12	6.5	Summary of Core Changes • Added additional configuration vector interface for programming registers 0 and 4 • Updated core to version 11.2, Xilinx tools 13.4 • Updated that Virtex-7 does not support TBI Summary of Major Documentation Changes • Added Voltage Requirements and Speed Grade sections. • Updated IP Facts table. Moved some information in the notes to other sections. • Removed List of Acronyms. For the first occurrence of each acronym, spelled out occurrence followed by acronym. Example; Field Programmable Gate Array (FPGA) • Added paragraph to Optional PCS Management Registers section. • Updated and added signals to Table 4, Configuration Vector Definition. • Updated and added signals to Table 7, Optional Auto-Negotiation Interface Signal Pinout. • Updated Virtex-7 FPGA information in Table 9, Family Support for the 1000BASE-X PCS/PMA or SGMII Core. • Modified Bit[15:14] description in Table 2, Other Common Signals.

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