Fig: Basic organization of a hardwired control unit

Micro-programmed control unit:

In this type of control organization, the control information is stored in control memory which is programmed to start the desired sequence of micro operations. It is an alternative to the hardwired control unit. The logic of the control unit is specified by a micro program. A microprogram consists of a sequence of instructions that specify micro-operations. It is a relatively simple logic circuit that is capable of ~~of~~ sequencing through micro instructions and generating control signals to execute each micro instructions.

The set of micro instructions is stored in the contral memory. The contral address register contains the address of the next micro instruction to be read. When a micro instruction is read from the contral memory, it is transferred to the contral buffer register.

The content of the contral buffer register generates contral signals and next address information for the Sequencing Logic unit. The Sequencing Logic loads this new address into the contral address register. All this happens in one clock pulse.

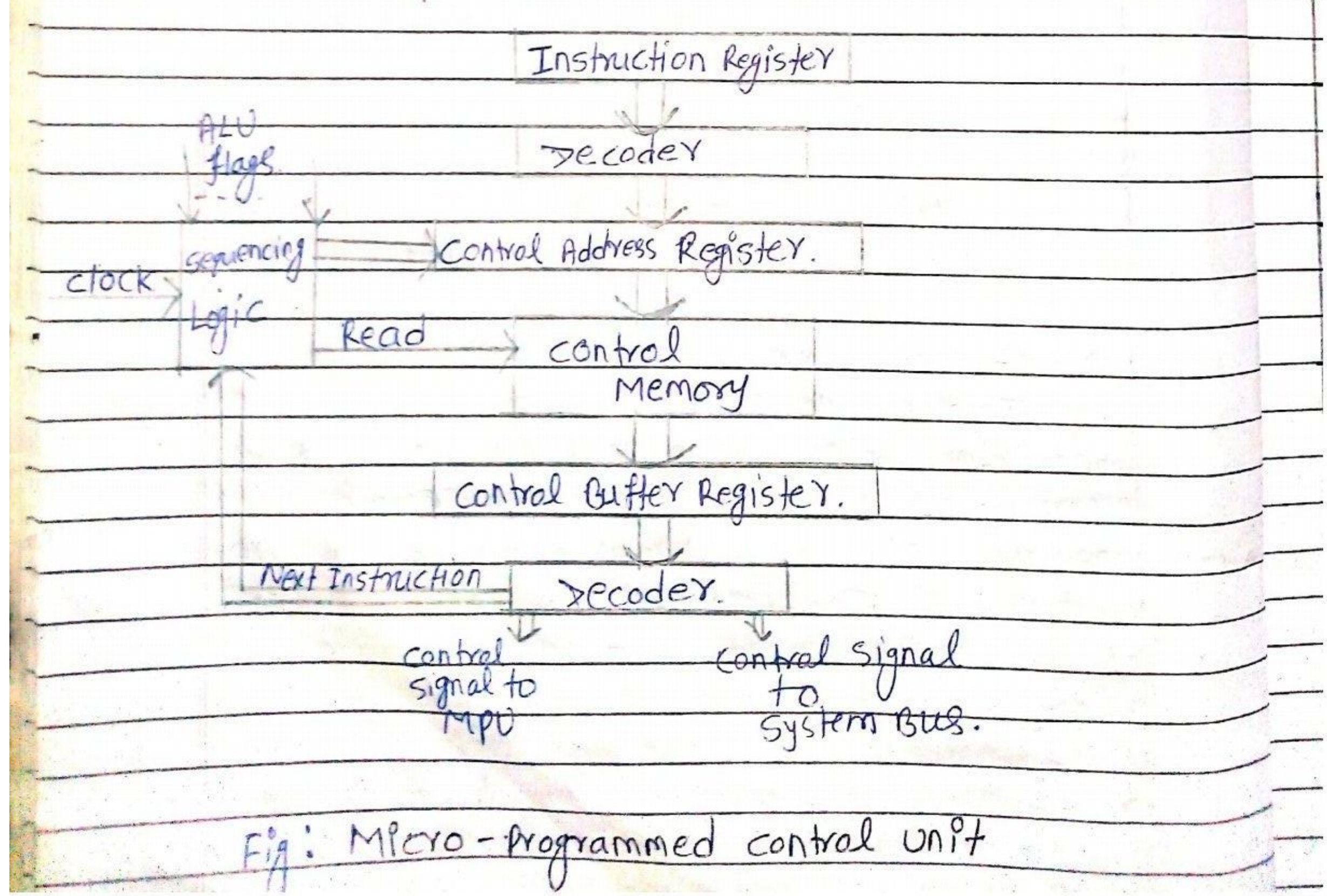

Fig: Micro-programmed control unit

T.M.L

S.No.	Attributes	Hardwired control Unit	Micro-Programmed Control Unit.
1	control functions	Implemented using hardware.	Implemented in Software.
2.	speed	Faster, as digital circuitry operate faster than control memory.	Slower than hardwire control as time is required to access the control memory.
3.	Flexibility	Not flexible, cannot accommodate new system specifications and new instructions once the circuit is designed.	More flexible, can accommodate new System specifications with small changes or addition in the micro-program.
4.	Ability to handle Large/complex instruction sets	Some what difficult	Easier
5.	Ability to support operating system & debugging.	Does not provide os support debugging and maintenance.	Provides OS Support and diagnostic features.
6	Design process	Complicated	Orderly and Systematic
7	Application	Mostly RISC processor.	Mainframes and Some microprocessors.
8.	Instruction set size	Usually below 100 instructions.	Usually above 100 instructions.
9.	Cost	Cost increases with the complexity of the control.	Cost determined by the cost of control memory; PLAS LSI devices etc. which are gradually becoming cheaper.

Conditional Branching

- The branch logic provides decision-making capabilitie in the control unit.
- The status conditions are special bits in the system that provide parameter information such as the

carry-out of an adder, the sign bit of a number the mode bits of an instruction, and input or output status conditions.

- Information in these bits can be tested and actions initiated based on their condition: whether their value is 1 or 0.
- The status bits, together with the field in the microinstruction that specifies a branch address, control the conditional branch decisions generated in the branch logic.
- The branch logic hardware may be implemented in a variety of ways. The simplest way is to test the specified condition and branch to the indicated address if the condition is met; otherwise the address register is incremented.

Mapping of Instruction

- Each instruction has its own microprogram routine stored in a given location of control memory. The transformation from the instruction code bits to an address in control memory where the routine is located is referred to as a mapping process.

- A mapping procedure is a rule that transforms the instruction code into a control memory address.

- For example, a computer with a simple instruction format as shown in Fig. 7-3 has an operation code of four bits. Assume further that the control memory has 128 words, requiring an address of seven bits. For each operation code there exists a microprogram routine

in control memory that executes the instruction.

Computer Instruction	1011	address
mapping bits.	0xxxx	00
Microinstruction address	0101100	

Fig 7-3: Mapping from instruction code to microinstruction address.

- one simple mapping process that converts the 4-bit operation code to a 7-bit address for control memory.
- This mapping consists of placing a 0 in the most significant bit of the address, transferring the four operation code bits, and clearing the two least significant bits of the control address register. This provides for each computer instruction a microprogram routine with a capacity of four microinstructions.
- If the routine needs more than four microinstructions, it can use addresses 1000000 through 1111111.
- If it uses fewer than four microinstructions, the unused memory locations would be available for other routines.