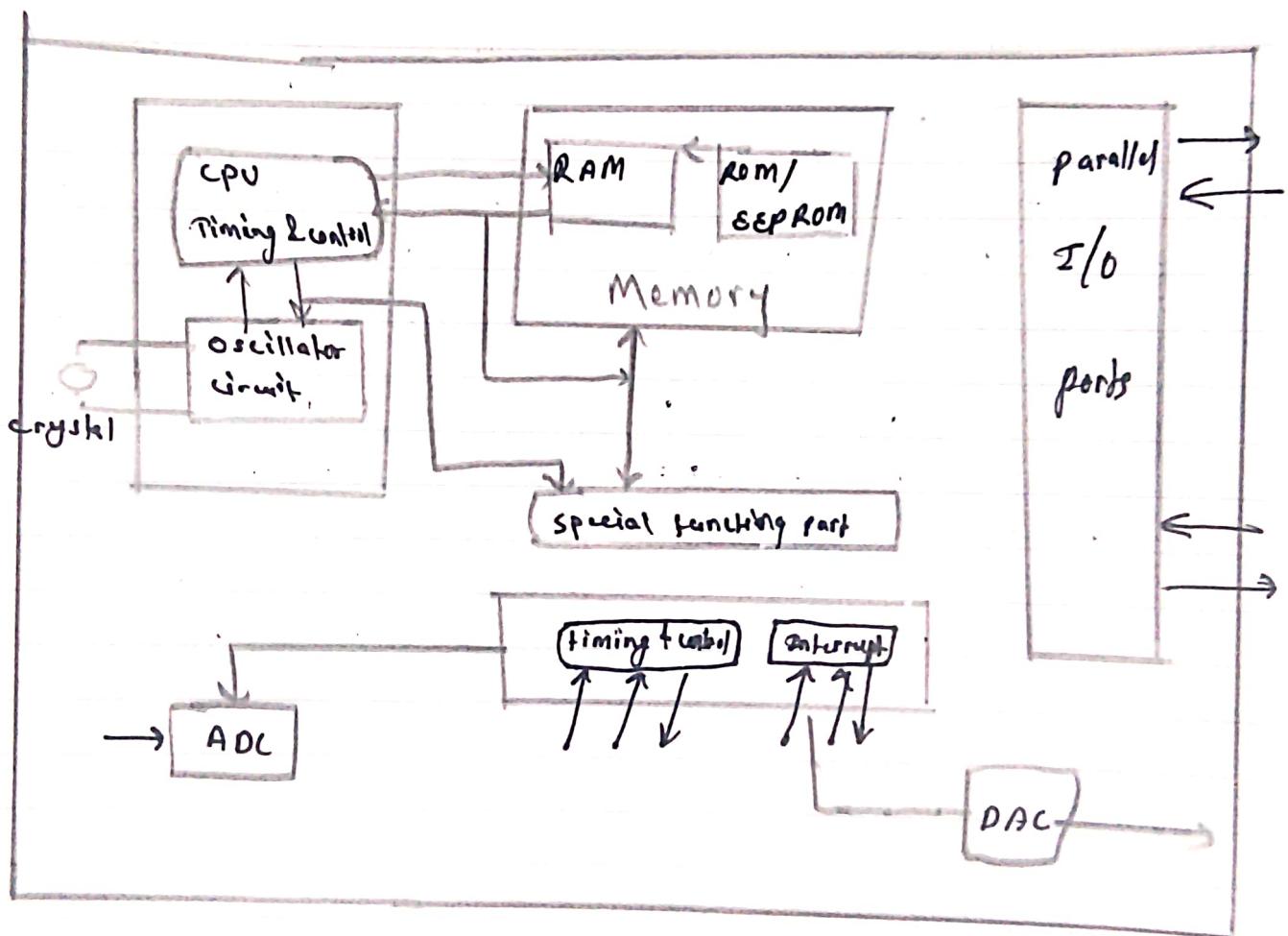


QNO:  
1

Group A

(Gobinda Samkale)

→ Microcontroller is a small & low cost micro computer which is designed to perform specific tasks of embedded systems like displaying Microwaves information, receiving remote signals. A General Microcontroller consists of processor Memory (RAM, ROM, EEPROM), serial ports & peripherals.



Block diagram of Micro controller.

Q.No 2

(Q) Why addressing modes are required in 8086? Discuss Addressing modes of 8086 in brief.

→ The term addressing modes refers to how the operand in an instruction is specified. An Addressing mode provide flexible access to Memory, Allowing you to easily access variables, arrays, records, pointer & other complex data types. So, Addressing modes are important to 8086.

• Addressing Modes of 8086 is discussed below:

① Immediate addressing Mode:

In this mode, data is present in address field of instruction. Designed like one address instruction format.

Example:

MOV AL, 35H (Move the data 35H into AL register).

② Register Addressing Mode:

In this addressing Mode, data is placed in one of 8-bit or 16 bit general purpose register. Data will be in the register of that instruction.

Example:

MOV AX, CX (Move the content of CX to AX register).

③ Register Indirect Mode:

In this addressing Mode, operand's address is placed by some registers like BX, BP, SI, DI in the instruction.

Here 8086 CPUs let you access memory indirectly through a register using the register indirect addressing mode.

MOV AX, [BX]

(Mov content of Memory location addressed by register BX to the register AX).



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#### ④ Direct addressing / Absolute addressing Mode:

The operands ~~op~~ offset is given in the instruction as an 8 bit or 16 bit displacement element. In this addressing Mode, 16 bit E.A of data is part of instruction.

Example:

ADD AL, [0301] (add the ~~op~~ offset address 0301 to AL).

#### ⑤ Indexed addressing Mode:

The operand's offset is sum of the content of a base register BX or BP to index register SI or DI.

Example:

ADD AX, [BX+SI]

#### ⑥ Implied Mode:

In this mode operand is specified in instruction itself.

In this mode data is of 8 bit or 16 bit. Which is the part of instruction.

Example:

CLC ( used to reset carry flag to zero)

③

→ STA C030H.

- STA means store Accumulator. Content of accumulator is stored in C030H.
- The opcode of STA instruction is 32H which is fetched from 4300H.
- Lower order Memory address: 30
- Higher order Memory Address: C0
- Combination of both the address are considered & content of accumulator is written in C030A.
- Let us assume Memory address for instruction & let the content of accumulator is C7H. so C7H is now stored in C030H.

Address	Mnemonics	Opcode
4300	STA C030H	32H
4200		30H
4201		C0H

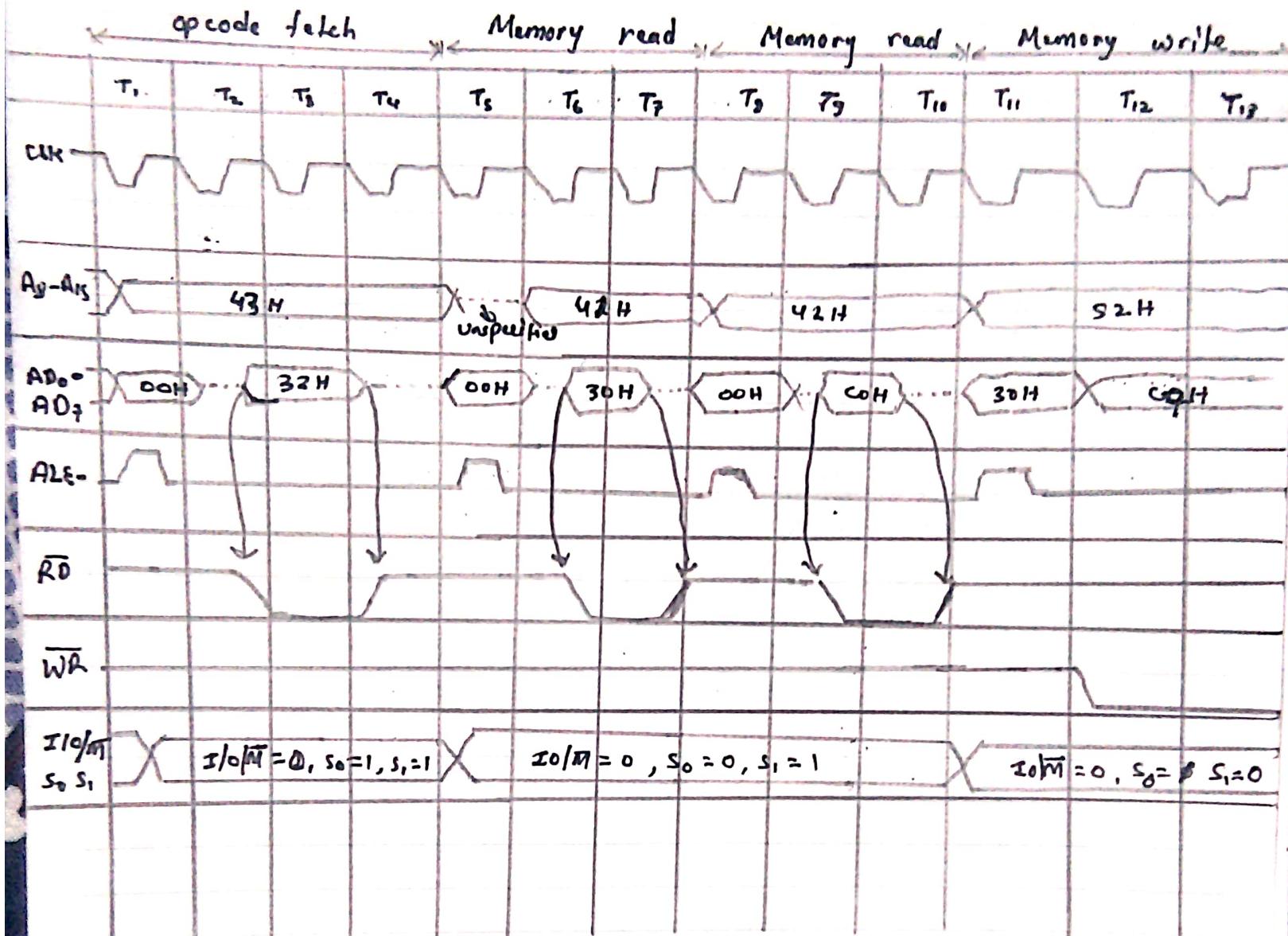


fig: Timing diagram of MVI C 030H.

## Q NO 4

- Microinstruction is a single instruction in a microcode.  
 It is the most elementary instruction in the computer,  
 such as moving the content of register to the ALU.  
 It specifies one or more microoperation in a system.  
 Sequence of microinstruction combines to form a Microprogram.

### Micro-instruction format:

3	3	3	2	2	7
F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	CD	BR	AD

F<sub>1</sub>, F<sub>2</sub>, F<sub>3</sub> = Microoperation fields

CD = Condition for Branching

BR = Branch field

AD = Address field.

Microinstruction code format is of 20 bit.

## COMPUTER HARDWARE CONFIGURATION

It consists of:

### ① Memory units:

ⓐ Main Memory → for storing instruction & data

ⓑ Control Memory → for storing Microprogram.

### ② Registers:

ⓐ processor unit registers: AL, PC, AR, DR

ⓑ Control Unit register: Control Address register (CAR)

, SBR  
(subroutine register)

### ③ Multiplexors:

- The transfer of information among register in a processor is done through a Multiplexer rather than Common Bus.



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#### ④ ALU:

- The Arithmetic, logic & shift unit perform microoperations with data from AC & DR & place result in AC.
- AR can receive information from PC or DR.
- DR can receive data from AC, PC or Memory
- PC can only receive information from AR.
- Write memory done only from DR & Read memory done only to PR.

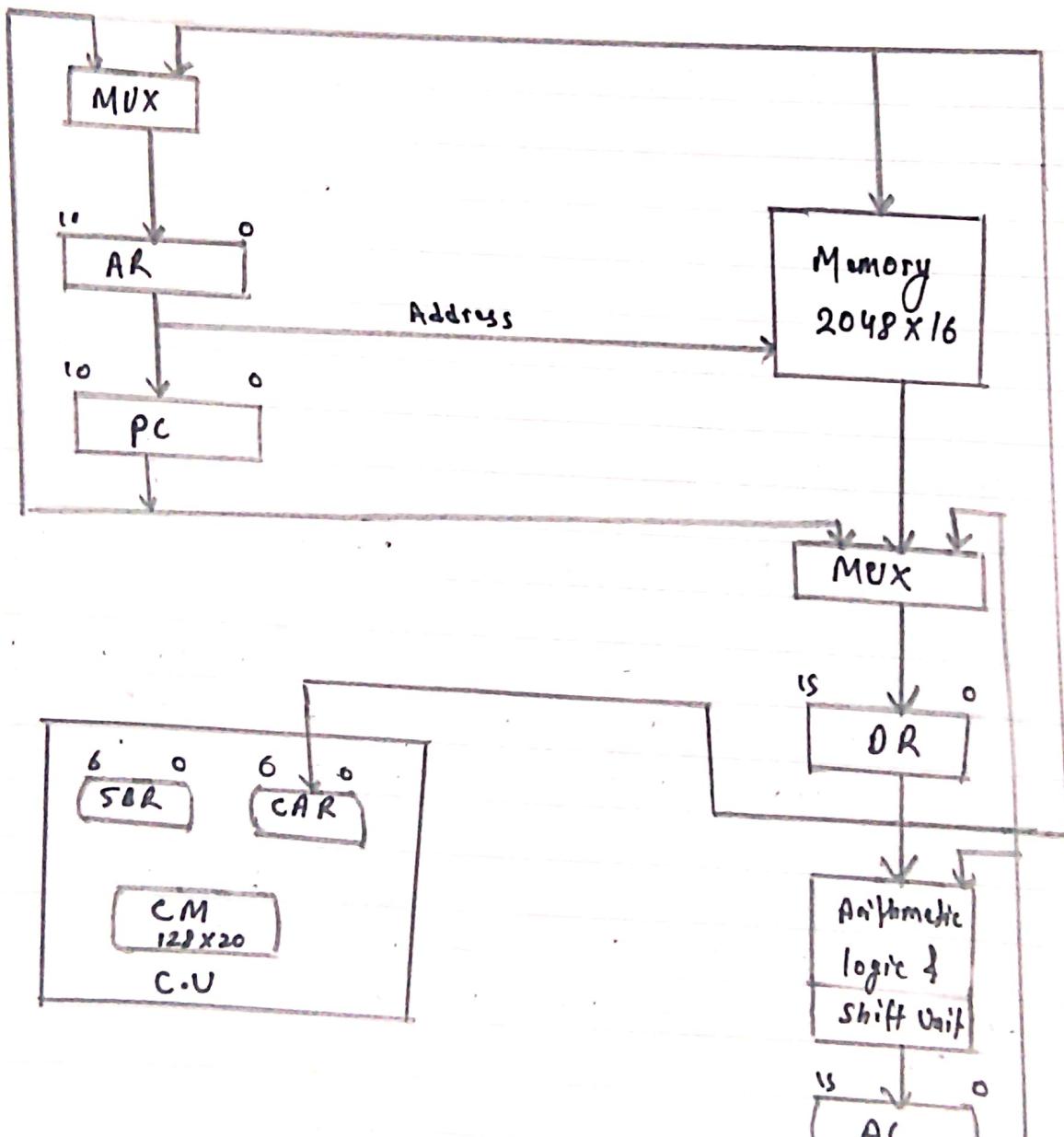


fig: Computer Hardware configuration.



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## Q/5 Register-Based organization with Block Diagram.

- Generally CPU has 7 registers. Register shows how registers are selected and how data flow from register to ALU & viceversa. A decoder is used to select particular register. The output of 2 registers is connected to 2 multiplexer to form the two Buses A & B. The selection line in each multiplexer select the input data for particular bus.

The A & B buses form the two inputs of AN ALU. The operation select lines decide the microoperation to be performed by ALU. The result of ALU Microoperation is available at output bus. The output bus is connected to input of all registers, thus By selecting a destination register it is possible to store result 'in' it.

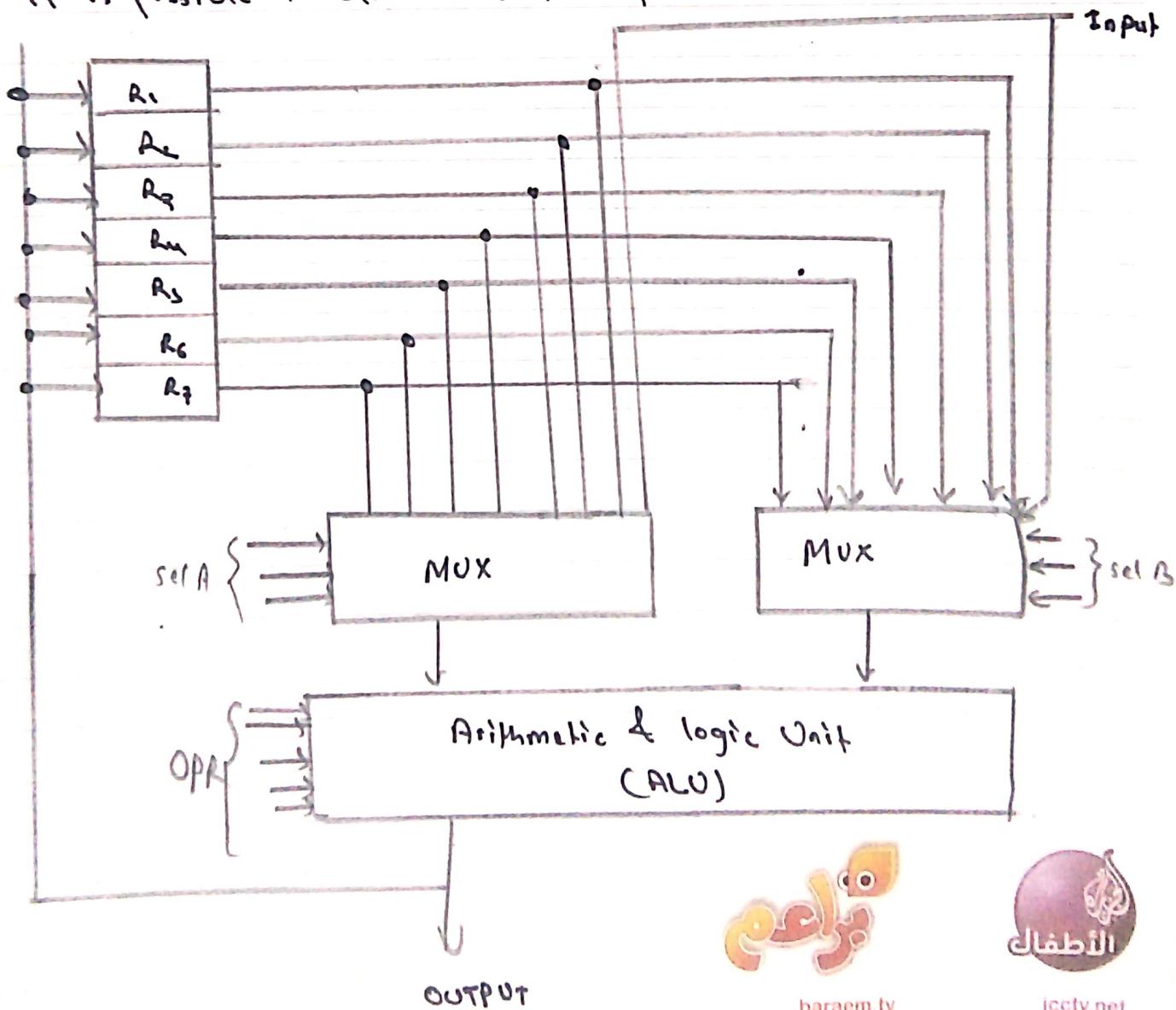


fig: Register Organization.



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Ques Define pipelining & its example. four segment pipelining.

- Pipelining is a technique of decomposing a sequential process into sub-operations, with each sub-process being executed in a special dedicated segment that operates concurrently with all segments. It's a technique to achieve parallel processing.

Some types of pipelining:

- ① Arithmetic pipelining.
- ② Instruction pipelining
- ③ Processor pipelining
- ④ Vector pipelining.
- ⑤ Dynamic pipelining

Instructions can be Executed by Overlapping fetch, decode & execute phases of an instruction cycle.

In the most general case the computer needs to process each instruction with following sequence:

- ① fetch the instruction from memory
- ② Decode the "
- ③ calculate the Effective address.
- ④ fetch the operand from E.A of the memory.
- ⑤ execute the instruction
- ⑥ store the result in the proper place.

- In four segment Instruction pipeline, Assume that Decoding of the Instruction can be combined with EA calcuation of E.A. into one segment.

- further assume execution & storing of result can be combined into one segment.



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This reduces the instruction in 4 segments.

With the help of this technique we can <sup>execute</sup> various instructions simultaneously which is pipelining.

Figure below shows the four segment pipelining.

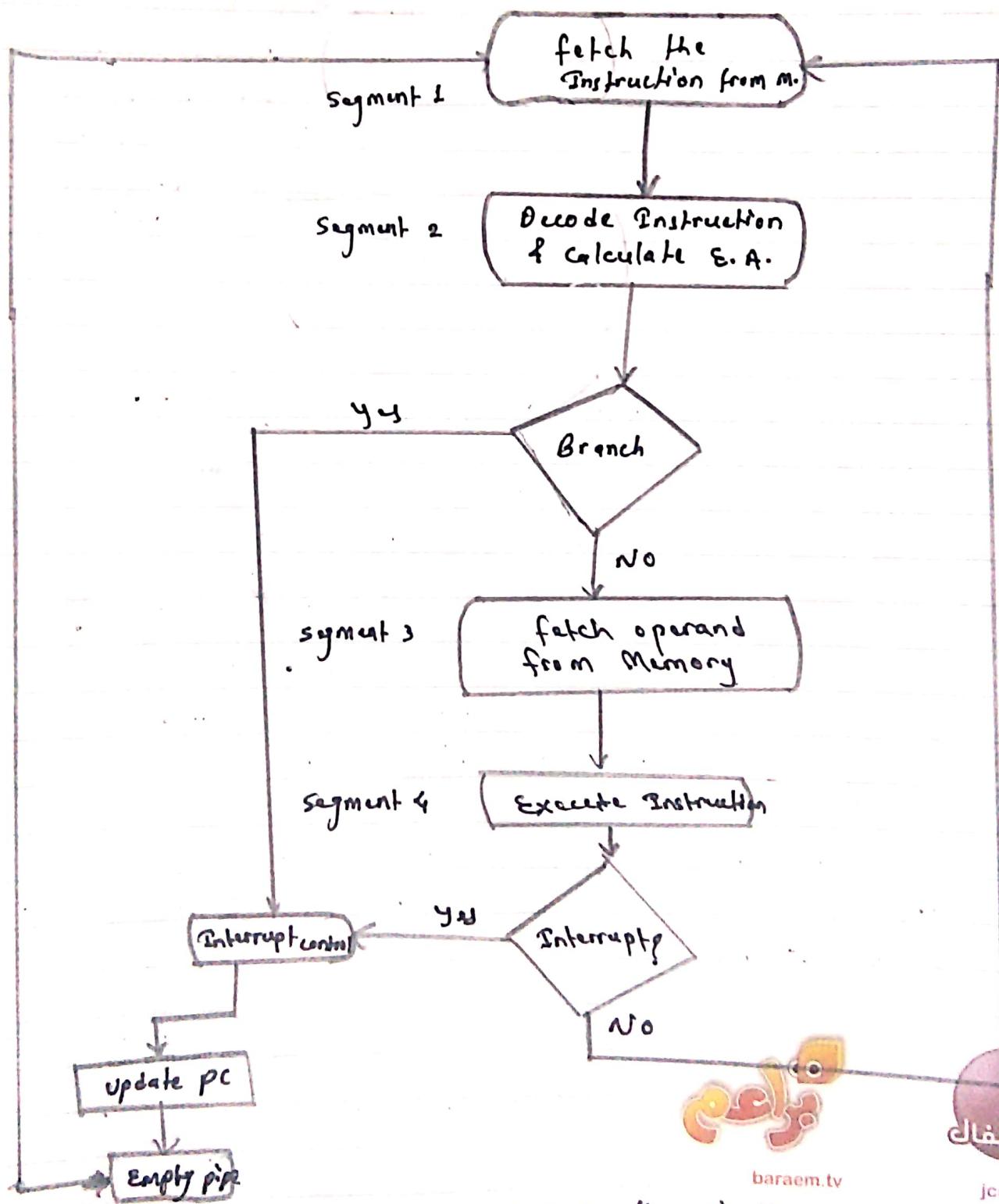
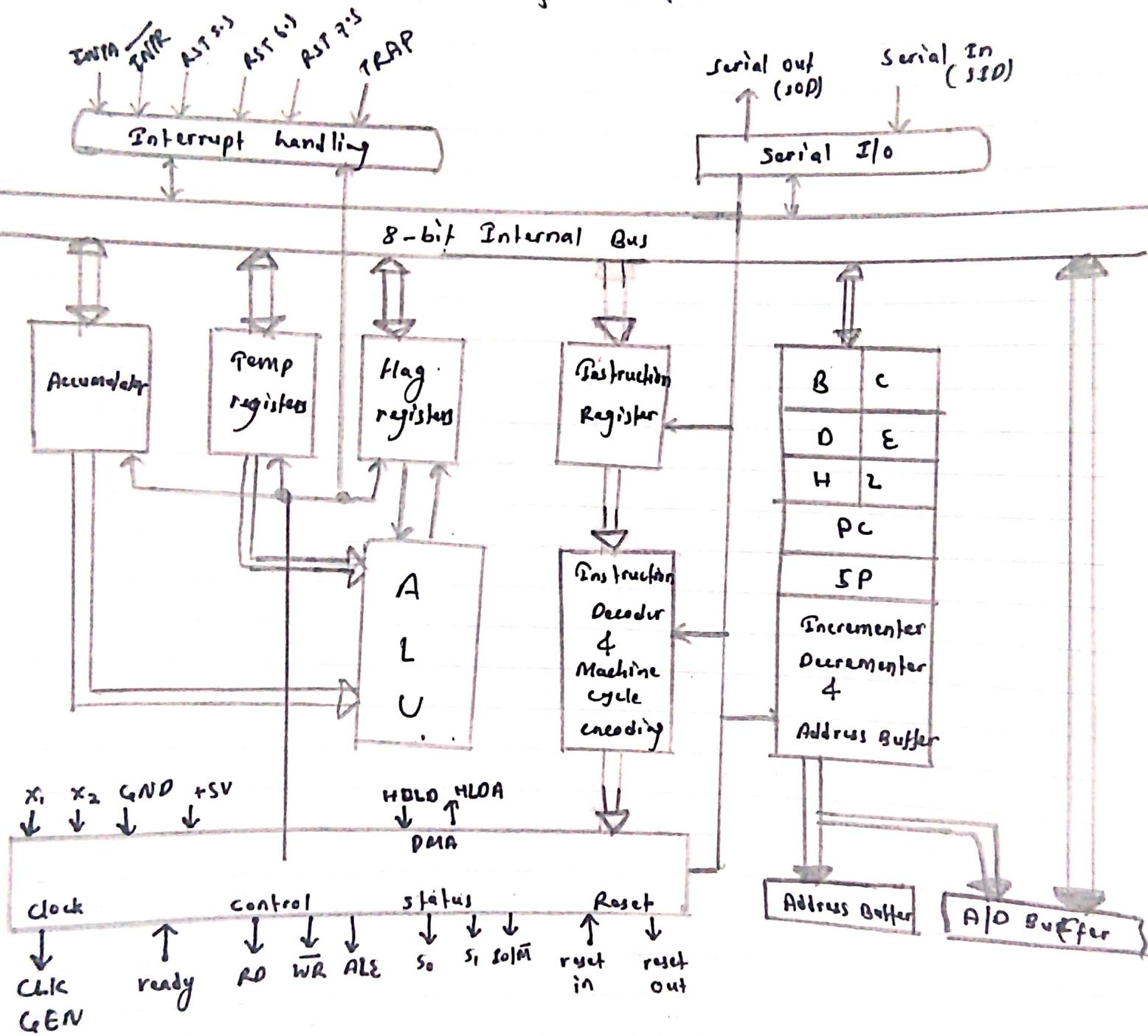


fig: four segment Instruction pipeline

### Group - C

Block Diagram of 8085



→ The architecture of 8085 Microprocessor mainly includes the timing & control Unit, ALU, decoder, IR, interrupt control, register, serial I/O & CPU.

In 8085 Signals are classified into 7 groups.

#### ① Power Supply & Frequency Signals:

- It uses 5V for power & It can run maximum frequency of 500 KHz to 3000 KHz (3MHz).

#### ② Data & Address Bus:

- In 8085 It has 8 bit data bus to carry 8 bit data or instruction & has 16 bit Address Bus to carry ~~4-bit~~ upto 16 bit address.

#### ③ Control Bus:

- It generates timing & control signals to control all the associate peripherals, Microprocessor uses control bus to process data.

#### ④ Interrupt Signal

- Interrupts are the signals generated by external devices to request the microprocessor perform a task. These signals are RST 5.5, RST 6.5, RST 7.5, TRAP, INTR, INTA.

#### ⑤ Serial I/O signals

- Serial I/O pins are used to read & write one bit data to & from peripheral devices. There are 2 serial I/O in 8085 ~~MP~~ i.e. SID & SOD.

#### ⑥ DMA signal

- It is used to write directly to RAM without intervention from processor.



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⑦

## Reset Signal

- ① Reset IN - Used to reset M/S/P. by setting PC to zero.
- ② Reset OUT - Used to reset all the connected device while the M/S/P is reset

There are various 8-bit registers.

### i) Accumulator.

- AC can hold 8-bit data. It stores result carried out by ALU.  
It is connected to internal Data Bus & ALU

### ii) Temporary registers

- It acts as temporary Memory for ALU during execution. It is of 8 bit.

### iii) General purpose register:

- There's 6 General purpose register (B, C, D, E, H, L) all are of 8-bit & can be combined to pairs (BC, DE, HL) which become 16 bit register pairs.  
HL pair can work as Memory pointer.

### iv) Instruction Register

- part of CU that holds 8-bit instructions currently being executed.

### v) flag register.

- There are various flags: sign flag, zero flag, auxiliary flag, parity flag, carry flag. These have their own uses.

### vi) stack pointer (sp):

- portion of RAM <sup>which</sup> 16 bit register used as Memory pointer.  
It maintains the address of last byte that is entered in stack.



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### Viii) Program Counter

→ A program counter is special purpose register. It stores the instruction(next) to be executed. It is 16 bit register which hold memory address.

### Viii) Incrementor / Decrementor Address latch.

→ a 16-bit register is used to increment/decrement the contents of program counter or stack pointer. It is not accessible to user.

Addressing Modes.	Details	Examples
① Immediate addressing Mode	- Here source operand is always data, can be found in instruction itself.	① MVI A 32H ② LDI H 3050
② Register Addressing Mode	→ Data to be operated is inside a register & operand is register in any instruction.	① MOV A,B ② ADD B
③ Direct addressing Mode.	→ Data to be operated is in Memory location. That M.L. is directly specified by operand.	① LD A 2050
④ Indirect addressing Mode.	→ Data to be operated by is in memory location which is indirectly specified by H-L pair.	① LD AX B
⑤ Implied addressing Mode.	→ Operand is hidden & data to be operated is available in instruction itself.	① CMA ② RRC ③ RLC



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(10)

- Interrupt is the method of creating a temporary halt during a program execution & allows peripheral devices to access the Microprocessor.

### Types of Interrupt

#### ① External Interrupt

- It is a computer system interrupt that happens as a result of outside interference, whether that is from user or, peripherals or from other hardware device through a network.

#### ② Internal Interrupt

- It's a type of interrupt that arises from illegal or erroneous use of an instruction or data. It is also called TRAP.

#### ③ Software Interrupt:

- A software interrupt is initialized by executing an instruction. It is a special call instruction that behaves like an interrupt rather than subroutine call.

# Differences Between RISC & CISC are as follows:

RISC	CISC
① Stands for Reduced instruction set computer.	① Stands for complex instruction set computer.
② Uses small & highly optimized set of instructions.	② Utilize a large, specialized & complex set of Instructions.
③ Machine oriented.	③ Programmer oriented.
④ One clock cycle required to execute instruction.	④ Multiple clock cycle is required to execute instruction.
⑤ has more registers.	⑤ has few registers.
⑥ Requires More RAM.	⑥ Requires less RAM.
⑦ Used in Hardwired control unit.	⑦ Used in Microprogrammed control unit.
⑧ Eg: Mobiles, tablets.	⑧ Eg: Desktop computer, laptops.