Explain timing Diagram of A-byte instruction (MVI A, 32H).

Resolved

8085 microprocessor timing-diagram

Lecture Notes
10-02-2021 04:41 PM

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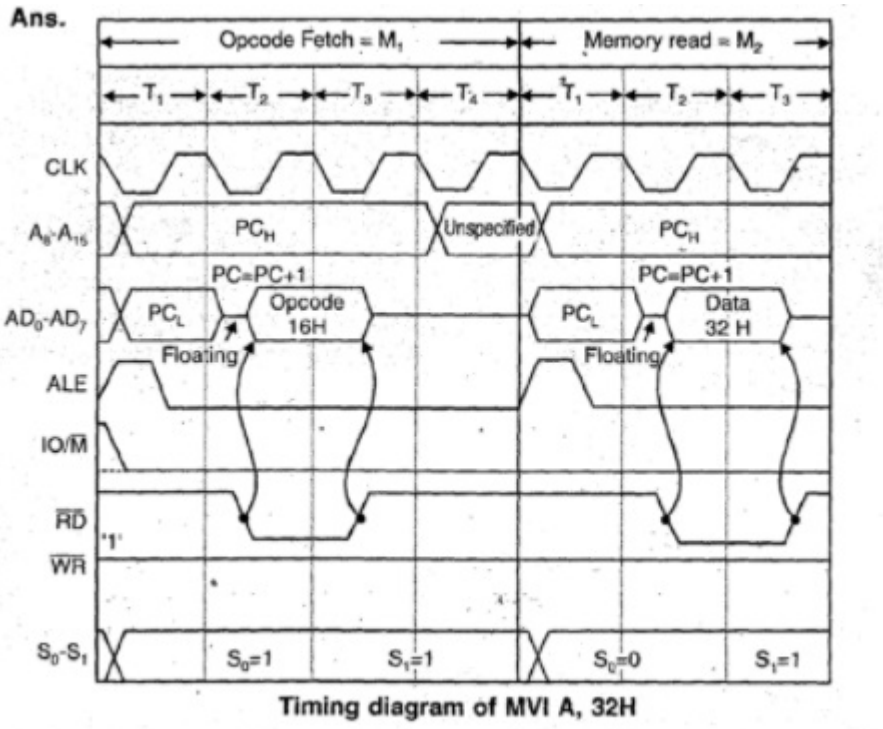
1 Answer

Mr.K Sanath Kumar Kannam
10-02-2021 Best Answer

Ans.



Timing diagram of MVI A, 32H

This is a 2 byte instruction so it requires 2 machine cycles to fetch the instruction
I Op code fetch and
2 Memory read

1 OPCODE fetch The program counter places the address on the higher order and the lower order address bus The op code at this memory location is read into the microprocessor The PC is then incremented by 1 to point to the next byte This machine cycles requires 4 T states

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2 Memory Read The data is read from the addressed memory location into the specific register The PC is again incremented by one to point to next instruction after MVI
The same timing diagram is applicable to following instructions also ACI data ADI data, ANI data CPI data, CR1 data, SUI data SBI data, XRI data MVI R, data The only difference is that op codes for these instructions are differen

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