

## Timing diagram of MVI instruction

### Related Articles

MVI B, 45

**Explanation of the command** – It stores the immediate 8 bit data to a register or memory location.

Example: MVI B, 45

Opcode: MVI

Operand: B is the destination register and 45 is the source data which needs to be transferred to the register.

'45' data will be stored in the B register.

### Algorithm –

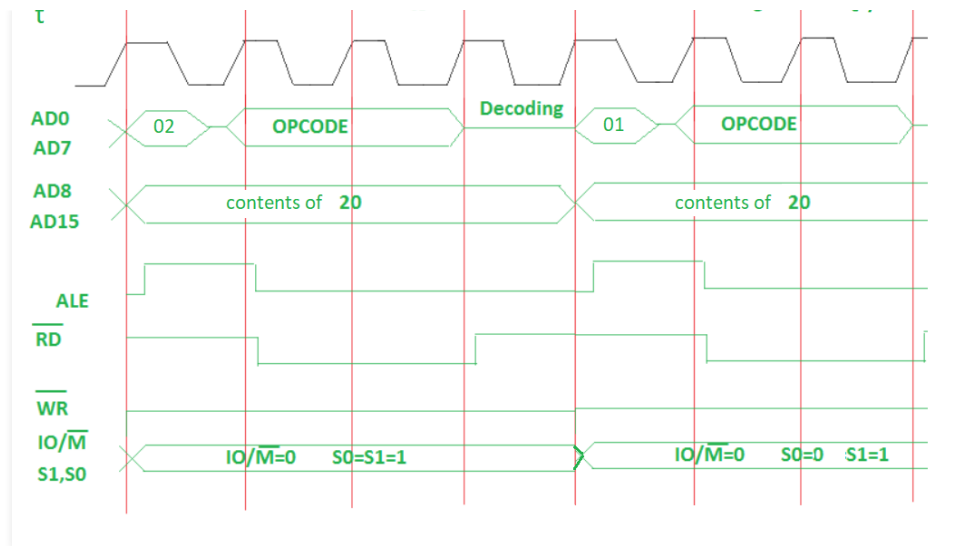
- Decide what is the opcode and what is the data. Here, opcode is 'MVI B' and data is 45.
- Assume the memory address of the opcode and the data. For example:

```
MVI B, 45
2000: Opcode
2001: 45
```

- The opcode fetch will be same in all the instructions.
- Only the read instruction of the opcode needs to be added in the successive T states.
- For the opcode fetch the IO/M (low active) = 0, S1 = 1 and S0 = 1. Also, 4 T states will be required to fetch the opcode from memory.

For the opcode read the IO/M (low active) = 0, S1 = 1 and S0 = 0. Also, only 3 T states will be required to read data from memory.





### In Opcode fetch ( t1-t4 T states ) -

- 00 – lower bit of address where opcode is stored.
- 20 – higher bit of address where opcode is stored.
- ALE – Provides signal for multiplexed address and data bus. Only in t1 it used as address bus to fetch lower bit of address otherwise it will be used as data bus.
- RD (low active) – Signal is 1 in t1 & t4, no data is read by microprocessor. Signal is 0 in t2 & t3, data is read by microprocessor.
- WR (low active) – Signal is 1 throughout, no data is written by microprocessor.
- IO/M (low active) – Signal is 0 in throughout, operation is performing on memory.
- S0 and S1 – Signal is 1 in t1 to t4 states, as to fetch the opcode from the memory.

### In Opcode read ( t5-t7 T states ) -

- 01 – lower bit of address where data is stored.
- 20 – higher bit of address where data is stored.
- ALE – Provides signal for multiplexed address and data bus. Only in t5 it used as address bus to fetch lower bit of address otherwise it will be used as data bus.
- RD (low active) – Signal is 1 in t5 as no data is read by microprocessor. Signal is 0 in t6 & t7 as data is read by microprocessor.
- WR (low active) – Signal is 1 throughout, no data is written by microprocessor.
- IO/M (low active) – Signal is 0 in throughout, operation is performing on memory.
- S0 – Signal is 0 in throughout, operation is performing on memory to read data 45.
- S1 – Signal is 1 throughout, operation is performing on memory to read data 45.