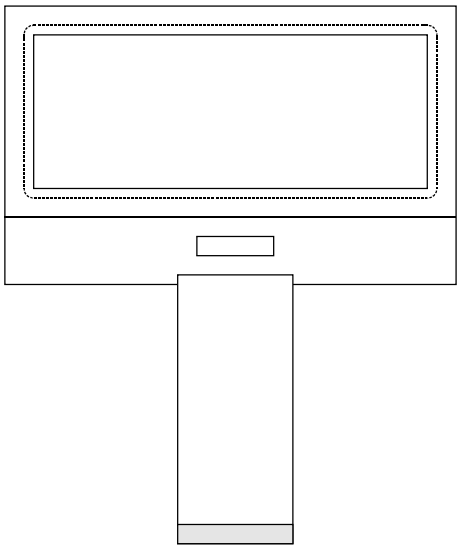
HANTRONIX

PRODUCT SPECIFICATION

HDG12864F-3

128x64 GRAPHICS
Chip-On-Glass
Parallel Interface
LCD DISPLAY MODULE



HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	**Q.A.:** JK	**REV.:** 1.0	HDG12864F-3	SHEET 1 OF 17 **DATE:** 10/17/01

1. MECHANICAL DATA

(1) Product No.		HDG12864F-3
(2) Module Size		71.0 (W)mm x 52.0 (H)mm x 2.8 (D)mm
(3) Dot Size		0.42 (W)mm x 0.51 (H)mm
(4) Dot Pitch		0.46 (W)mm x 0.56 (H)mm
(5) Resolution		128 (W) x 64 (H)
(6) Duty		1/64
(9) LCD Display Mode	FSTN:	Normally White / Positive Image
	Rear Polarizer:	Reflective
(10) Viewing Direction		6 O'clock
(11) Backlight		Excluded
(12) Weight		22.0 g(Approx.)
(13) Controller		SED1565D0B (S1D15605D00B000)

2. ABSOLUTE MAXIMUM RATINGS

(1) ELECTRICAL ABSOLUTE RATINGS

VSS=0V

	SYMBOL	MIN	MAX	UNIT	COMMENT
Power Supply for Logic	VDD−VSS	−0.3	5.5	V	
Input Voltage	VI	−0.3	VDD	V	
Static Electricity	−	−	−	−	Note 1

(2) ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE	
Ambient Temperature	MIN.	MAX.	MIN.	MAX.
	−20	70	−30	80
Humidity(Without Condensation	Note 2,3		Note 2,4	

Note 1 LCM should be grounded during handling LCM.

Note 2 Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 3 Ta ≦ 70°C : 75%RH max
Ta > 70°C : Absolute humidity must be lower than the humidity of 75%RH at 70°C

Note 4 Ta at −30°C will be < 48hrs, at 80°C will be < 120hrs

3. ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	VDD	25°C		2.7	3.3	5.5	V
Input Voltage	VIH	H level		0.7VDD	–	VDD	
	VIO	L level		−0.3	–	0.2VDD	
Recommended LCD Driving Voltage	VDD−VL6 (VLCD)	DUTY= 1/64 Bias= 1/9	−20℃	11.5	11.8	12.1	V
			0℃	11.0	11.3	11.6	
			25℃	10.5	10.8	11.1	
			50℃	10.1	10.4	10.7	
			70℃	9.8	10.1	10.4	
Power Supply Current	IDD	VDD = +5.0v		–	1.7	2.6	mA

4. OPTICAL CHARACTERISTICS

AT V_{OP}

ITEM / MODE		Cr(Contrast Ratio)										θ(Viewing Angle)		φ(Viewing Angle)	
		−20°C		0°C		25°C		50°C		70°C		25°C		25°C	
		MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	MIN.	TYP.
S	J	5.0	7.0	5.0	7.0	5.5	7.5	4.5	6.5	3.0	4.5	−	73	−	±38
NOTE		NOTE 6										NOTE 5			

NOTE :

S : TRANSFLECTIVE(NORMAL)

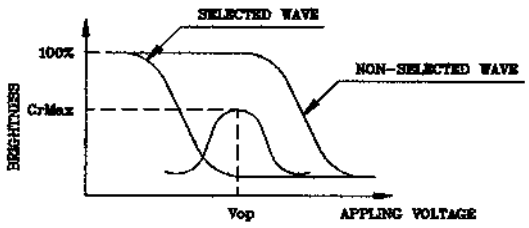
J : NORMALLY WHITE 6 O'CLOCK

AT $\phi=0°$ $\theta=0°$

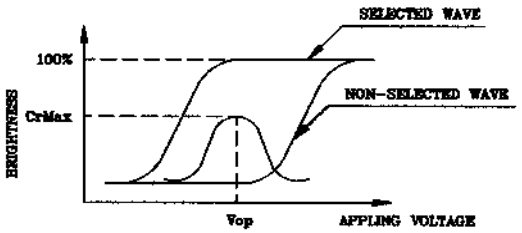
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Response Time (rise)	Tr	−20°C	2200	2700	3200	ms	NOTE 2
		0°C	450	600	750		
		25°C	150	180	210		
		50°C	65	80	95		
		70°C	40	50	60		
Response Time (fall)	Tf	−20°C	1000	1200	1400	ms	NOTE 2
		0°C	200	250	300		
		25°C	65	80	95		
		50°C	32	40	48		
		70°C	20	25	50		

(NOTE 1)

Definition of Operation Voltage(Vop)



(positive type)



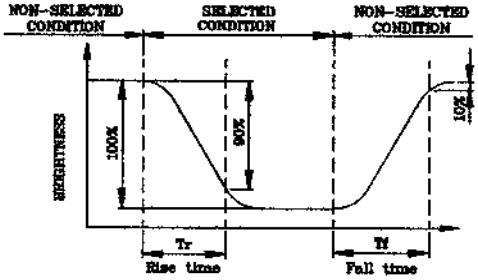
(negative type)

*Conditions

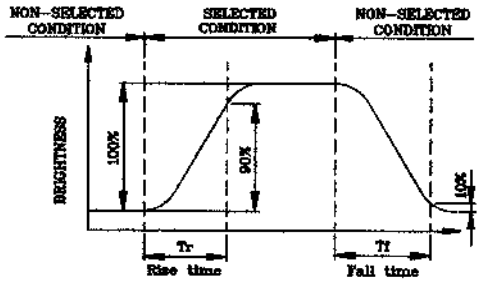
Viewing Angle : 0
Frame Frequency : 70Hz
Appling Waveform : I/N duty 1/a bias

(NOTE 2)

Definition of Response Time(Tr,Tf)



(positive type)



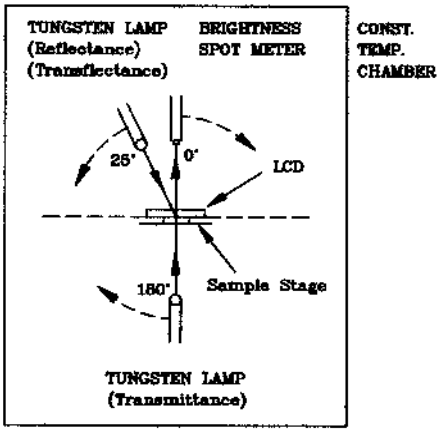
(negative type)

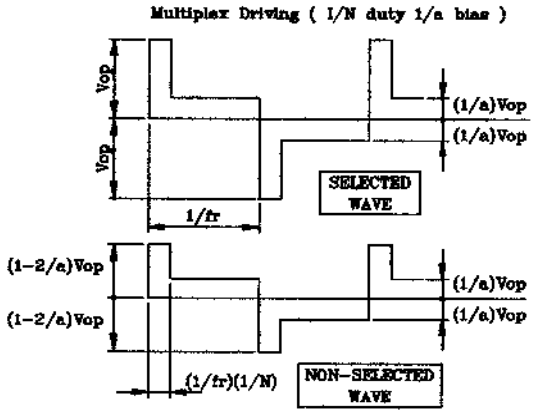
*Conditions

Operating Voltage : Vop
Viewing Angle (ϕ,θ) : (0,0)
Frame Frequency : 70Hz
Appling Waveform : I/N duty 1/a bias

(NOTE 3)

Description of Measuring Equipment and Driving Waveforms





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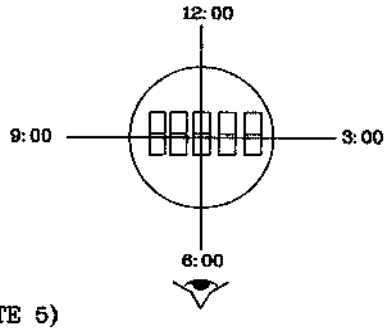
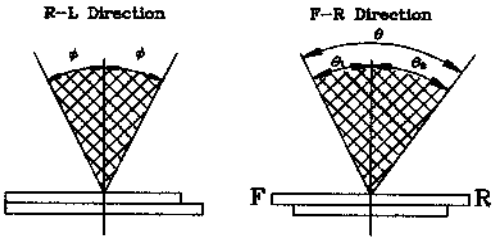
(NOTE 4)

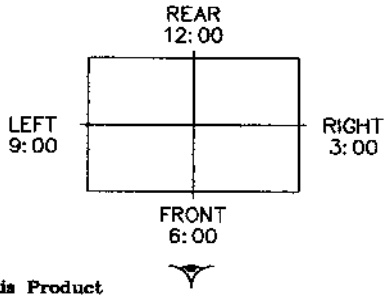
Definition of Viewing Direction



(NOTE 5)

Definition of Viewing Angle





*For This Product

The Viewing Direction Is 6 O'clock

So $\theta 1 > \theta 2$

$\theta = \theta_1 + \theta_2$

*Conditions

Operating Voltage : Vop

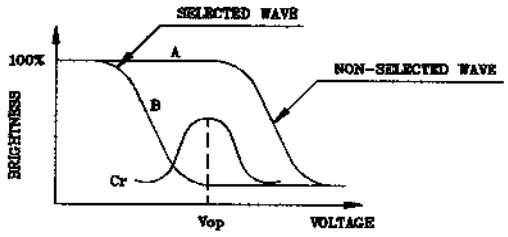
Frame Frequency : 70Hz

Appling Waveform : 1/N duty 1/a bias

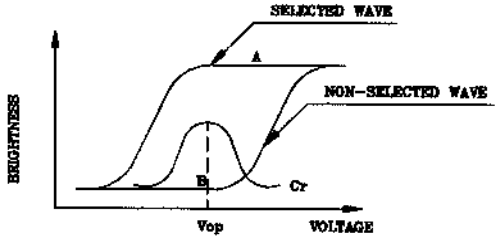
Contrast Ratio : larger than 2

(NOTE 6)

Definition of Contrast Ratio (Cr)



(positive type)



(negative type)

Contrast Ratio : Cr=A/B

*Conditions

Viewing Angle : 0

Frame Frequency : 70Hz

Appling Waveform : 1/N duty 1/a bias

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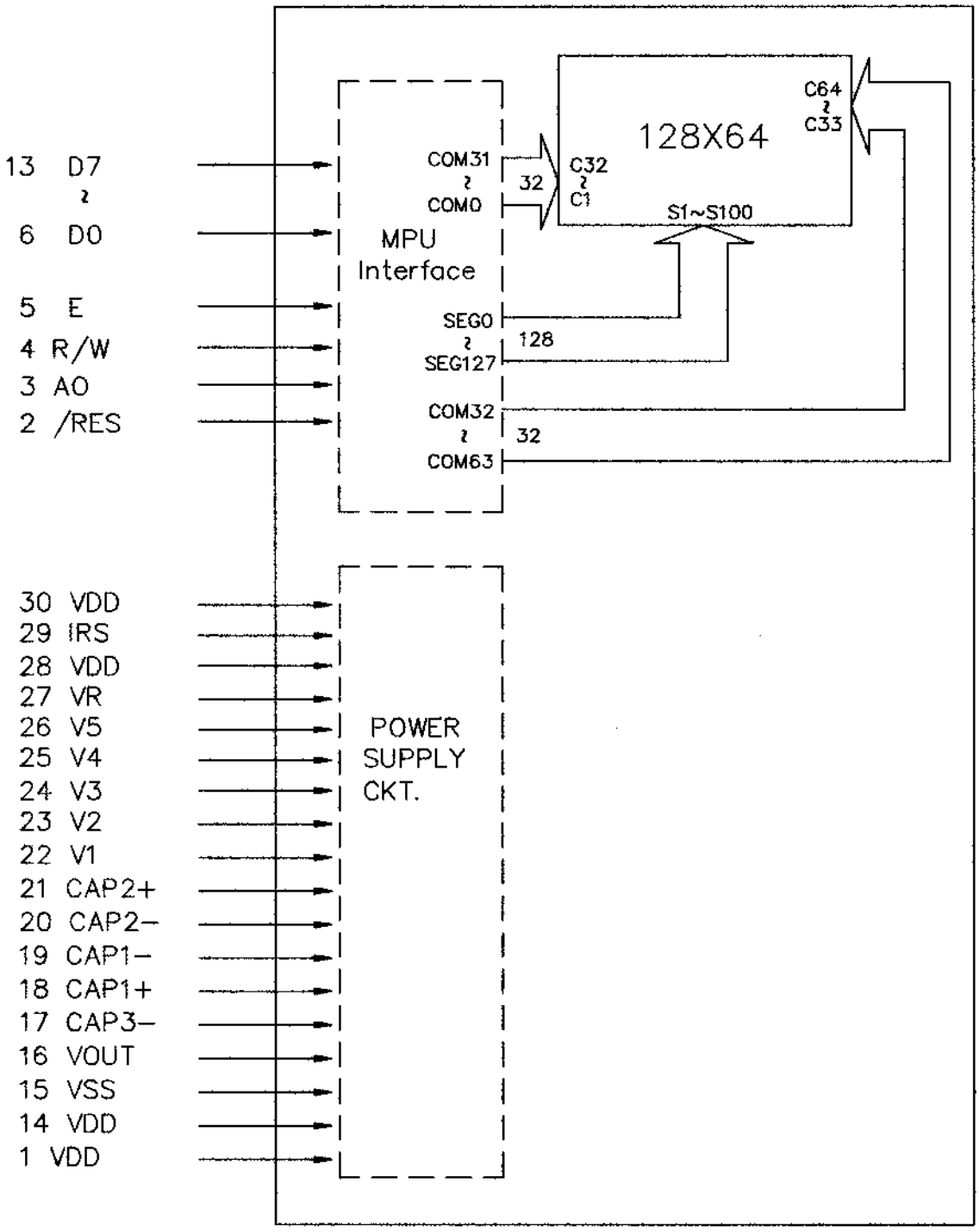
5. BLOCK DIAGRAM



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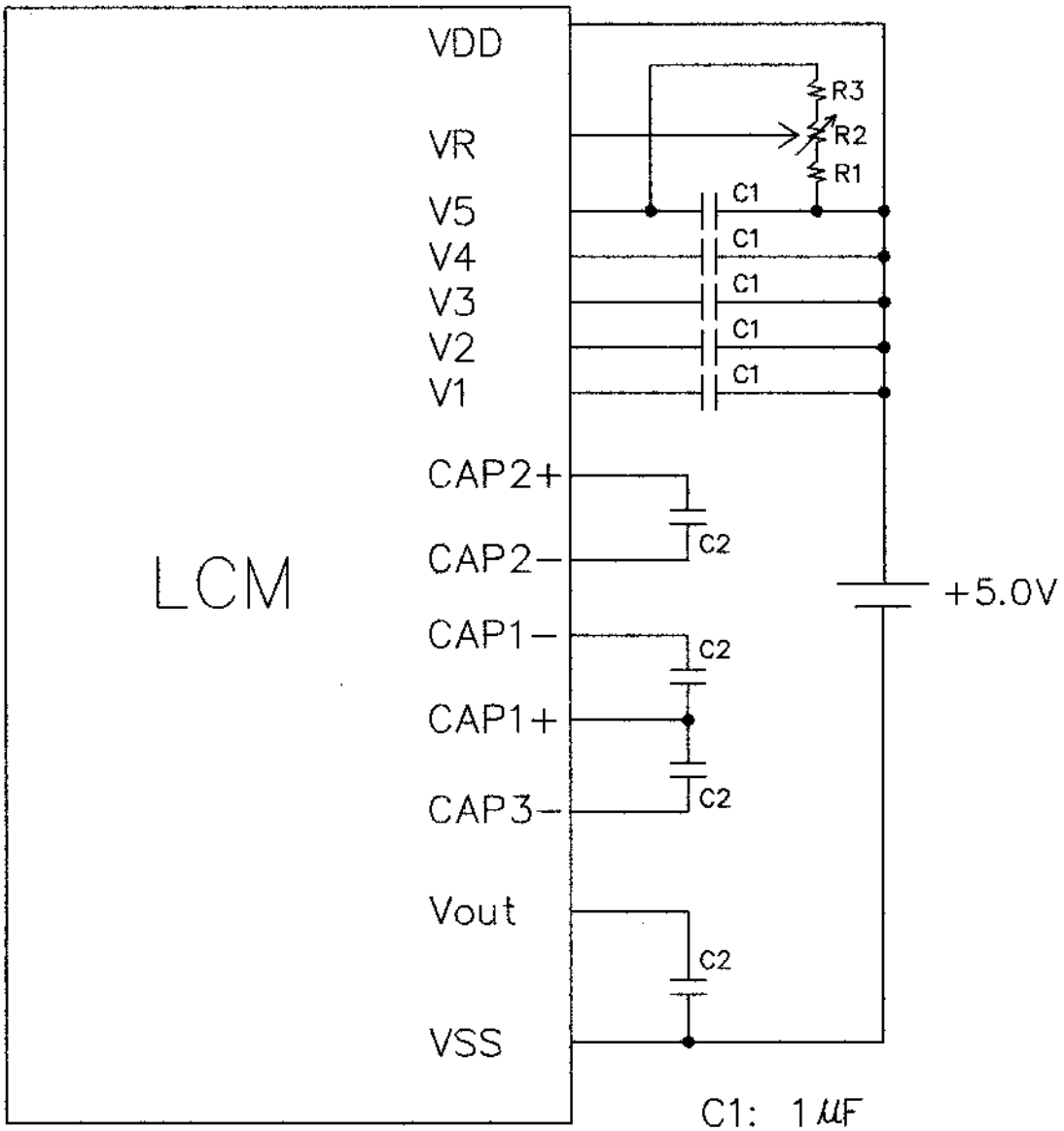
6. INTERNAL PIN CONNECTION

Pin No.	Symbol	Function
1	VDD	Power Supply for Logic
2	$\overline{RES}$	Reset Signal
3	A0	Control/Data Select Signal
4	R/W	Signal to Select Read and Write
5	E	Enable Clock Input
6	D0	Data Bus
7	D1	
8	D2	
9	D3	
10	D4	
11	D5	
12	D6	
13	D7	
14	VDD	Power Supply for Logic
15	VSS	Ground
16	Vout	DC/DC Converter Output
17	CAP3-	DC/DC Voltage Converter Capacitor 3 Nagetive Connection
18	CAP1+	DC/DC Voltage Converter Capacitor 1 Positive Connection
19	CAP1-	DC/DC Voltage Converter Capacitor 1 Negative Connection
20	CAP2-	DC/DC Voltage Converter Capacitor 2 Negative Connection
21	CAP2+	DC/DC Voltage Converter Capacitor 2 Positive Connection
22	V1	LCD Driver Supply Voltages
23	V2	
24	V3	
25	V4	
26	V5	
27	VR	Voltage Adjustment Pin.
28	VDD	Power Supply for Logic
29	IRS	"H":Use Internal Resistor ; "L":Not Use Internal Resistor
30	VDD	Power Supply for Logic

Used Cable : FPC , 0.5mm , 30 Pins , thickness 0.3mm.

Mating Connector : Molex 52689-3093 or Compatible.

7. POWER SUPPLY



C1: 1 μF
C2: 2.2 μF
R1: 240KΩ
R2: 200KΩ
R3: 1MΩ

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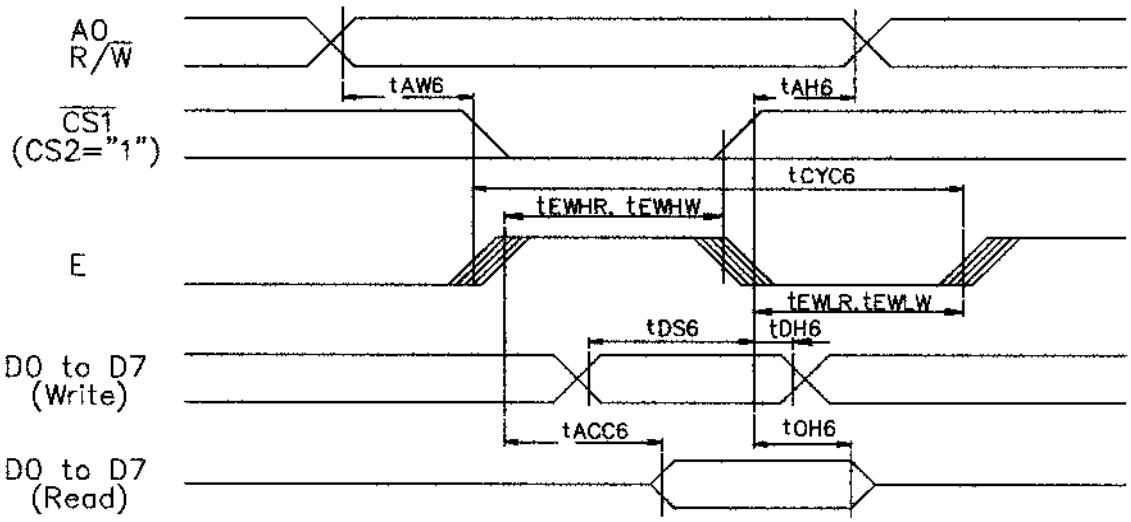
8. TIMING CHARACTERISTICS

8–1 For 6800 Series MPU



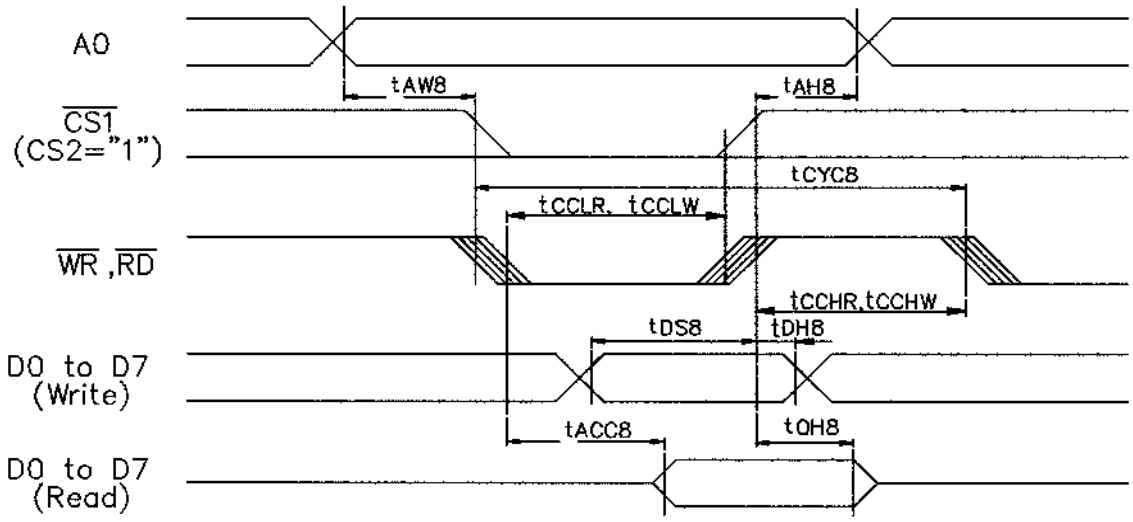
VDD=4.5~5.5V, Ta=−40~85°C

Item		Signal	Symbol	Condition	Rating Min	Rating Max	Unites
Address hold time Address setup time		A0	tAH6 tAW6		0 0	– –	ns ns
System cycle time		A0	tCYC6		166	–	ns
Data setup time Data hold time		D0 to D7	tDS6 tDH6		30 10	– –	ns ns
Access time Output disable time		D0 to D7	tACC6 tOH6	CL=100pF	– 10	70 50	ns ns
Enable H pulse time	Read Write	E	tEWHR tEWHW		70 30	– –	ns ns
Enable L pulse time	Read Write	E	tEWLR tEWLW		30 30	– –	ns ns

VDD=2.7~4.5V, Ta=−40~85°C

Item		Signal	Symbol	Condition	Rating Min	Rating Max	Unites
Address hold time Address setup time		A0	tAH6 tAW6		0 0	– –	ns ns
System cycle time		A0	tCYC6		300	–	ns
Data setup time Data hold time		D0 to D7	tDS6 tDH6		40 15	– –	ns ns
Access time Output disable time		D0 to D7	tACC6 tOH6	CL=100pF	– 10	140 100	ns ns
Enable H pulse time	Read Write	E	tEWHR tEWHW		120 60	– –	ns ns
Enable L pulse time	Read Write	E	tEWLR tEWLW		60 60	– –	ns ns

8-2 For 8080 Series MPU



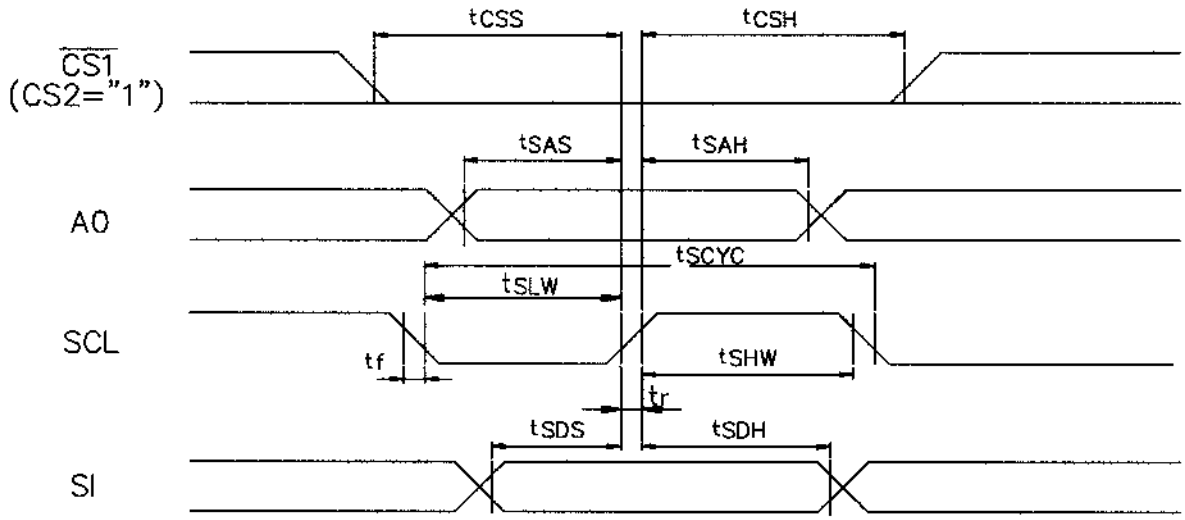
VDD=4.5~5.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating Min	Rating Max	Unites
Address hold time	A0	tAH8		0	–	ns
Address setup time		tAW8		0	–	ns
System cycle time	A0	tCYC8		166	–	ns
Control L pulse width (WR)	WR	tCCLW		30	–	ns
Control L pulse width (RD)	RD	tCCLR		70	–	ns
Control H pulse width (WR)	WR	tCCHW		30	–	ns
Control H pulse width (RD)	RD	tCCHR		30	–	ns
Data setup time	D0 to D7	tDS8		30	–	ns
Data hold time		tDH8		10	–	ns
RD access time	D0 to D7	tACC8	CL=100pF	–	70	ns
Output disable time		tOH8		5	50	ns

VDD=2.7~4.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating Min	Rating Max	Unites
Address hold time	A0	tAH8		0	–	ns
Address setup time		tAW8		0	–	ns
System cycle time	A0	tCYC8		300	–	ns
Control L pulse width (WR)	WR	tCCLW		60	–	ns
Control L pulse width (RD)	RD	tCCLR		120	–	ns
Control H pulse width (WR)	WR	tCCHW		60	–	ns
Control H pulse width (RD)	RD	tCCHR		60	–	ns
Data setup time	D0 to D7	tDS8		40	–	ns
Data hold time		tDH8		15	–	ns
RD access time	D0 to D7	tACC8	CL=100pF	–	140	ns
Output disable time		tOH8		10	100	ns

8-3 For Series Interface



VDD=4.5~5.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating Min	Rating Max	Unites
Serial Clock Period	SCL	tSCYC		200	–	ns
SCL "H" pulse width		tSHW		75	–	ns
SCL "L" pulse width		tSLW		75	–	ns
Address setup time	A0	tSAS		50	–	ns
Address hold time		tSAH		100	–	ns
Data setup time	SI	tSDS		50	–	ns
Data hold time		tSDH		50	–	ns
CS-SCL time	CS	tCSS		100	–	ns
		tCSH		100	–	ns

VDD=2.7~4.5V, Ta=-40~85°C

Item	Signal	Symbol	Condition	Rating Min	Rating Max	Unites
Serial Clock Period	SCL	tSCYC		250	–	ns
SCL "H" pulse width		tSHW		100	–	ns
SCL "L" pulse width		tSLW		100	–	ns
Address setup time	A0	tSAS		150	–	ns
Address hold time		tSAH		150	–	ns
Data setup time	SI	tSDS		100	–	ns
Data hold time		tSDH		100	–	ns
CS-SCL time	CS	tCSS		150	–	ns
		tCSH		150	–	ns

8-4 SED1565 Series Commands

Command	Command Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)Display data write	1	1	0	Write data								Writes to the display RAM
(7)Display data read	1	0	1	Read data								Reads from the display RAM
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all point ON
(11)LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio SED1565***....0: 1/9, 1: 1/7 SED1566***....0: 1/8, 1: 1/6 SED1567***....0: 1/6, 1: 1/5
(12)Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)End	0	1	0	1	1	1	0	1	1	1	0	Clearv read/modify/write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)V5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V5 output voltage electronic volume register
(19)Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static indicator register set	0	1	0	*	*	*	*	*	*	mode		Set the flashing mode
(20)Power saver												Display OFF and display all points ON compound command
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command
(23)Test mode reset	0	1	0	1	1	1	1	0	0	0	0	Enter during the refresh sequence.

(Note)*: disabled data

9. RELIABILITY TEST

NO	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	70°C	120HR		Appearance without defect	
2	Low Temp. Storage	−20°C	120HR		Appearance without defect	
3	High Temp. & High Humi. Storage	40°C 90%RH	120HR		Appearance without defect	
4	Thermal Shock	−20°C, 30min → 25°C.5min → 70°C, 30min → 25°C.5min (1cycle)			Appearance without defect	5 cycles

NOTE:

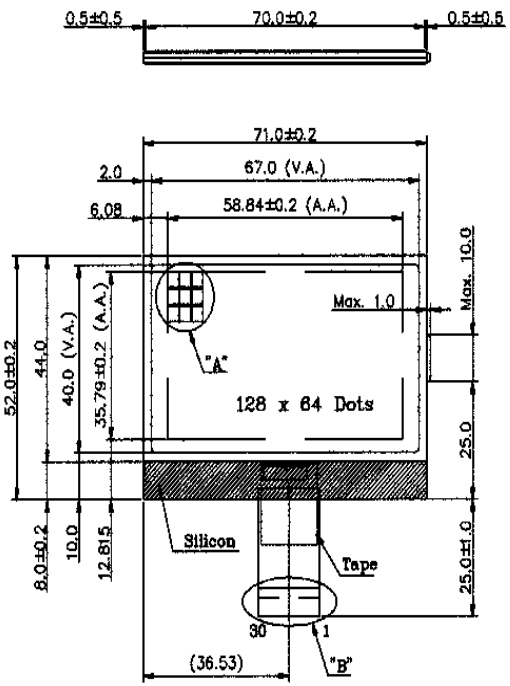
- SAFETY
  1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
  2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

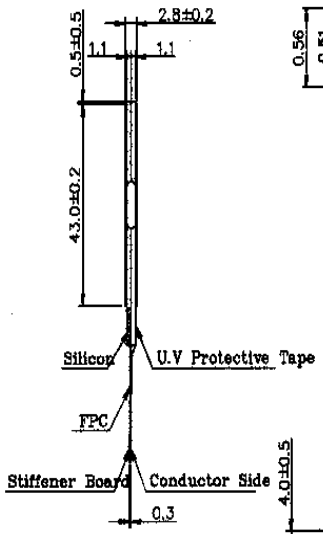
- HANDLING
  1. Avoid static electricity which can damage the CMOS LSI.
  2. Do not remove the panel or frame from the module.
  3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
  4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
  5. Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

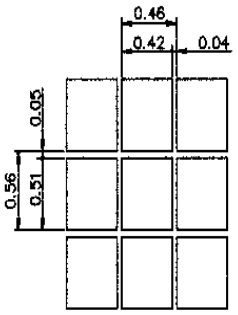
- STORAGE
  1. Store the panel or module in a dark place where the temperature is 25°C±5°C and the humidity is below 65% RH.
  2. Do not place the module near organics solvents or corrosive gases.
  3. Do not crush, shake, or jolt the module.

- TERMS OF WARRANT
  1. Acceptance inspection period
     The period is within one month after the arrival of contracted commodity at the buyer's factory site.
  2. Applicable warrant period
     The period is within twelve months since the date of shipping out under normal using and storage conditions.
  3. Strengthen Q.C inspection on the light guide, especially the hooks & pinholes.

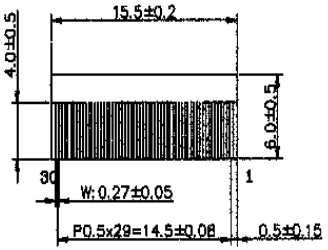
Pin No	Symbol	Function
1	VDD	Power Supply for Logic
2	RES	Reset Signal
3	A0	Control/Data Select Signal
4	R/W	Signal to Select Read and Write
5	E	Enable Clock Input
6	D0	Data Bus
7	D1	
8	D2	
9	D3	
10	D4	
11	D5	
12	D6	
13	D7	
14	VDD	Power Supply for Logic
15	VSS	Ground
16	Vout	DC/DC Converter Output
17	CAP3-	DC/DC Voltage Converter Capacitor 3 Negative Connection
18	CAP1+	DC/DC Voltage Converter Capacitor 1 Positive Connection
19	CAP1-	DC/DC Voltage Converter Capacitor 1 Negative Connection
20	CAP2-	DC/DC Voltage Converter Capacitor 2 Negative Connection
21	CAP2+	DC/DC Voltage Converter Capacitor 2 Positive Connection
22	V1	LCD Driver Supply Voltages
23	V2	
24	V3	
25	V4	
26	V5	
27	VR	Voltage Adjustment Pin.
28	VDD	Power Supply for Logic
29	IRS	"H": Use Internal Resistor ; "L" : Not Use Internal Resistor
30	VDD	Power Supply for Logic







Detail "A"
(Scale 30:1)



Detail "B"
(Scale 3:1)

GENERAL TOLERANCE LIST

DIMENSION	TOLERANCE
L ≦ 6	±0.25 (mm)
6 < L ≦ 18	±0.3 (mm)
18 < L ≦ 50	±0.4 (mm)
50 < L ≦ 125	±0.5 (mm)
125 < L	±0.6 (mm)
ANGLE	±1° (DEG)

Notes :

1. Resolution : 128 x 64 Dots
2. Controller IC : "EPSON" SED 1565D0B
3. Thickness of Glass : 1.1mm

SHEET 17 OF 17

DATE: 10/17/01

HDG12864F-3

REV.: 1.0

Q.A.: JK

HANTRONIX, INC.
10080 BUBB RD.
CUPERTINO, CA 95014