~\MobaXterm\home\QuartusProjects\Homework\hw8\hw8_serial_parser\serial_tb.vhd

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use work.all;
4
5  entity serial_tb is
6  end serial_tb;
7
8  architecture tb of serial_tb is
9
10     constant period_c   : time := 10 ns;
11     signal clock_net    : std_logic;
12     signal RST_net : std_logic;
13     signal serial_net : std_logic;
14     signal wave_out_net : std_logic;
15
16     component serial
17         port (
18             clock : in std_logic;
19             RST : in std_logic;
20             serial : in std_logic;
21             wave_out : out std_logic
22         );
23     end component serial;
24
25
26 begin
27
28     serial_instance: serial
29     port map(
30         clock => clock_net,
31         RST => RST_net,
32         serial => serial_net,
33         wave_out => wave_out_net
34     );
35
36     tb_clk: process
37     begin
38         clock_net <= '1';
39         wait for period_c / 2;
40         clock_net <= '0';
41         wait for period_c / 2 ;
42     end process tb_clk;
43
44     tb_p: process
45     begin
46         serial_net <= '0';
47         RST_net <= '1';
48         wait for 4 * period_c;
49         RST_net <= '0';
50
51         wait for period_c;
52
```

```
53          serial_net <= '1';
54          wait for 4 * period_c;
55
56          serial_net <= '0';
57          wait for 2 * period_c;
58
59          serial_net <= '1';
60          wait for 2 * period_c;
61
62          serial_net <= '1';
63          wait for 3 * period_c;
64
65          serial_net <= '0';
66          wait for 5 * period_c;
67
68          assert false
69          report "End of TestBench"
70          severity failure;
71
72      end process tb_p;
73
74  end tb;
```