Lab 2 - 2-Bit Comparator

Joey Macauley and Ian Flury

CPEN 430 - Digital System Design

September 12, 2023

Table of Contents:

Overview:

The circuit implemented by this VDHL code takes two 2-bit unsigned numbers and compares them, checking for equality. There are two inputs “A” and “B” of type std_logic_vector. These numbers are given as input to the system by switches SW[0-3].The circuit indicates whether A is greater than, equal to, or less than B by setting three outputs (AGTB, AEQB, ALTB) high. These outputs are wired to LEDs (LEDG0, LEDG1, LEDG2) respectively. The circuit will also display the characters “AGTB,” “AEQB,” and “ALTB” on the seven segment displays.

Analysis:

Reviewing the Quartus Analysis and Synthesis Summary tells us that our circuit uses a total of 35 pins, and 3 logic elements. By examining the logic analyzer output created in ModelSim by our test bench file (cmp_tb) we can conclude that our circuit successfully realizes the logic we want to implement. There was no timing analysis for this lab.