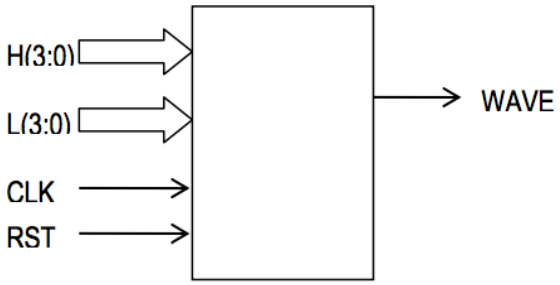
# *CPEN430 - Problem Set*

*Problem #1*

Use VHDL to design and test a programmable square wave generator. The circuit must be able generate a square wave with variable HIGH and LOW intervals, and must be completely synchronous except for the reset signal RST. The duration of the intervals are specified by two 4-bit signals H and L, representing two positive integer values. The high and low intervals are H*100 ns and L*100ns respectively. Assume the clock CLK has a period of 20 ns.




Make sure to submit:

1. VHDL code for both design and testbench.
2. The waveforms used for testing the unit. Comment the waveforms and make sure to illustrate that the system works as expected
3. The synthesized Hardware (use RTL viewer)

*Problem #2*

Use VHDL to design and test a circuit that takes as input a serial bit stream and outputs a '1' whenever the sequence "111" occurs. Overlaps must also be considered, that is, if …001111110… occur than the output should remain active for **four** consecutive clock cycles.

Make sure to submit:

1. ASM diagram
2. VHDL code for both design and testbench.
3. The waveforms used for testing the unit. Comment the waveforms and make sure to illustrate that the system works as expected
4. The synthesized Hardware (use RTL viewer)