Lab. 4

Design a circuit that 1) counts the number of times the key-3 push-button is pressed 2) display the count on the board's LCD, 3) uses the push-button key-0 to reset the system. The default value displayed on the LCD before key-3 is pressed for the first time is 0. If the number of times the key-3 push-button is pressed exceeds ten, the system should display the text:

YOU PUSHED TOO
MANY TIMES

On the DE2-115 board the FPGA controls the LCD via the interface shown in figure:

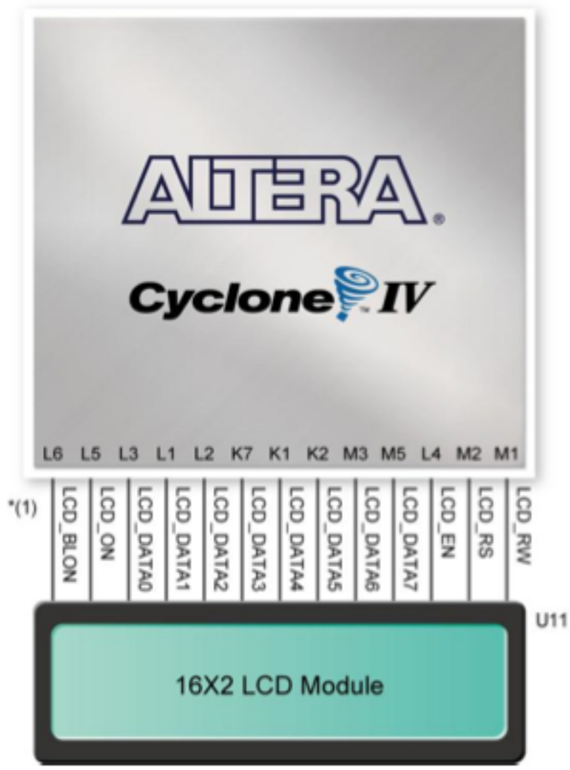

Figure 4-12 Connections between the LCD module and Cyclone IV E FPGA

*(1): Note the current LCD modules used on DE2-115 boards do not have backlight. Therefore the LCD_BLON signal should not be used in users' design projects.

Table 4-6 Pin Assignments for LCD Module

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LCD_DATA[7]	PIN_M5	LCD Data[7]	3.3V
LCD_DATA[6]	PIN_M3	LCD Data[6]	3.3V
LCD_DATA[5]	PIN_K2	LCD Data[5]	3.3V
LCD_DATA[4]	PIN_K1	LCD Data[4]	3.3V
LCD_DATA[3]	PIN_K7	LCD Data[3]	3.3V
LCD_DATA[2]	PIN_L2	LCD Data[2]	3.3V
LCD_DATA[1]	PIN_L1	LCD Data[1]	3.3V
LCD_DATA[0]	PIN_L3	LCD Data[0]	3.3V
LCD_EN	PIN_L4	LCD Enable	3.3V
LCD_RW	PIN_M1	LCD Read/Write Select, 0 = Write, 1 = Read	3.3V
LCD_RS	PIN_M2	LCD Command/Data Select, 0 = Command, 1 = Data	3.3V
LCD_ON	PIN_L5	LCD Power ON/OFF	3.3V
LCD_BLON	PIN_L6	LCD Back Light ON/OFF	3.3V

The 2 x 16 character LCD has a built in graphic controller.
The controller has three internal memory regions (DDRAM, CGROM, CGRAM), each with a specific purpose. The display must be initialized before accessing any of these memory regions.
The memory map, the command set of the internal controller and the operation and timing of the 8-bit Data Interface are described in the attached data sheet.

1. Write a short report documenting the main characteristic and performance of the system you designed (think of the document as the "data sheet" of your system)
2. Submit VHDL code for both design and test bench.
3. Submit the waveforms used for the test bench. Comment the waveforms and make sure to illustrate that the system works as expected
4. Analyze the synthesis and implementation reports and submit a short summary including area and timing.
5. Demonstrate the operation of the circuit on the prototyping board

Grading will be based on:
A. Correctness of the design [40 pts]
B. Coding style quality [20 pts]
C. Effectiveness of testing [30 pts]
D. Quality of the report [20 pts]

Crystalfontz America, Inc.

CUSTOMER		
MODEL	**CFAH1602B-TMC-JP**	
APPROVAL	**BY:**	**DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

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Contents

1.Module Classification Information

CFA H 1602 B－T M C－ JP

① ② ③ ④ ⑤ ⑥ ⑦ ⑧

①	Brand: CRYSTALFONTZ AMERICA, INCORPORATED		
②	Display Type: **H→Character Type**, G→Graphic Type		
③	Display's logical dimensions: **16** columns by **02** lines		
④	Model serials no.		
⑤	Backlight Type:	N→Without backlight B→EL, Blue green D→EL, Green W→EL, White F→CCFL, White **T→LED, White**	Y→LED, Yellow Green A→LED, Amber R→LED, Red O→LED, Orange G→LED, Green
⑥	LCD Mode:	B→TN Positive, Gray N→TN Negative, G→STN Positive, Gray Y→STN Positive, Yellow Green	**M→STN Negative, Blue** F→FSTN Positive T→FSTN Negative
⑦	LCD Polarizer Type, Temperature range, Viewing direction:	A→Reflective, N.T, 6:00 D→Reflective, N.T, 12:00 G→Reflective, W. T, 6:00 J→Reflective, W. T, 12:00 B→Transflective, N.T,6:00 E→Transflective, N.T.12:00	H→Transflective, W.T,6:00 K→Transflective, W.T,12:00 **C→Transmissive, N.T,6:00** F→Transmissive, N.T,12:00 I→Transmissive, W. T, 6:00 L→Transmissive, W.T,12:00
⑧	Special Code:	**JP→English and Japanese standard font**	

2. Precautions in use of LCD Modules

(1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2) Don’t make extra holes on the printed circuit board, modify its shape or change the components of LCD module.

(3) Don’t disassemble the LCM.

(4) Don’t operate it above the absolute maximum rating.

(5) Don’t drop, bend or twist LCM.

(6) Soldering:only to the I/O terminals.

(7) Storage:please storage in anti-static electricity container and clean environment.

3. General Specification

ITEM	STANDARD VALUE	UNIT
Number of Characters:	16 characters × 2 Lines	
Module dimension:	80.0 × 36.0 × 13.5(MAX)mm	mm
View area:	66.0 × 16.0mm	mm
Active area:	56.2 × 11.5mm	mm
Character size:	(L)2.95 × (W)5.55mm	mm
Character pitch:	(L)3.55 × (W)5.95mm	mm
LCD type:	STN, Negative ,transmissive, Blue	
Duty:	1/16	
View direction:	6 o’clock	
Backlight:	LED White	

4. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_{OP}	0	—	+50	℃
Storage Temperature	T_{ST}	-10	—	+60	℃
Input Voltage	V_I	V_{SS}	—	V_{DD}	V
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-0.3	—	7	V
Supply Voltage For LCD	$V_{DD}-V_0$	-0.3	—	Vdd+0.3	V
Supply current FOR LED B/L	I_{LED}	—	—	25	mA

5. Electrical Characteristics

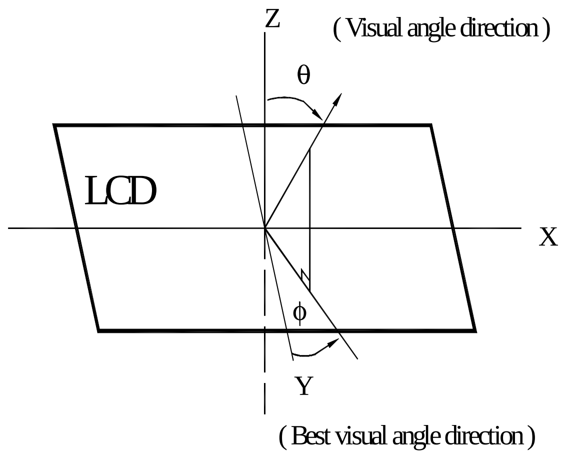
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	4.5	—	5.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	Ta=0℃	—	4.2	4.5	V
		Ta=25℃	—		—	V
		Ta=50℃	3.8		—	V
Input High Vol	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Vol	V_{IL}	—	—	—	0.6	V
Output High Vol	V_{OH}	—	2.4	—	—	V
Output Low Vol.	V_{OL}	—	—	—	0.4	V
Supply Current	I_{DD}	V_{DD}=5V	—	1.2	—	mA

6. Optical Characteristics

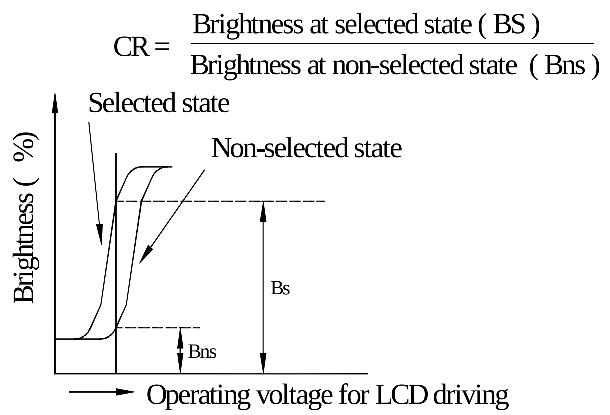
ITEM	SYMBAL	CONDITION	MIN.	TYP.	MAX.	UNIT
View Angle	(V) θ	CR≧3	10		105	deg
	(H) φ	CR≧3	-30		30	deg
Contrast Ratio	CR	—		5		—
Response Time	T rise	—		200	300	ms
	T fall	—		200	300	ms

6.1 Definitions

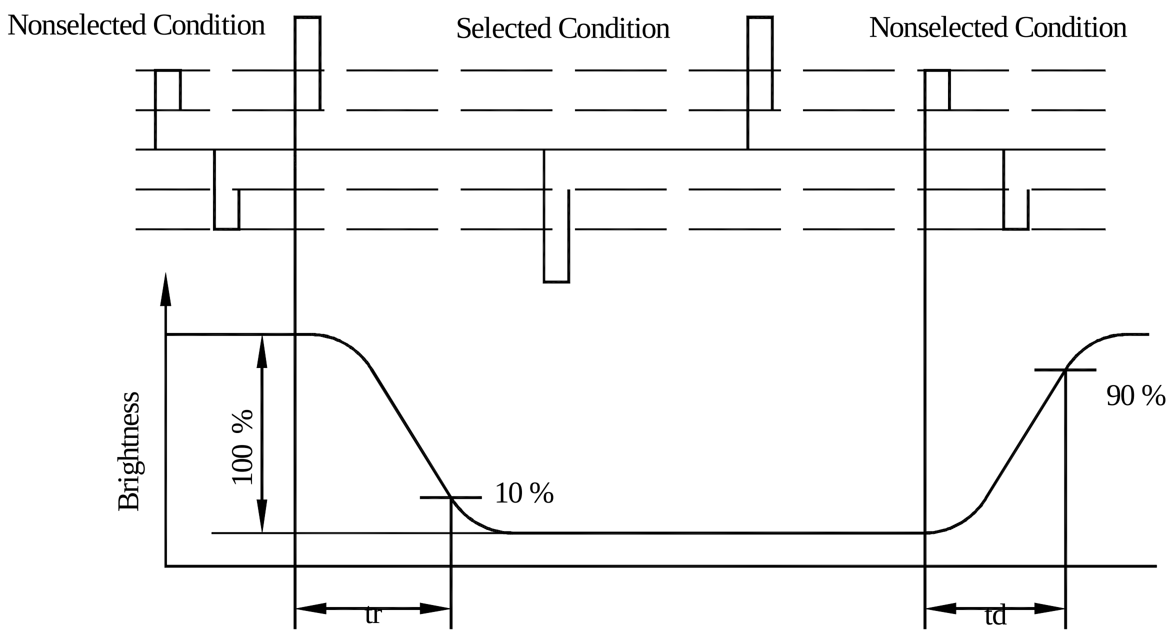
■View Angles



■Contrast Ratio



■Response Time



7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H:DATA, L:Instruction code
5	R/W	H/L	H:Read(MPU→Module)L:Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A	—	Power supply for LED backlight (+)
16	K	—	Power supply for LED backlight (-)

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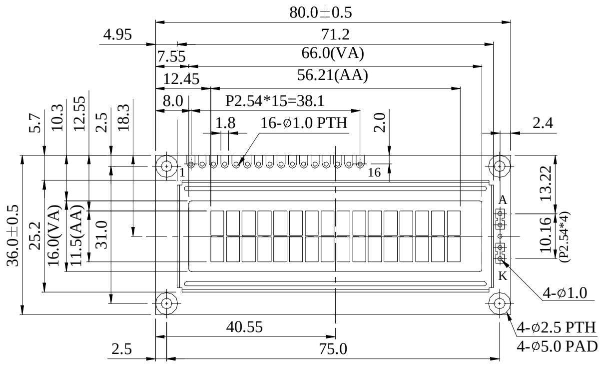
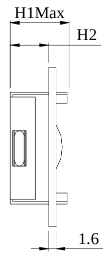
8.Counter drawing

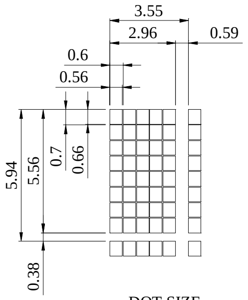




LED H/L B/L

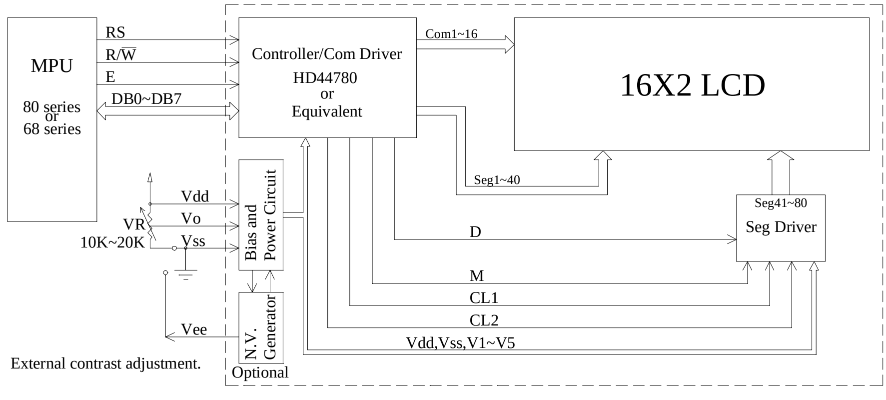
	High	
H1	13.2	
H2	8.6	

PIN NO.	SYMBOL
1	Vss
2	Vdd
3	Vo
4	RS
5	R/$\overline{W}$
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A/Vee
16	K



DOT SIZE

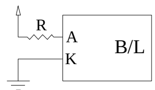
The non-specified tolerance of dimension is ±0.3mm.



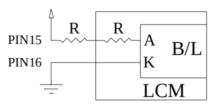
External contrast adjustment.

LED B/L Drive Method

1.Drive from A,K

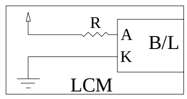


2.Drive from pin15, pin16



(Will never get Vee output from pin15)

3.Drive from Vdd,Vss



(Contrast performance may go down.)

Recommanded Value

V_{LED}= 3.3V, I_{LED}=25mA

Character located	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

9. Backlight Information

9.1 Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	—	25		mA	V=3.3V
Supply Voltage	V	—	3.3	3.6	V	
Reverse Voltage	VR	—	—	8	V	
Luminous Intensity	IV	20	—	—	CD/M^2	ILED=25mA
Wave Length	λp				nm	ILED=25mA
Life Time		—	100000	—	Hr.	$V \leqq 3.6V$
Color	White					

10. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.

	High bits			Low bits			
AC (hexadecimal)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example:DDRAM addresses 4E

1	0	0	1	1	1	0

DDRAM Address

Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

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Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

Table 1.

For 5 * 8 dot character patterns

Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low)	CGRAM Address 5 4 3 (High)	CGRAM Address 2 1 0 (Low)	Character Patterns (CGRAM data) 7 6 5 (High)	Character Patterns (CGRAM data) 4 3 2 1 0 (Low)	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	■ ■ ■ ■ 0	Character pattern(1)
		0 0 1	* * *	■ 0 0 0 ■	
		0 1 0	* * *	■ 0 0 0 ■	
		0 1 1	* * *	■ ■ ■ ■ 0	
		1 0 0	* * *	■ 0 ■ 0 0	
		1 0 1	* * *	■ 0 0 ■ 0	
		1 1 0	* * *	■ 0 0 0 ■	
		1 1 1	* * *	0 0 0 0 0	Cursor pattern
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	■ 0 0 0 ■	Character pattern(2)
		0 0 1	* * *	0 ■ 0 ■ 0	
		0 1 0	* * *	■ ■ ■ ■ ■	
		0 1 1	* * *	0 0 ■ 0 0	
		1 0 0	* * *	■ ■ ■ ■ ■	
		1 0 1	* * *	0 0 ■ 0 0	
		1 1 0	* * *	0 0 ■ 0 0	
		1 1 1	* * *	0 0 0 0 0	Cursor pattern
		0 0 0	* * *		
		0 0 1			
0 0 0 0 * 1 1 1	1 1 1	1 0 0			
		1 0 1			
		1 1 0			
		1 1 1	* * *		

For 5 * 10 dot character patterns

Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low)	CGRAM Address 5 4 (High)	CGRAM Address 3 2 1 0 (Low)	Character Patterns (CGRAM data) 7 6 5 (High)	Character Patterns (CGRAM data) 4 3 2 1 0 (Low)	
0 0 0 0 * 0 0 0	0 0	0 0 0 0	* * *	0 0 0 0 0	Character pattern
		0 0 0 1	* * *	0 0 0 0 0	
		0 0 1 0	* * *	■ 0 ■ ■ 0	
		0 0 1 1	* * *	■ ■ 0 0 ■	
		0 1 0 0	* * *	■ 0 0 0 ■	
		0 1 0 1	* * *	■ 0 0 0 ■	
		0 1 1 0	* * *	■ ■ ■ ■ 0	
		0 1 1 1	* * *	■ 0 0 0 0	
		1 0 0 0	* * *	■ 0 0 0 0	
		1 0 0 1	* * *	■ 0 0 0 0	
		1 0 1 0	* * *	0 0 0 0 0	Cursor pattern
		1 1 1 1	* * *	* * * * *	

■ : " High "

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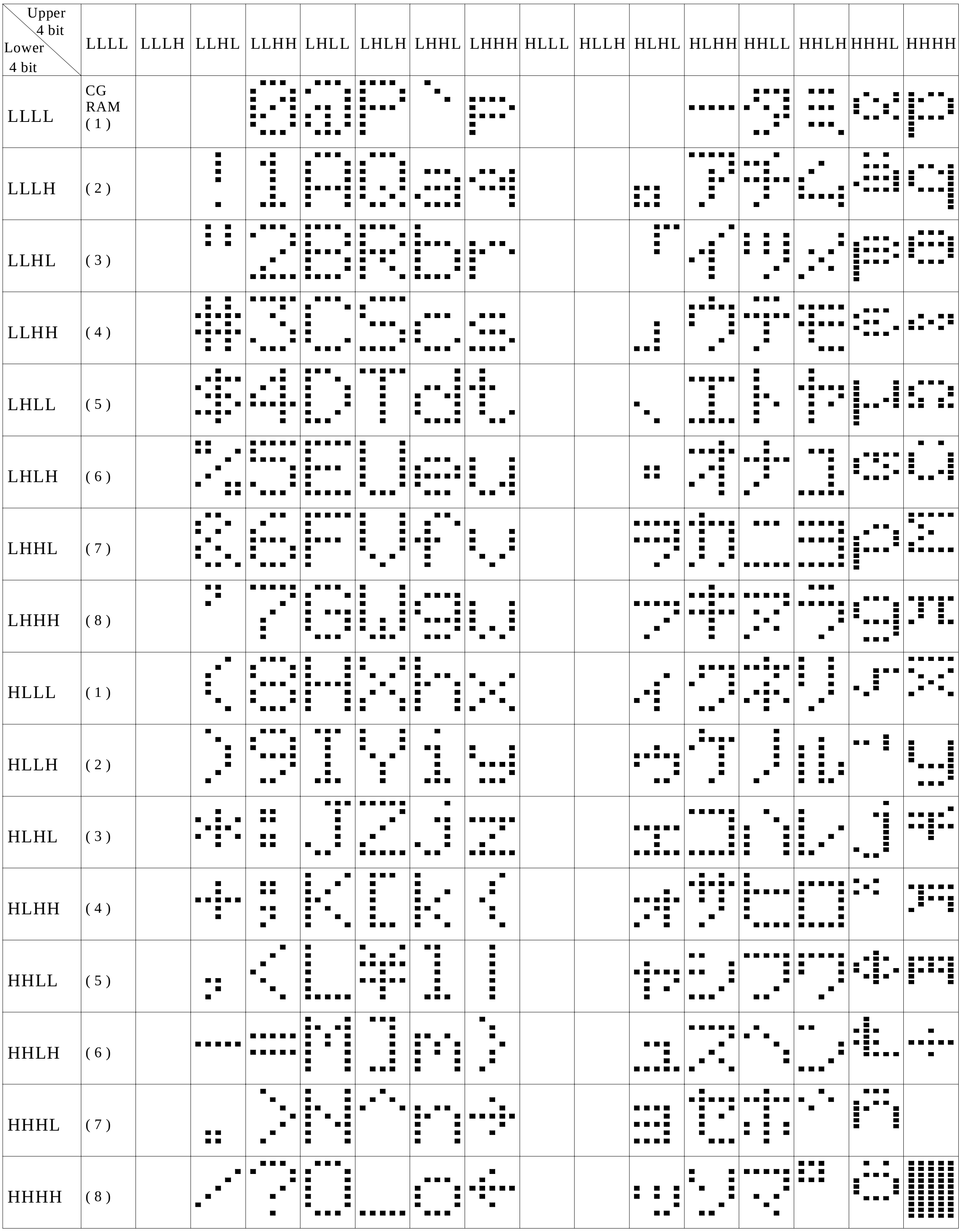
11. Character Generator ROM Pattern

Table.2



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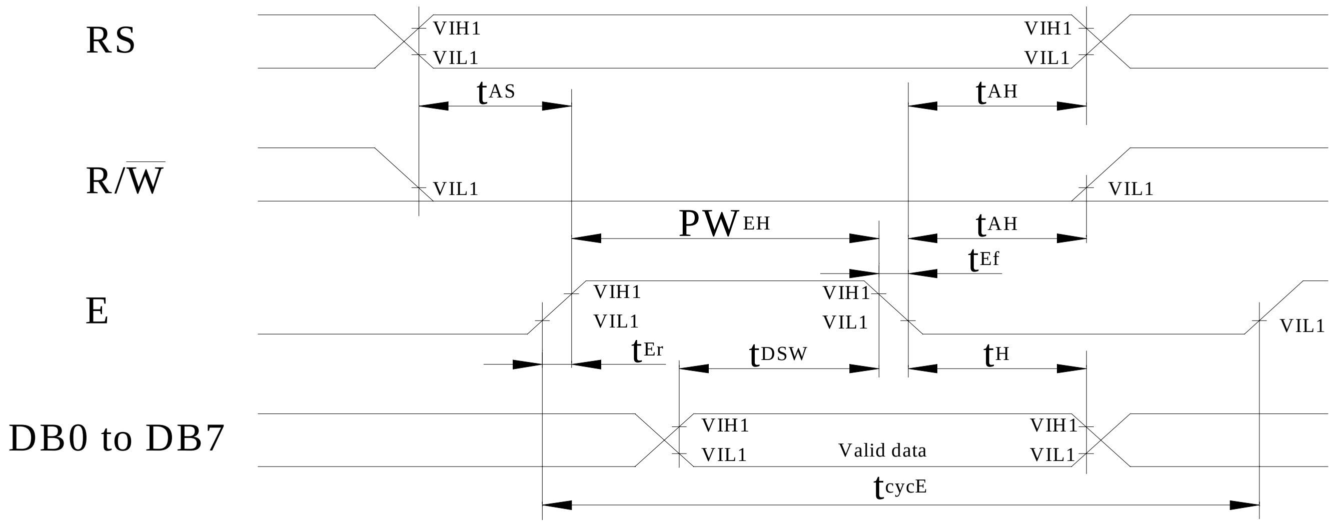
12. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “00H” to DDRAM and set DDRAM address to “00H” from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

＊ ”—”：don’t care

13. Timing Characteristics

13.1 Write Operation



Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data set-up time	t_{DSW}	80	—	—	ns
Data hold time	t_H	10	—	—	ns

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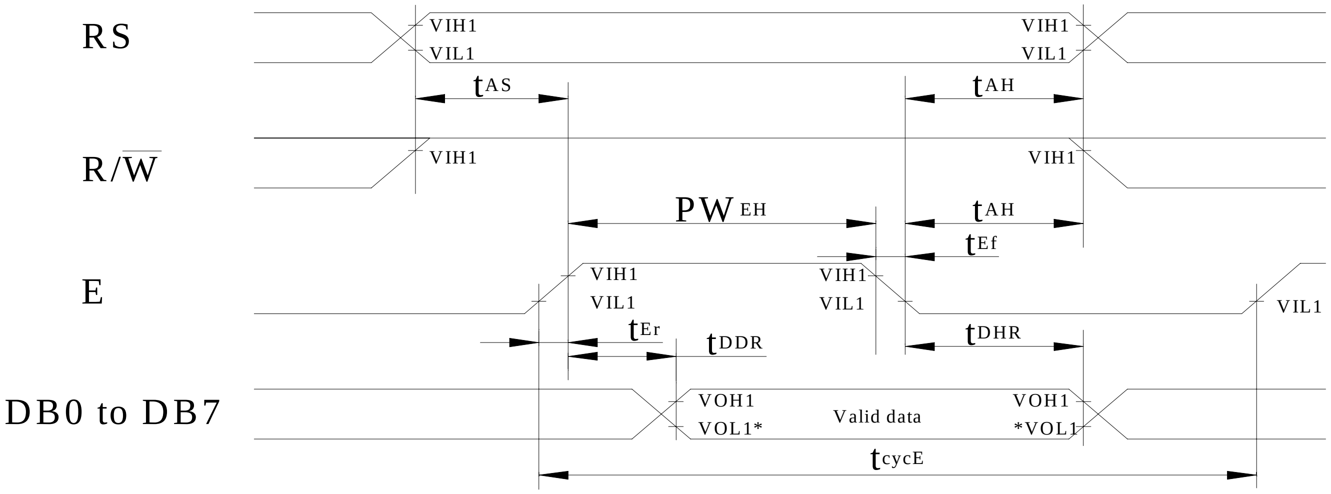
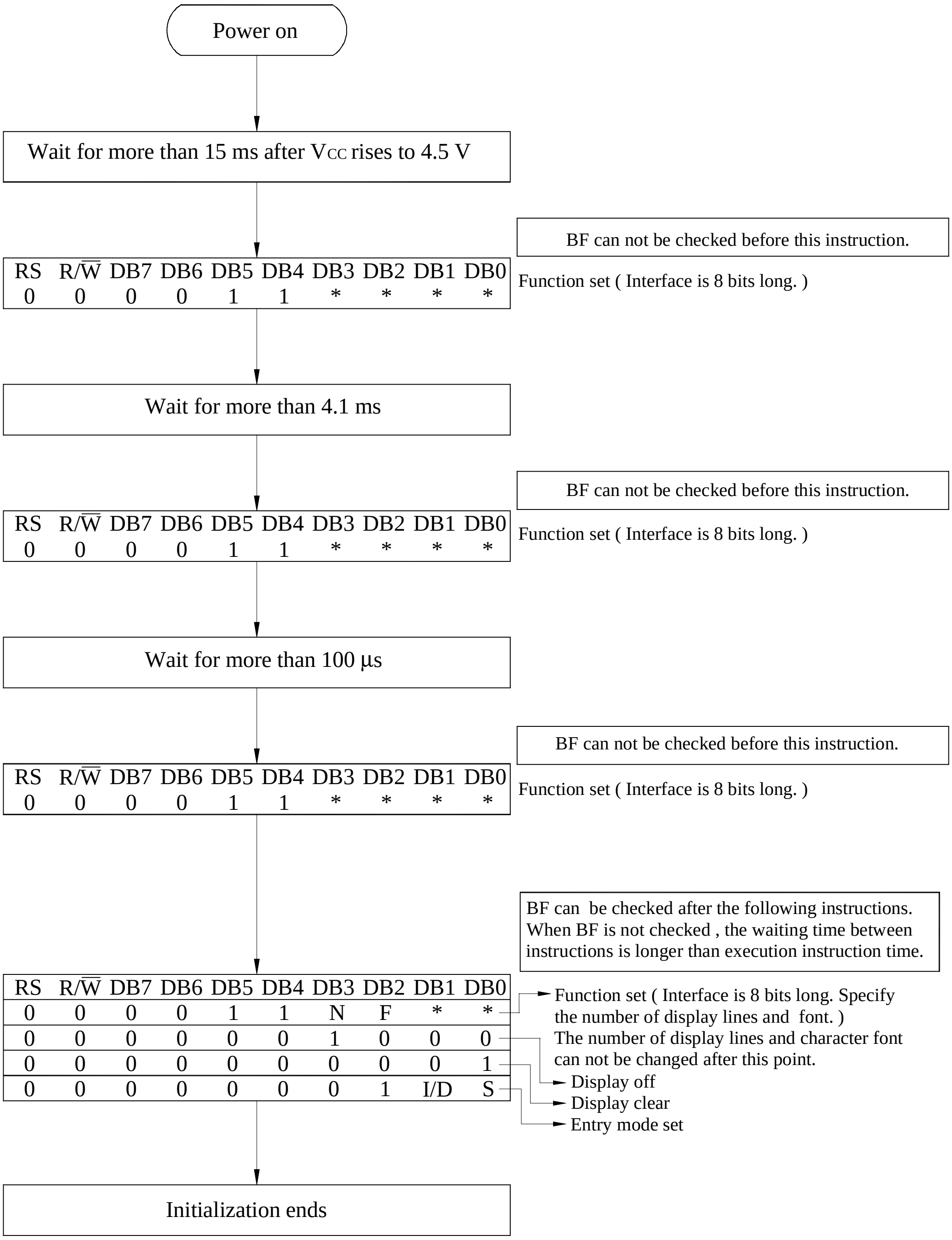
13.2 Read Operation



NOTE: *VOL1 is assumed to be 0.8V at 2 MHZ operation.

ITEM	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data delay time	t_{DDR}	—	—	160	ns
Data hold time	t_{DHR}	5	—	—	ns

14. Initializing of LCM



8-Bit Ineterface

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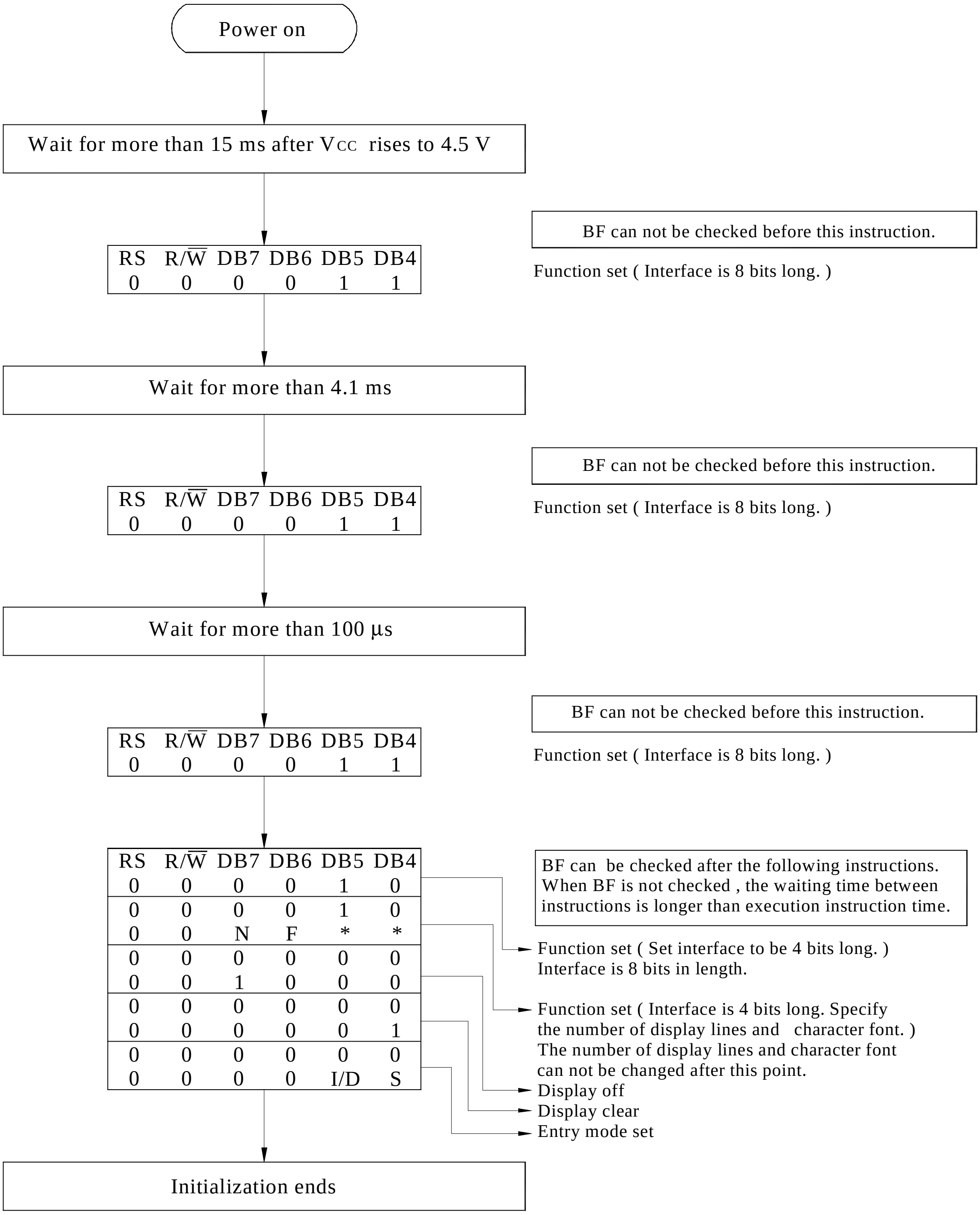


4-Bit Ineterface

15. Quality Assurance

◆ Screen Cosmetic Criteria

No.	Defect	Judgement Criterion	Partition
1	Spots	A)Clear Size:d mm — Acceptable Qty in active area d ≦0.1 — Disregard 0.1<d≦0.2 — 6 0.2<d≦0.3 — 2 0.3<d — 0 Note:Including pin holes and defective dots which must be within one pixel size. B)Unclear Size:d mm — Acceptable Qty in active area d ≦0.2 — Disregard 0.2<d≦0.5 — 6 0.5<d≦0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarizer	Size:d mm — Acceptable Qty in active area d≦0.3 — Disregard 0.3<d≦1.0 — 3 1.0<d≦1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

16. RELIABILITY

■Content of Reliability Test

No.	Test Item	Content of Test	Test Condition	Applicable Standard
Environmental Test				
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60℃ 200hrs	——
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10℃ 200hrs	——
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50℃ 200hrs	——
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 200hrs	——
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60℃,90%RH 96hrs	——
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	50℃,90%RH 96hrs	——
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -10℃ 25℃ 60℃ ←→ 30min 5min 30min 1 cycle	-10℃/60℃ 10 cycles	——
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	——
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃

HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7V to 5.5V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
  — 2.7 to 5.5V
- Wide range of liquid crystal display driver power
  — 3.0 to 11V
- Liquid crystal drive waveform
  — A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  — 2 MHz (when V_{CC} = 5V)
- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  — 208 character fonts (5 × 8 dot)
  — 32 character fonts (5 × 10 dot)

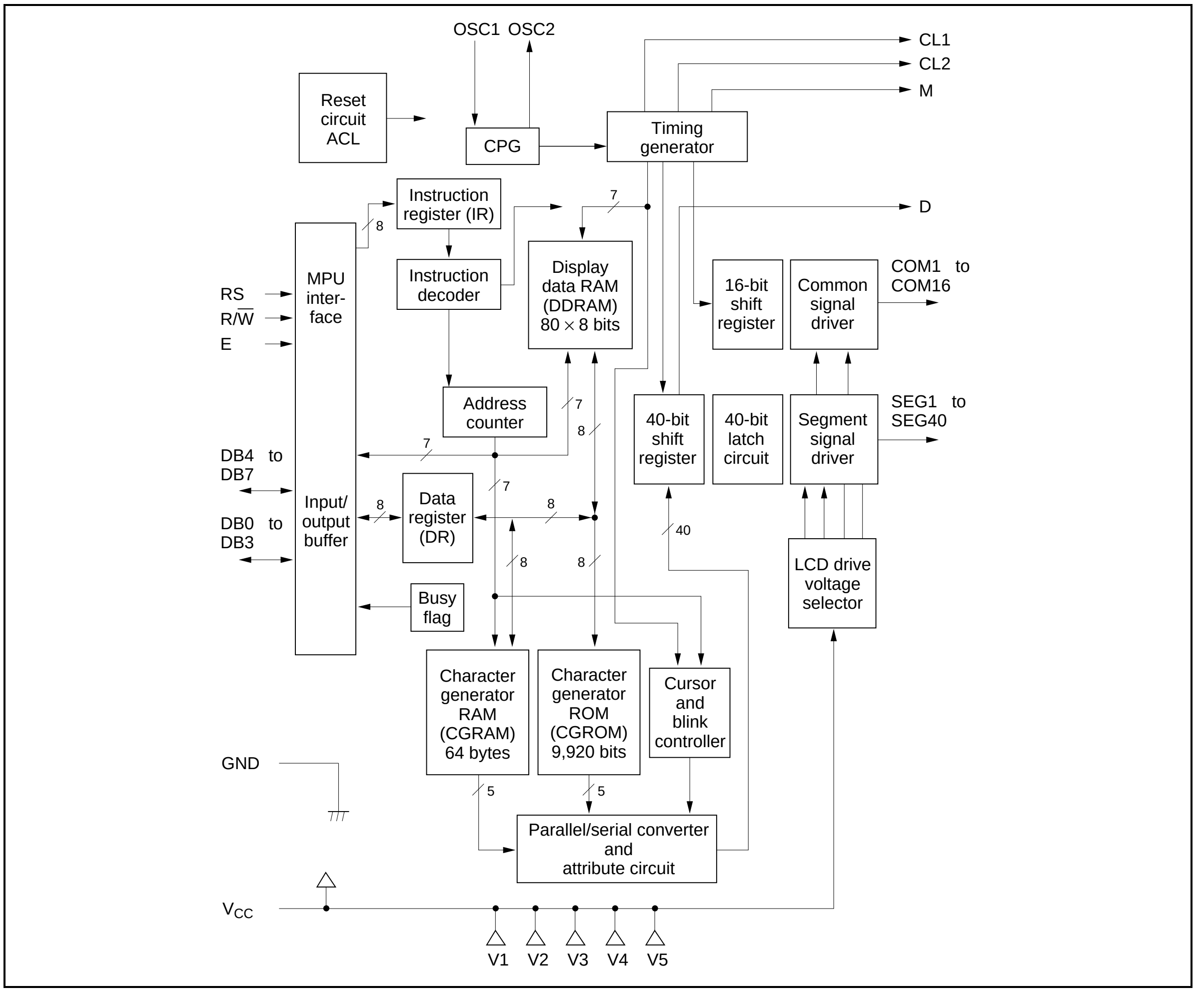
- 64 × 8-bit character generator RAM
  - 8 character fonts (5 × 8 dot)
  - 4 character fonts (5 × 10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 × 8 dots with cursor
  - 1/11 for one line of 5 × 10 dots with cursor
  - 1/16 for two lines of 5 × 8 dots with cursor
- Wide range of instruction functions:
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

Ordering Information

Type No.	Package	CGROM
HD44780UA00FS	FP-80B	Japanese standard font
HCD44780UA00	Chip	
HD44780UA00TF	TFP-80F	
HD44780UA02FS	FP-80B	European standard font
HCD44780UA02	Chip	
HD44780UA02TF	TFP-80F	
HD44780UBxxFS	FP-80B	Custom font
HCD44780UBxx	Chip	
HD44780UBxxTF	TFP-80F	

Note: xx: ROM code No.

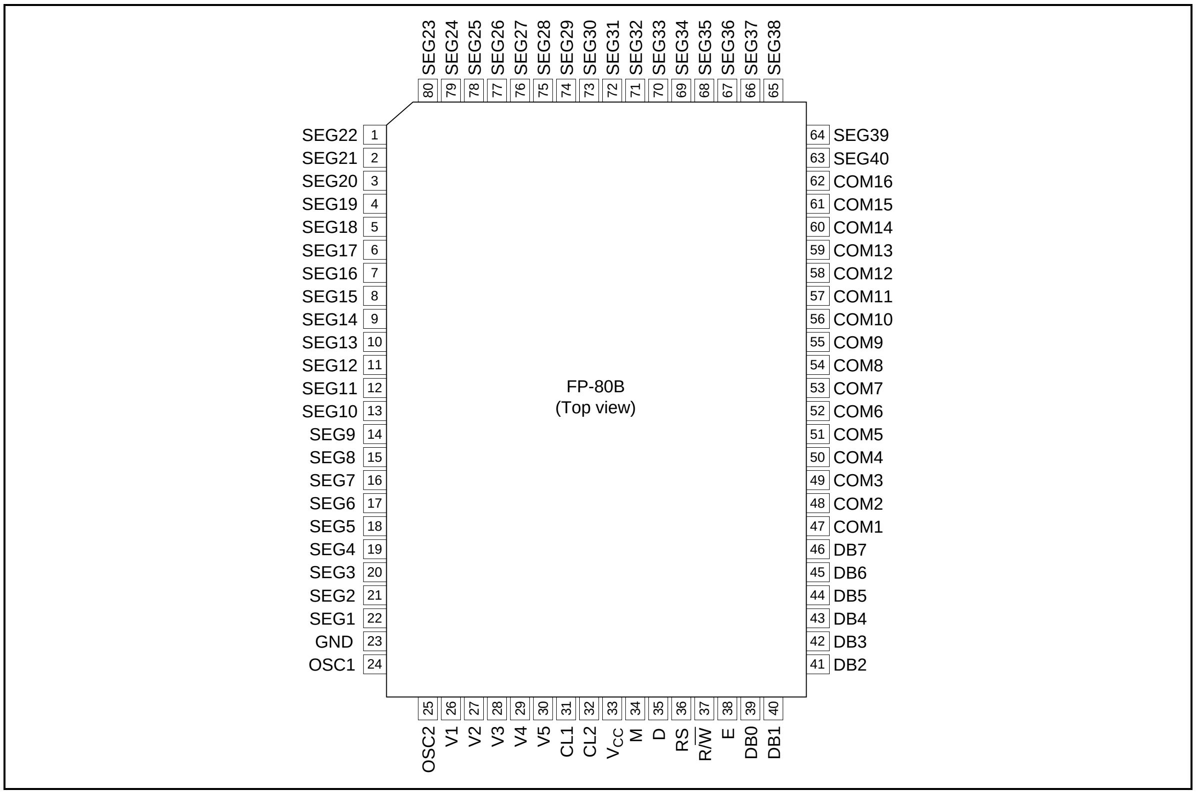
HD44780U Block Diagram



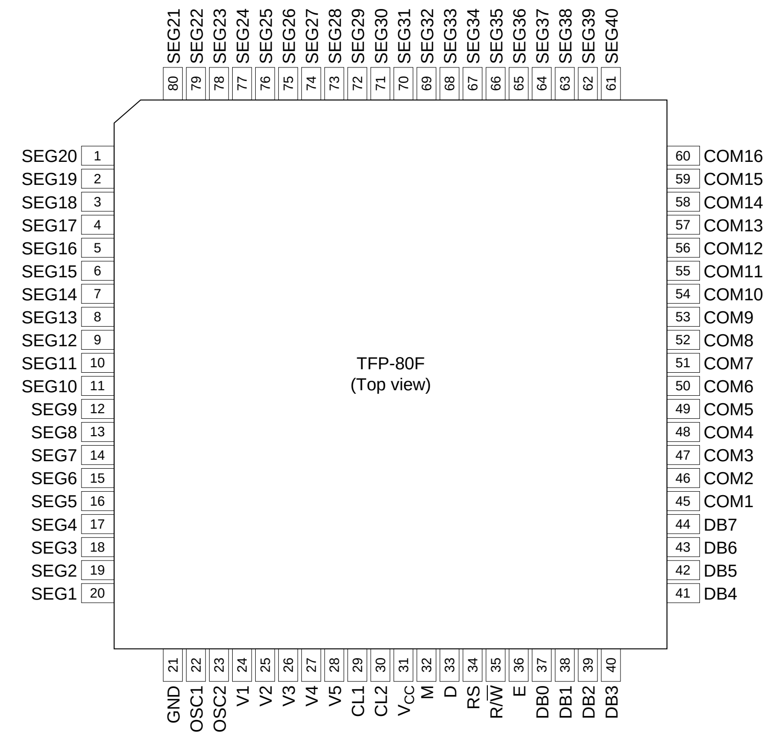
LCD-II Family Comparison

Item		HD44780S	HD44780U
Power supply voltage		5 V ±10%	2.7 to 5.5 V
Liquid crystal drive voltage VLCD	1/4 bias	3.0 to 11.0V	3.0 to 11.0V
	1/5 bias	4.6 to 11.0V	3.0 to 11.0V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)	9,920 bits (208 character fonts for 5 × 8 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes
DDRAM		80 bytes	80 bytes
Segment signals		40	40
Common signals		16	16
Liquid crystal drive waveform		A	A
Oscillator	Clock source	External resistor, external ceramic filter, or external clock	External resistor or external clock
	R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ±30% (59 to 110 Hz for 1/8 and1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)
	R_f resistance	91 kΩ ±2%	91 kΩ ±2% (when V_{cc} = 5V) 75 kΩ ±2% (when V_{cc} = 3V)
Instructions		Fully compatible within the HD44780S	
CPU bus timing		1 MHz	1 MHz (when V_{cc} = 3V) 2 MHz (when V_{cc} = 5V)
Package		FP-80 FP-80A	FP-80B TFP-80F

HD44780U Pin Arrangement (FP-80B)

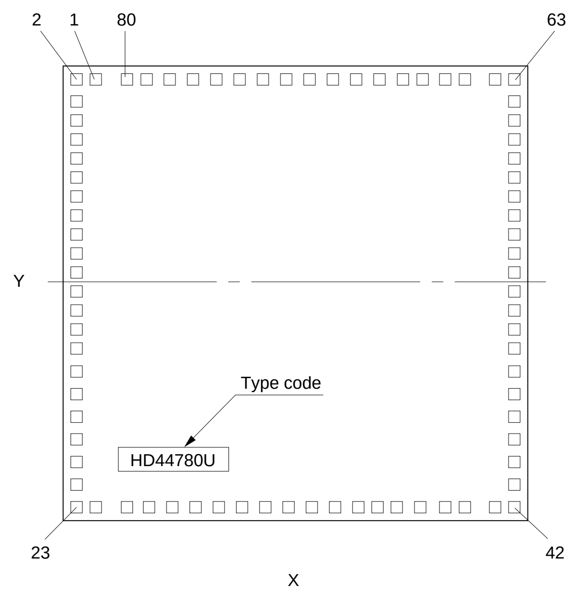


HD44780U Pin Arrangement (TFP-80F)



HD44780U Pad Arrangement

Chip size: 4.90 × 4.90 mm^2
Coordinate: Pad center (μm)
Origin: Chip center
Pad size: 114 × 114 μm^2



HCD44780U Pad Location Coordinates

Pad No.	Function	Coordinate X (um)	Coordinate Y (um)	Pad No.	Function	Coordinate X (um)	Coordinate Y (um)
1	SEG22	–2100	2313	41	DB2	2070	–2290
2	SEG21	–2280	2313	42	DB3	2260	–2290
3	SEG20	–2313	2089	43	DB4	2290	–2099
4	SEG19	–2313	1833	44	DB5	2290	–1883
5	SEG18	–2313	1617	45	DB6	2290	–1667
6	SEG17	–2313	1401	46	DB7	2290	–1452
7	SEG16	–2313	1186	47	COM1	2313	–1186
8	SEG15	–2313	970	48	COM2	2313	–970
9	SEG14	–2313	755	49	COM3	2313	–755
10	SEG13	–2313	539	50	COM4	2313	–539
11	SEG12	–2313	323	51	COM5	2313	–323
12	SEG11	–2313	108	52	COM6	2313	–108
13	SEG10	–2313	–108	53	COM7	2313	108
14	SEG9	–2313	–323	54	COM8	2313	323
15	SEG8	–2313	–539	55	COM9	2313	539
16	SEG7	–2313	–755	56	COM10	2313	755
17	SEG6	–2313	–970	57	COM11	2313	970
18	SEG5	–2313	–1186	58	COM12	2313	1186
19	SEG4	–2313	–1401	59	COM13	2313	1401
20	SEG3	–2313	–1617	60	COM14	2313	1617
21	SEG2	–2313	–1833	61	COM15	2313	1833
22	SEG1	–2313	–2073	62	COM16	2313	2095
23	GND	–2280	–2290	63	SEG40	2296	2313
24	OSC1	–2080	–2290	64	SEG39	2100	2313
25	OSC2	–1749	–2290	65	SEG38	1617	2313
26	V1	–1550	–2290	66	SEG37	1401	2313
27	V2	–1268	–2290	67	SEG36	1186	2313
28	V3	–941	–2290	68	SEG35	970	2313
29	V4	–623	–2290	69	SEG34	755	2313
30	V5	–304	–2290	70	SEG33	539	2313
31	CL1	–48	–2290	71	SEG32	323	2313
32	CL2	142	–2290	72	SEG31	108	2313
33	V_{CC}	309	–2290	73	SEG30	–108	2313
34	M	475	–2290	74	SEG29	–323	2313
35	D	665	–2290	75	SEG28	–539	2313
36	RS	832	–2290	76	SEG27	–755	2313
37	R/$\overline{W}$	1022	–2290	77	SEG26	–970	2313
38	E	1204	–2290	78	SEG25	–1186	2313
39	DB0	1454	–2290	79	SEG24	–1401	2313
40	DB1	1684	–2290	80	SEG23	–1617	2313

Pin Functions

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
$R/\overline{W}$	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write.
DB4 to DB7	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB7 can be used as a busy flag.
DB0 to DB3	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.
CL1	1	O	Extension driver	Clock to latch serial data D sent to the extension driver
CL2	1	O	Extension driver	Clock to shift serial data D
M	1	O	Extension driver	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	Extension driver	Character pattern data corresponding to each segment signal
COM1 to COM16	16	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor.
SEG1 to SEG40	40	O	LCD	Segment signals
V1 to V5	5	—	Power supply	Power supply for LCD drive V_{cc} –V5 = 11 V (max)
V_{cc}, GND	2	—	Power supply	V_{cc}: 2.7V to 5.5V, GND: 0V
OSC1, OSC2	2	—	Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.

Function Description

Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DDRAM or CGRAM and temporarily stores data to be read from DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into DDRAM or CGRAM by an internal operation. The DR is also used for data storage when reading data from DDRAM or CGRAM. When address information is written into the IR, data is read and then stored into the DR from DDRAM or CGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (Table 1).

Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (Table 1), the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DDRAM or CGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM or CGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB0 to DB6 when RS = 0 and R/$\overline{W}$ = 1 (Table 1).

Table 1 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (Figure 2)
  - — When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See Figure 3.

    When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

	High order bits			Low order bits			
AC (hexadecimal)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example: DDRAM address 4E

1	0	0	1	1	1	0

Figure 1 DDRAM Address

Display position (digit)	1	2	3	4	5		79	80
DDRAM address (hexadecimal)	00	01	02	03	04	....	4E	4F

Figure 2 1-Line Display

Display position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
For shift left	01	02	03	04	05	06	07	08
For shift right	4F	00	01	02	03	04	05	06

Figure 3 1-Line by 8-Character Display Example

- 2-line display (N = 1) (Figure 4)
  - — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters × 2 lines are displayed. See Figure 5.

    When display shift operation is performed, the DDRAM address shifts. See Figure 5.

Display position	1	2	3	4	5		39	40
DDRAM address (hexadecimal)	00	01	02	03	04	....	26	27
	40	41	42	43	44	....	66	67

Figure 4 2-Line Display

Display position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For shift left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For shift right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 5 2-Line by 8-Character Display Example

— Case 2: For a 16-character × 2-line display, the HD44780 can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	$\underbrace{\hspace{4em}}_{\text{HD44780U display}}$								$\underbrace{\hspace{4em}}_{\text{Extension driver display}}$							
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 6 2-Line by 16-Character Display Example

Character Generator ROM (CGROM)

The character generator ROM generates 5×8 dot or 5×10 dot character patterns from 8-bit character codes (Table 4). It can generate 208 5×8 dot character patterns and 32 5×10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns.

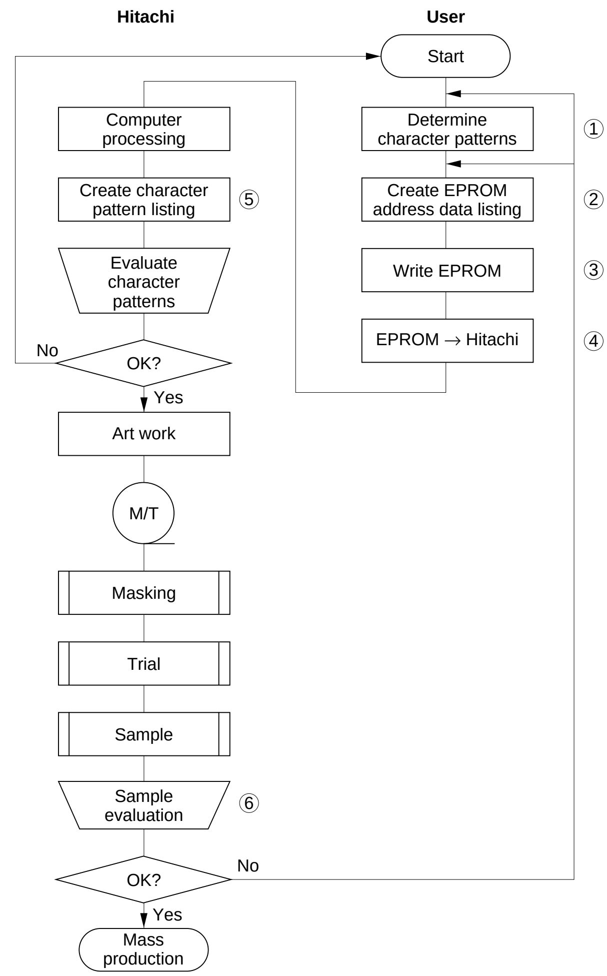
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in Figure 7:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 7 Character Pattern Development Procedure

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD44780U character generator ROM can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns for a total of 240 different character patterns.

  — Character patterns

  EPROM address data and character pattern data correspond with each other to form a 5 × 8 or 5 × 10 dot character pattern (Tables 2 and 3).

Table 2 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 Dots)

EPROM Address												Data					
																LSB	
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0	
								0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← Cursor position
								1	0	0	0	0	0	0	0	0	
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	
Character code								Line position									

Notes: 1. EPROM addresses A11 to A4 correspond to a character code.
2. EPROM addresses A3 to A0 specify a line position of the character pattern.
3. EPROM data O4 to O0 correspond to character pattern data.
4. EPROM data O5 to O7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 9 and the following lines must be blanked with 0s for a 5 × 8 dot character fonts.

— Handling unused character patterns

1. EPROM data outside the character pattern area: Always input 0s.
2. EPROM data in CGRAM area: Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)
3. EPROM data used when the user does not use any HD44780U character pattern: According to the user application, handled in one of the two ways listed as follows.

a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)

b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 Dots)

EPROM Address												Data					
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0 (LSB)	
								0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	1	1	0	1	
								0	0	1	1	1	0	0	1	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	0	1	1	1	1	
0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1	
								1	0	0	0	0	0	0	0	1	
								1	0	0	1	0	0	0	0	1	
								1	0	1	0	0	0	0	0	0	← Cursor position
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	

Character code (A11–A4); Line position (A3–A0)

Notes: 1. EPROM addresses A11 to A3 correspond to a character code.
2. EPROM addresses A3 to A0 specify a line position of the character pattern.
3. EPROM data O4 to O0 correspond to character pattern data.
4. EPROM data O5 to O7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 11 and the following lines must be blanked with 0s for a 5 × 10 dot character fonts.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
xxxx0001	(2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	(3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
xxxx0011	(4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	(5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	$\bar{x}$
xxxx1001	(2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	$^{-1}$	y
xxxx1010	(3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	(4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	^{x}	万
xxxx1100	(5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	(6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	(8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

Note: The user can specify any pattern for character-generator RAM.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A02)

Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	▶		0	@	P	`	p	Б	α	‖	°	À	Ð	à	ð
xxxx0001	(2)	◀	!	1	A	Q	a	q	Д	♪	¡	±	Á	Ñ	á	ñ
xxxx0010	(3)	“	"	2	B	R	b	r	Ж	Γ	¢	²	Â	Ò	â	ò
xxxx0011	(4)	”	#	3	C	S	c	s	З	π	£	³	Ã	Ó	ã	ó
xxxx0100	(5)	⏫	$	4	D	T	d	t	И	Σ	¤	₧	Ä	Ô	ä	ô
xxxx0101	(6)	⏬	%	5	E	U	e	u	Й	σ	¥	µ	Å	Õ	å	õ
xxxx0110	(7)	●	&	6	F	V	f	v	Л	♬	¦	¶	Æ	Ö	æ	ö
xxxx0111	(8)	↵	'	7	G	W	g	w	П	τ	§	·	Ç	×	ç	÷
xxxx1000	(1)	↑	(	8	H	X	h	x	У	🔔	ƒ	ω	È	Ø	è	ø
xxxx1001	(2)	↓	)	9	I	Y	i	y	Ц	Θ	©	¹	É	Ù	é	ù
xxxx1010	(3)	→	*	:	J	Z	j	z	Ч	Ω	ª	º	Ê	Ú	ê	ú
xxxx1011	(4)	←	+	;	K	[	k	{	Ш	δ	«	»	Ë	Û	ë	û
xxxx1100	(5)	≤	,	<	L	\	l	|	Щ	∞	Ю	¼	Ì	Ü	ì	ü
xxxx1101	(6)	≥	-	=	M	]	m	}	Ъ	♥	Я	½	Í	Ý	í	ý
xxxx1110	(7)	▲	.	>	N	^	n	~	Ы	ε	®	¾	Î	Þ	î	þ
xxxx1111	(8)	▼	/	?	O	_	o	⌂	Э	∩	‘	¿	Ï	ß	ï	ÿ

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

For 5 × 8 dot character patterns

Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low)	CGRAM Address 5 4 3 (High)	CGRAM Address 2 1 0 (Low)	Character Patterns (CGRAM data) 7 6 5 (High)	Character Patterns (CGRAM data) 4 3 2 1 0 (Low)	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	Character pattern (1)
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	Character pattern (2)
		0 0 1		0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0		0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	Cursor position
		0 0 0	* * *		
		0 0 1			
0 0 0 0 * 1 1 1	1 1 1				
		1 0 0			
		1 0 1			
		1 1 0			
		1 1 1	* * *		

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.

   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.

   If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.

3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).

4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data) (cont)

For 5 × 10 dot character patterns

Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low)	CGRAM Address 5 4 (High)	CGRAM Address 3 2 1 0 (… Low)	Character Patterns (CGRAM data) 7 6 5 (High)	Character Patterns (CGRAM data) 4 3 2 1 0 (… Low)	
		0 0 0 0	* * *	0 0 0 0 0	Character pattern
		0 0 0 1		0 0 0 0 0	
		0 0 1 0		1 0 1 1 0	
		0 0 1 1		1 1 0 0 1	
		0 1 0 0		1 0 0 0 1	
0 0 0 0 * 0 0 *	0 0	0 1 0 1		1 0 0 0 1	
		0 1 1 0		1 1 1 1 0	
		0 1 1 1		1 0 0 0 0	
		1 0 0 0		1 0 0 0 0	
		1 0 0 1		1 0 0 0 0	
		1 0 1 0	* * *	0 0 0 0 0	Cursor position
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	
		0 0 0 0	* * *		
		0 0 0 1			
0 0 0 0 * 1 1 *	1 1	1 0 0 1			
		1 0 1 0	* * *		
		1 0 1 1	* * *	* * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1	* * *	* * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CGRAM address bits 4 and 5 (2 bits: 4 types).

2. CGRAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.

   Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.

   If the 11th line data is "1", "1" bits will light up the 11th line regardless of the cursor presence.

   Since lines 12 to 16 are not used for display, they can be used for general data RAM.

3. Character pattern row positions are the same as 5 × 8 dot character pattern positions.

4. CGRAM character patterns are selected when character code bits 4 to 7 are all 0.

   However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).

For example (Figure 8), when the address counter is 08H, the cursor position is displayed at DDRAM address 08H.

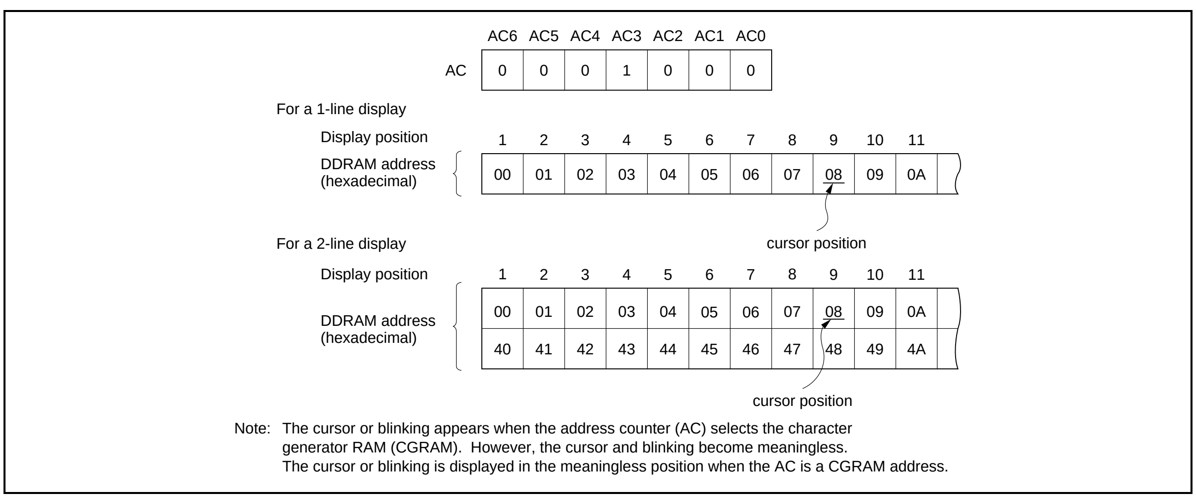


Figure 8 Cursor/Blink Display Example

Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.
- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

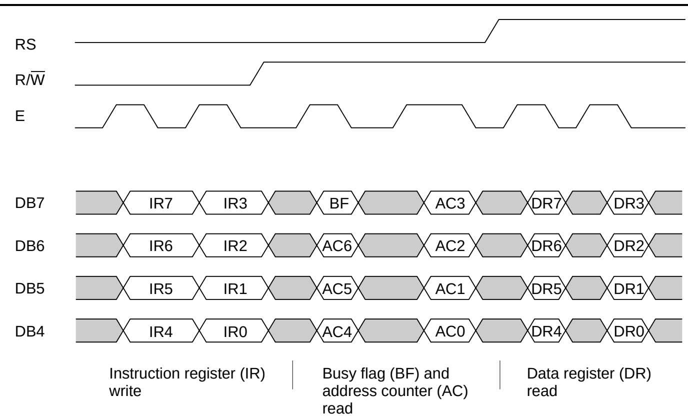


Figure 9 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initial-ization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD44780U can be controlled by the MPU. Before starting the internal operation of the HD44780U, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD44780U is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/

write signal (R/$\overline{W}$), and the data bus (DB0 to DB7), make up the HD44780U instructions (Table 6). There are four categories of instructions that:

- Designate HD44780U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD44780U RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (Table 11) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD44780U is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD44780U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Table 6 for the list of each instruc-tion execution time.

Table 6 Instructions

	Code											Execution Time (max) (when f_{cp} or
Instruction	**RS**	**R/$\overline{W}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Description**	**f_{osc} is 270 kHz)**
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 6 Instructions (cont)

Instruction	Code										Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Write data to CG or DDRAM	1	0	Write data								Writes data into DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
Read data from CG or DDRAM	1	1	Read data								Reads data from DDRAM or CGRAM.	37 µs t_{ADD} = 4 µs*
	I/D I/D S S/C S/C R/L R/L DL N F BF BF	= 1: = 0: = 1: = 1: = 0: = 1: = 0: = 1: = 1: = 1: = 1: = 0:	Increment Decrement Accompanies display shift Display shift Cursor move Shift to the right Shift to the left 8 bits, DL = 0: 4 bits 2 lines, N = 0: 1 line 5 × 10 dots, F = 0: 5 × 8 dots Internally operating Instructions acceptable								DDRAM: Display data RAM CGRAM: Character generator RAM ACG: CGRAM address ADD: DDRAM address (corresponds to cursor address) AC: Address counter used for both DD and CGRAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 250 kHz, $37\ \mu s \times \frac{270}{250} = 40\ \mu s$

Note: — indicates no effect.

* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

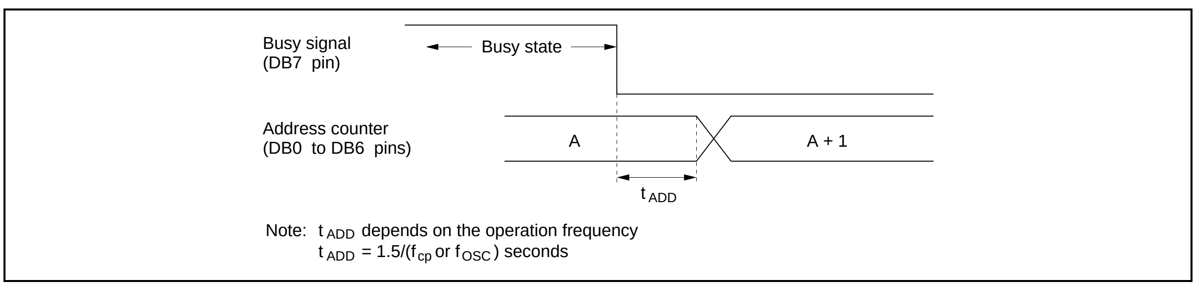


Figure 10 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DDRAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×8 dot character font selection and in the 11th line for the 5×10 dot character font selection (Figure 13).

B: The character indicated by the cursor blinks when B is 1 (Figure 13). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when f_{cp} or f_{OSC} is 250 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $409.6 \times 250/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (Table 7). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB7 to DB0) when DL is 1, and in 4-bit lengths (DB7 to DB4) when DL is 0.When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CGRAM Address

Set CGRAM address sets the CGRAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CGRAM.

		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear display	Code	0	0	0	0	0	0	0	0	0	1
Return home	Code	0	0	0	0	0	0	0	0	0	1
Entry mode set	Code	0	0	0	0	0	0	0	0	0	1
Display on/off control	Code	0	0	0	0	0	0	0	0	0	1

Note: * Don't care.

Figure 11

		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Cursor or display shift	Code	0	0	0	0	0	1	S/C	R/L	*	*
Function set	Code	0	0	0	0	0	DL	N	F	*	*
Set CGRAM address	Code	0	0	0	0	A	A	A	A	A	A

← Higher order bit   Lower order bit →

Note: * Don't care.

Figure 12

Set DDRAM Address

Set DDRAM address sets the DDRAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DDRAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DDRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CGRAM address and set DDRAM address.

Table 7 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 8 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 8 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 8 dots	1/16	Cannot display two lines for 5 × 10 dot character font

Note: * Indicates don’t care.

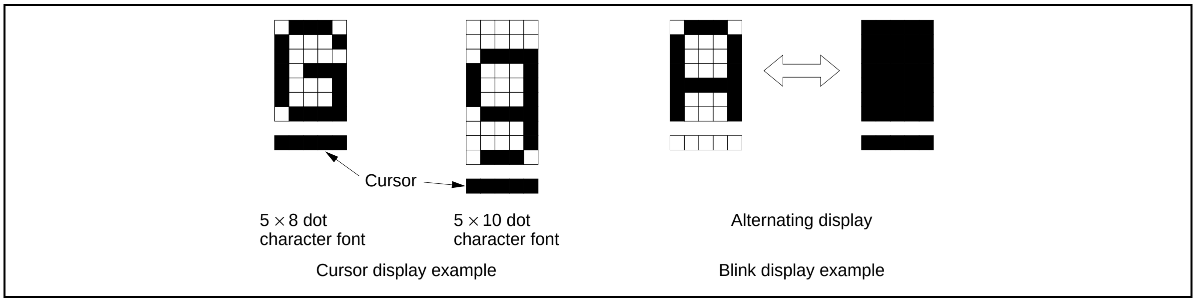


Figure 13 Cursor and Blinking

Set DDRAM address

	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	A	A	A	A	A	A	A

← Higher order bit   Lower order bit →

Read busy flag and address

	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher order bit   Lower order bit →

Figure 14

Write Data to CG or DDRAM

Write data to CG or DDRAM writes 8-bit binary data DDDDDDDD to CG or DDRAM.

To write into CG or DDRAM is determined by the previous specification of the CGRAM or DDRAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DDRAM

Read data from CG or DDRAM reads 8-bit binary data DDDDDDDD from CG or DDRAM.

The previous designation determines whether CG or DDRAM is to be read. Before entering this read instruction, either CGRAM or DDRAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DDRAM). The operation of the cursor shift instruction is the same as the set DDRAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CGRAM or DDRAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DDRAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write data to CG or DDRAM	Code	1	0	D	D	D	D	D	D	D	D
			← Higher order bits						Lower order bits →		

		RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read data from CG or DDRAM	Code	1	1	D	D	D	D	D	D	D	D
			← Higher order bits						Lower order bits →		

Figure 15

Interfacing the HD44780U

Interface to MPUs

- Interfacing to an 8-bit MPU

  See Figure 17 for an example of using a I/O port (for a single-chip microcomputer) as an interface device.

  In this example, P30 to P37 are connected to the data bus DB0 to DB7, and P75 to P77 are connected to E, R/$\overline{W}$, and RS, respectively.

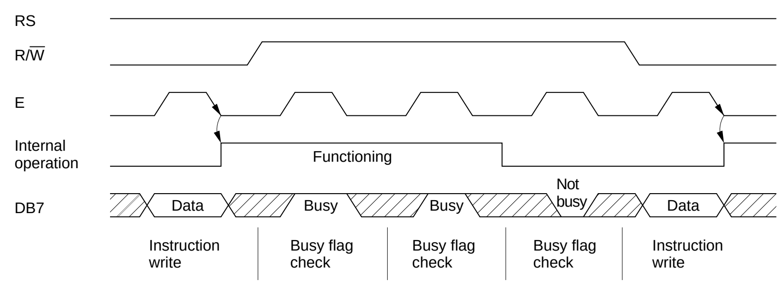


Figure 16 Example of Busy Flag Check Timing Sequence

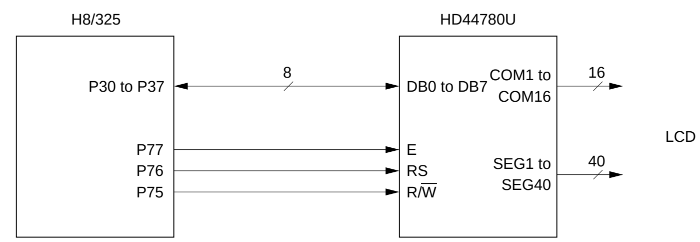


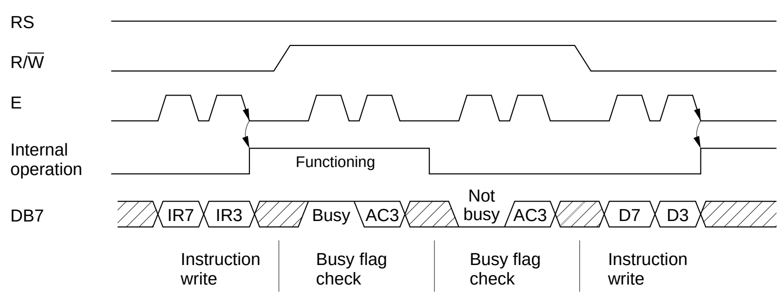
Figure 17 H8/325 Interface (Single-Chip Mode)

- Interfacing to a 4-bit MPU

  The HD44780U can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See Figure 18.)

  See Figure 19 for an interface example to the HMCS4019R.

  Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.



Note: IR7 , IR3 are the 7th and 3rd bits of the instruction.
AC3 is the 3rd bit of the address counter.

Figure 18 Example of 4-Bit Data Transfer Timing Sequence

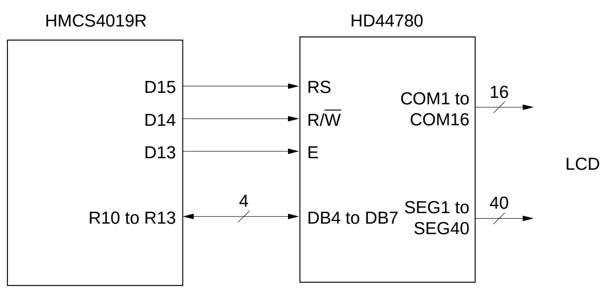


Figure 19 Example of Interface to HMCS4019R

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD44780U can perform two types of displays, 5 × 8 dot and 5 × 10 dot character fonts, each with a cursor.

Up to two lines are displayed for 5 × 8 dots and one line for 5 × 10 dots. Therefore, a total of three

types of common signals are available (Table 9).

The number of lines and font types can be selected by the program. (See Table 6, Instructions.)

Connection to HD44780 and Liquid Crystal Display: See Figure 20 for the connection examples.

Table 9 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 8 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 8 dots + cursor	16	1/16

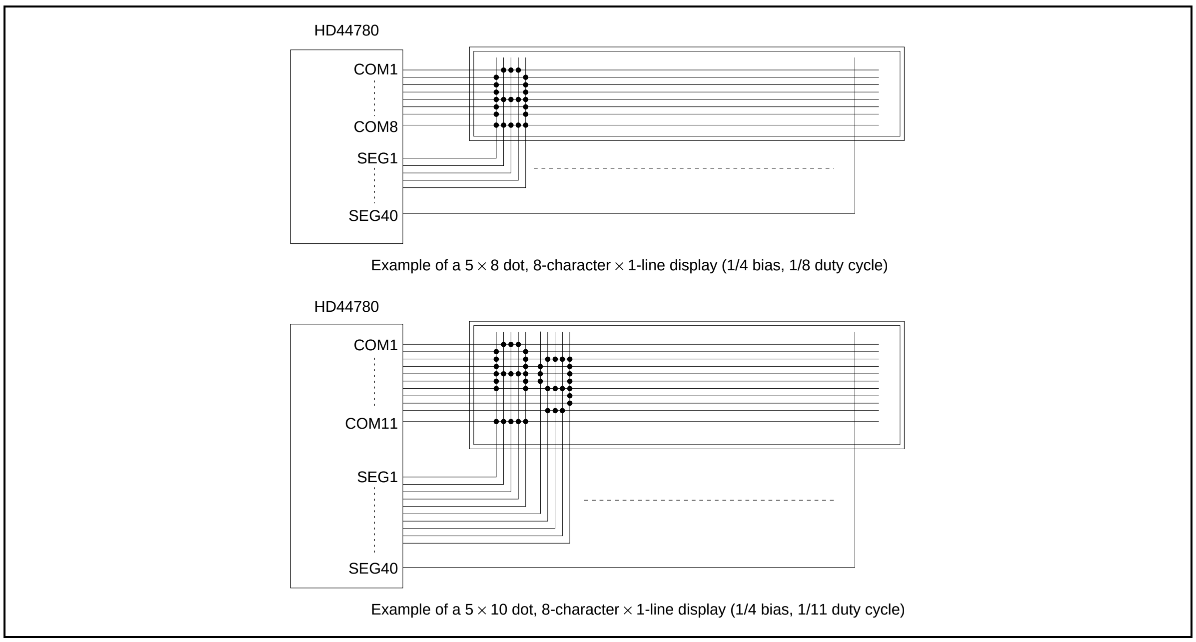


Figure 20 Liquid Crystal Display and HD44780 Connections

Since five segment signal lines can display one digit, one HD44780U can display up to 8 digits for a 1-line display and 16 digits for a 2-line display.

The examples in Figure 20 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (Figure 21).

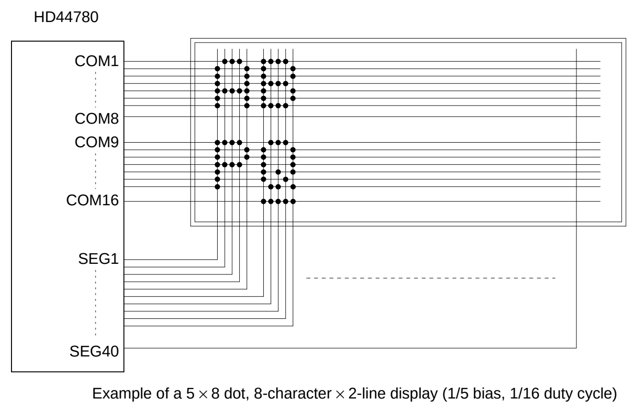


Figure 20 Liquid Crystal Display and HD44780 Connections (cont)

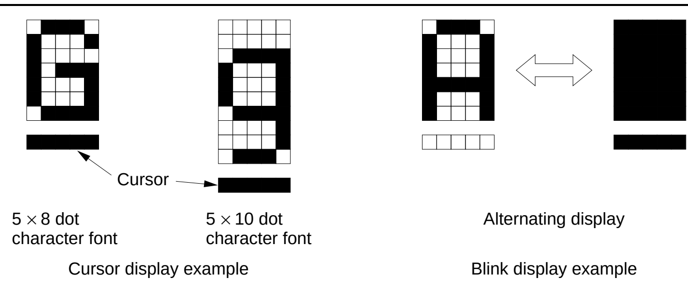


Figure 21 Using COM9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (Figure 22) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DDRAM) addresses for 4 characters $\times$ 2 lines and for 16 characters $\times$ 1 line are the same as in Figure 20.

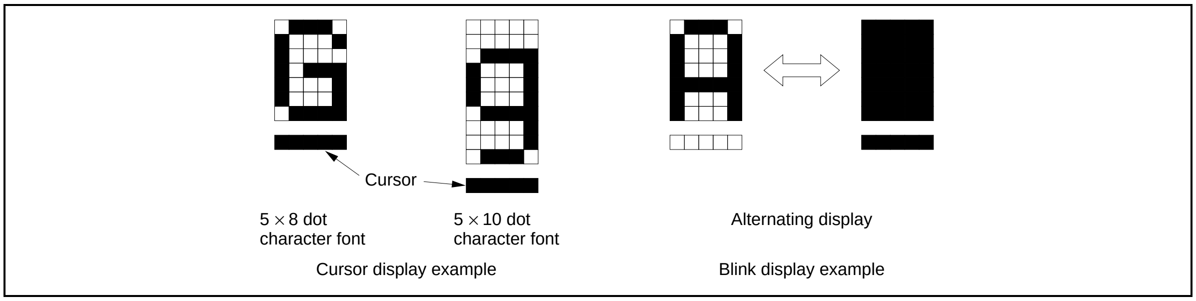


Figure 22 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V1 to V5 of the HD44780U to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (Table 10).

VLCD is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V1 to V5 (Figure 23).

Table 10 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Power Supply	1/4	1/5
V1	V_{cc}–1/4 VLCD	V_{cc}–1/5 VLCD
V2	V_{cc}–1/2 VLCD	V_{cc}–2/5 VLCD
V3	V_{cc}–1/2 VLCD	V_{cc}–3/5 VLCD
V4	V_{cc}–3/4 VLCD	V_{cc}–4/5 VLCD
V5	V_{cc}–VLCD	V_{cc}–VLCD

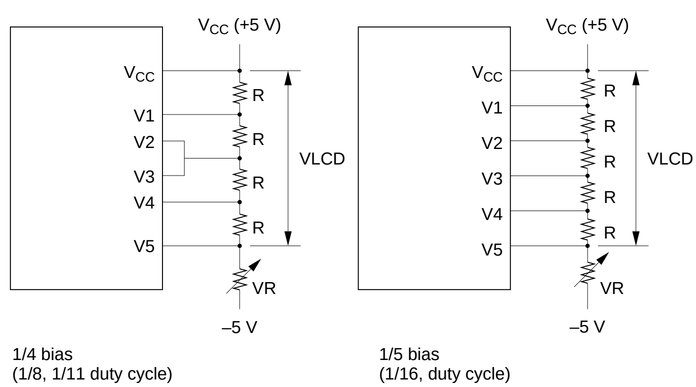
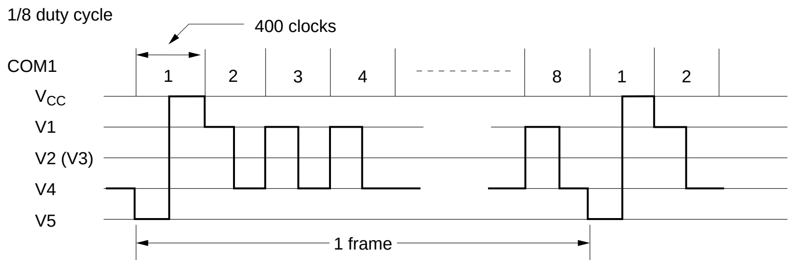


Figure 23 Drive Voltage Supply Example

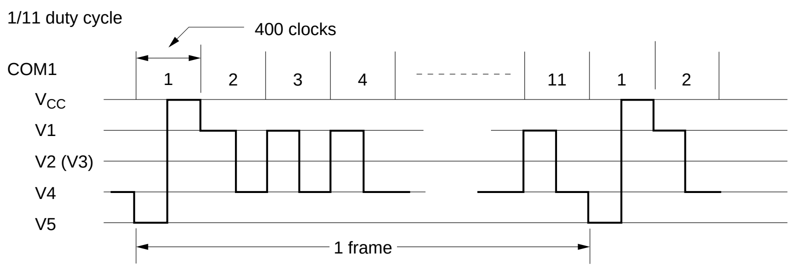
Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of Figure 24 apply only when the oscillation frequency is 270 kHz (one clock pulse of 3.7 µs).



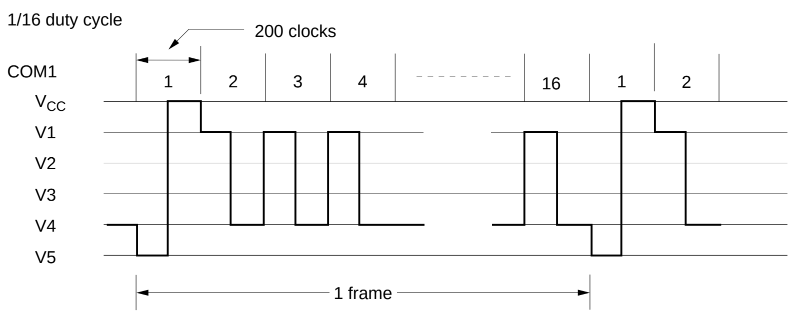
1 frame = 3.7 µs × 400 × 8 = 11850 µs = 11.9 ms

Frame frequency = $\frac{1}{11.9\ \text{ms}}$ = 84.3 Hz



1 frame = 3.7 µs × 400 × 11 = 16300 µs = 16.3 ms

Frame frequency = $\frac{1}{16.3\ \text{ms}}$ = 61.4 Hz



1 frame = 3.7 µs × 200 × 16 = 11850 µs = 11.9 ms

Frame frequency = $\frac{1}{11.9\ \text{ms}}$ = 84.3 Hz

Figure 24 Frame Frequency

Instruction and Display Correspondence

- 8-bit operation, 8-digit × 1-line display with internal reset

  Refer to Table 11 for an example of an 8-digit × 1-line display in 8-bit operation. The HD44780U functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

  Since the display shift operation changes only the display position with DDRAM contents unchanged, the first display data entered into DDRAM can be output when the return home operation is performed.

- 4-bit operation, 8-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (Table 12). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB0 to DB3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see Table 12). Thus, DB4 to DB7 of the function set instruction is written twice.

- 8-bit operation, 8-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be again set after the 8th character is completed. (See Table 13.) Note that the display shift operation is performed for the first and second lines. In the example of Table 13, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD44780U must be initialized by instructions. See the section, Initializing by Instruction.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set 0	0	0	0	1	1	0	0	*	*		Sets to 8-bit operation and selects 1-line display and 5 × 8 dot character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control 0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set 0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	0	H_	Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	1	HI_	Writes I.
7						· · · · ·					· · · · ·	
8	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
9	Entry mode set 0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CGRAM/DDRAM 1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset (cont)

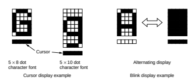
Step No.	Instruction: RS	$R/\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
11	Write data to CGRAM/DDRAM											Writes M.
	1	0	0	1	0	0	1	1	0	1		
12					· · · · ·						· · · · ·	
13	Write data to CGRAM/DDRAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CGRAM/DDRAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CGRAM/DDRAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20					· · · · ·						· · · · ·	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 12 4-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)							Initialized. No display.
2	Function set 0	 0	 0	 0	 1	 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function set 0 0	 0 0	 0 0	 0 0	 1 *	 0 *		Sets 4-bit operation and selects 1-line display and 5 × 8 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
4	Display on/off control 0 0	 0 0	 0 1	 0 1	 0 1	 0 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry mode set 0 0	 0 0	 0 0	 0 1	 0 1	 0 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
6	Write data to CGRAM/DDRAM 1 1	 0 0	 0 1	 1 0	 0 0	 0 0	H_	Writes H. The cursor is incremented by one and shifts to the right.

Note: The control is the same as for 8-bit operation beyond step #6.

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset

Step	Instruction											
No.	**RS**	**$R/\overline{W}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Display**	**Operation**
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display and 5 × 8 dot character font.
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control										_	Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CGRAM/DDRAM										H_	Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
	1	0	0	1	0	0	1	0	0	0		
6						. . . . .					. . . . .	
7	Write data to CGRAM/DDRAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	Set DDRAM address										HITACHI _	Sets DDRAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0		

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
9	Write data to CGRAM/DDRAM										HITACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
10						· · · · ·					· · · · ·	
11	Write data to CGRAM/DDRAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CGRAM/DDRAM										ITACHI ICROCOM_	Writes M. Display is shifted to the left. The first and second lines both shift at the same time.
	1	0	0	1	0	0	1	1	0	1		
14						· · · · ·					· · · · ·	
15	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to Figures 25 and 26 for the procedures on 8-bit and 4-bit initializations, respectively.

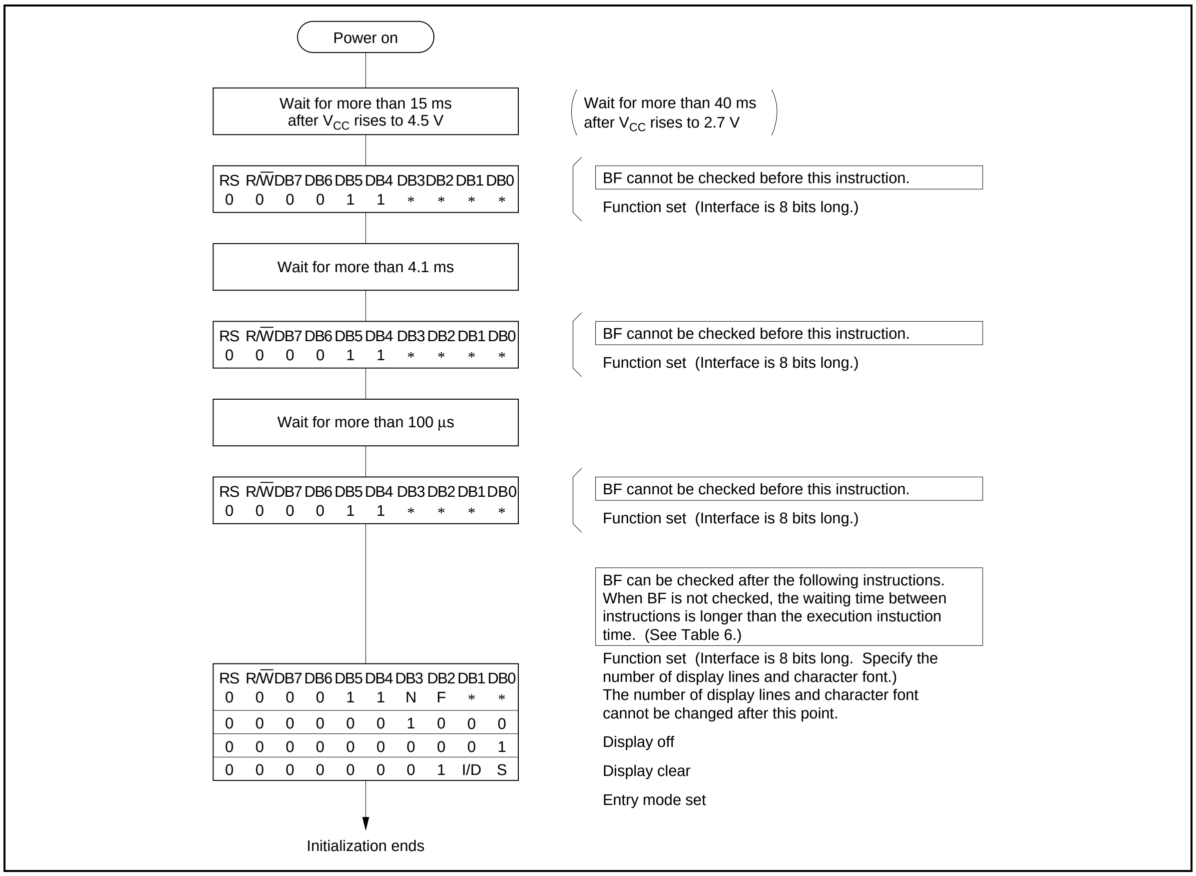


Figure 25 8-Bit Interface

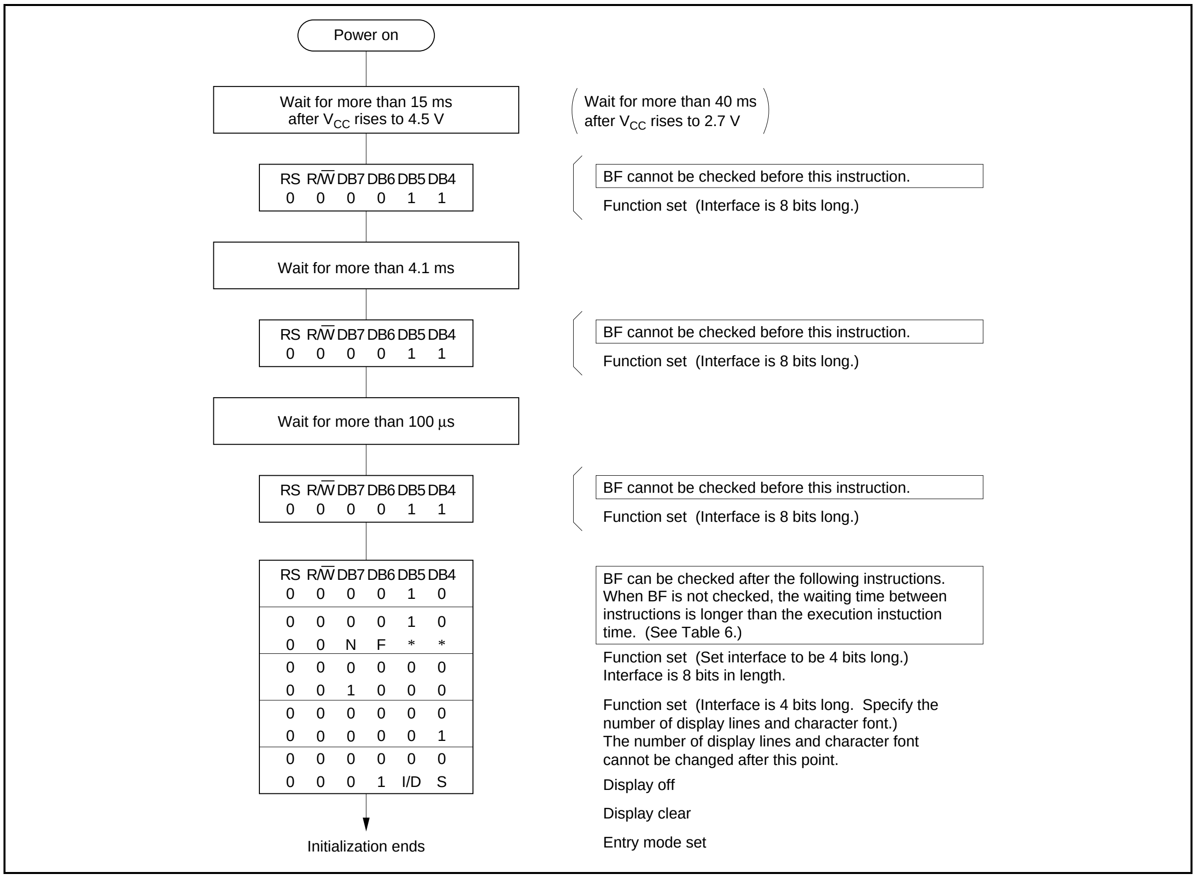


Figure 26 4-Bit Interface

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}–GND	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +13.0	V	1, 2
Input voltage	Vt	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 to 4.5 V, T_a = –20 to +75°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC1)	VIL1	–0.3	—	0.55	V		6
Input high voltage (2) (OSC1)	VIH2	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (DB0–DB7)	VOH1	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (DB0–DB7)	VOL1	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except DB0–DB7)	VOH2	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB0–DB7)	VOL2	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	2	20	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	2	30	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	VIN = 0 to V_{CC}	9
Pull-up MOS current (DB0–DB7, RS, R/$\overline{W}$)	$-I_p$	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	VLCD1	3.0	—	11.0	V	V_{CC}–V5, 1/5 bias	16
	VLCD2	3.0	—	11.0	V	V_{CC}–V5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 to 4.5 V, T_a = –20 to +75°C*[3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Note*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	μs		
	External clock fall time	t_{fcp}	—	—	0.2	μs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 75 kΩ, V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 27
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 28
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 29
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 30
Power supply off time	t_{OFF}	1	—	—		

DC Characteristics (V_{CC} = 4.5 to 5.5 V, T_a = –20 to +75°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	2.2	—	V_{CC}	V		6
Input low voltage (1) (except OSC1)	VIL1	–0.3	—	0.6	V		6
Input high voltage (2) (OSC1)	VIH2	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	1.0	V		15
Output high voltage (1) (DB0–DB7)	VOH1	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	7
Output low voltage (1) (DB0–DB7)	VOL1	—	—	0.4	V	I_{OL} = 1.2 mA	7
Output high voltage (2) (except DB0–DB7)	VOH2	0.9 V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB0–DB7)	VOL2	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	RCOM	—	2	20	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Driver on resistance (SEG)	RSEG	—	2	30	kΩ	±Id = 0.05 mA, VLCD = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	VIN = 0 to V_{CC}	9
Pull-up MOS current (DB0–DB7, RS, R/$\overline{W}$)	$-I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}	—	0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	VLCD1	3.0	—	11.0	V	V_{CC}–V5, 1/5 bias	16
	VLCD2	3.0	—	11.0	V	V_{CC}–V5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 4.5 to 5.5 V, T_a = –20 to +75°C*[3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	μs		11
	External clock fall time	t_{fcp}	—	—	0.2	μs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ V_{CC} = 5.0 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 27
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 28
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

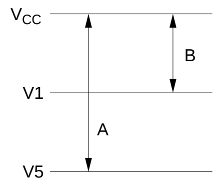
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 29
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 30
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

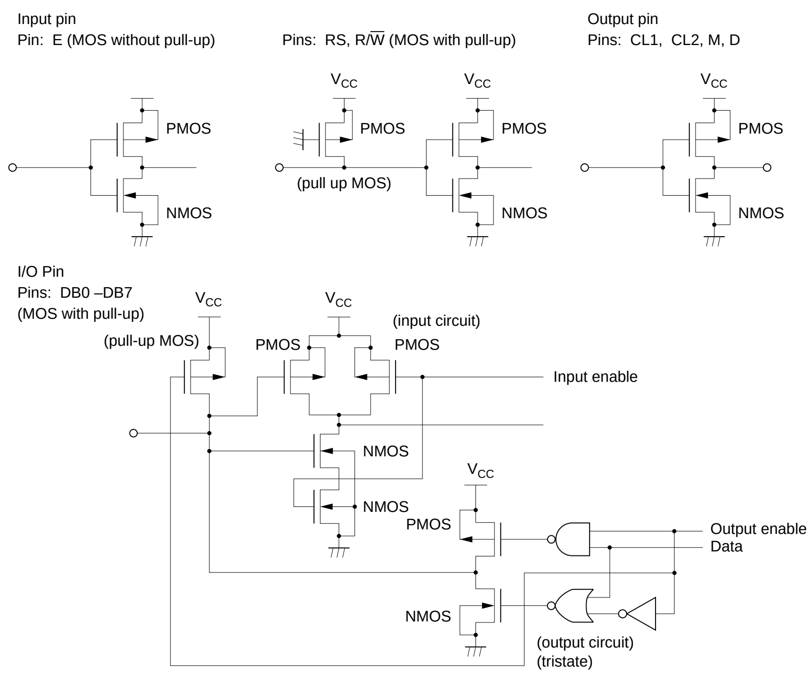
1. All voltage values are referred to GND = 0 V.



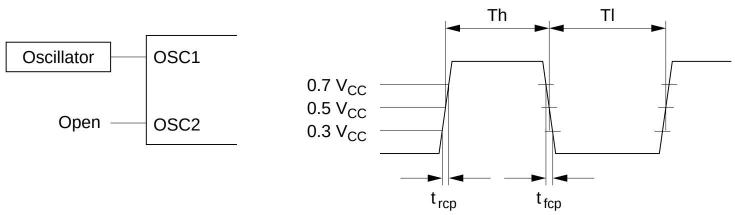
A = V_{CC} –V5
B = V_{CC} –V1
A ≥ 1.5 V
B ≤ 0.25 × A

The conditions of V1 and V5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified as LCD voltage VLCD.

2. V_{CC} ≥ V1 ≥ V2 ≥ V3 ≥ V4≥V5 must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

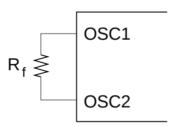


6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull–up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.

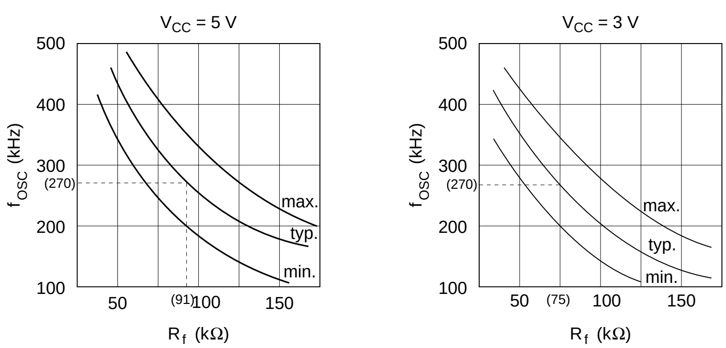


$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



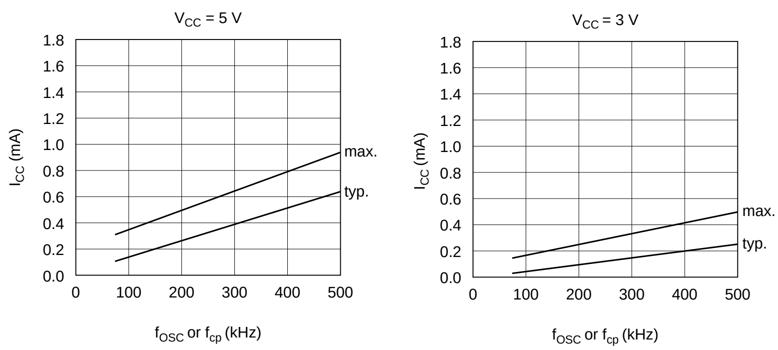
R_f: 75 kΩ ± 2% (when V_{CC} = 3 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.



13. RCOM is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM1 to COM16).

    RSEG is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

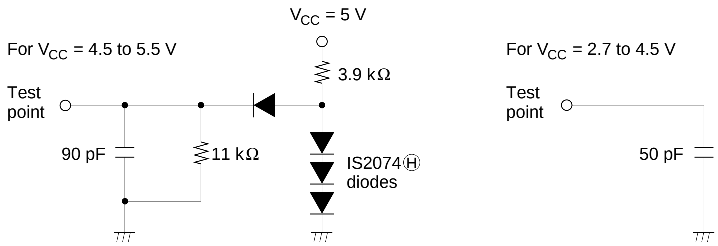
14. The following graphs show the relationship between operation frequency and current consumption.



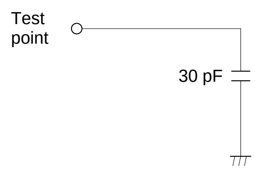
15. Applies to the OSC1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

Load Circuits

Data Bus DB0 to DB7



External Driver Control Signals: CL1, CL2, D, M



Timing Characteristics

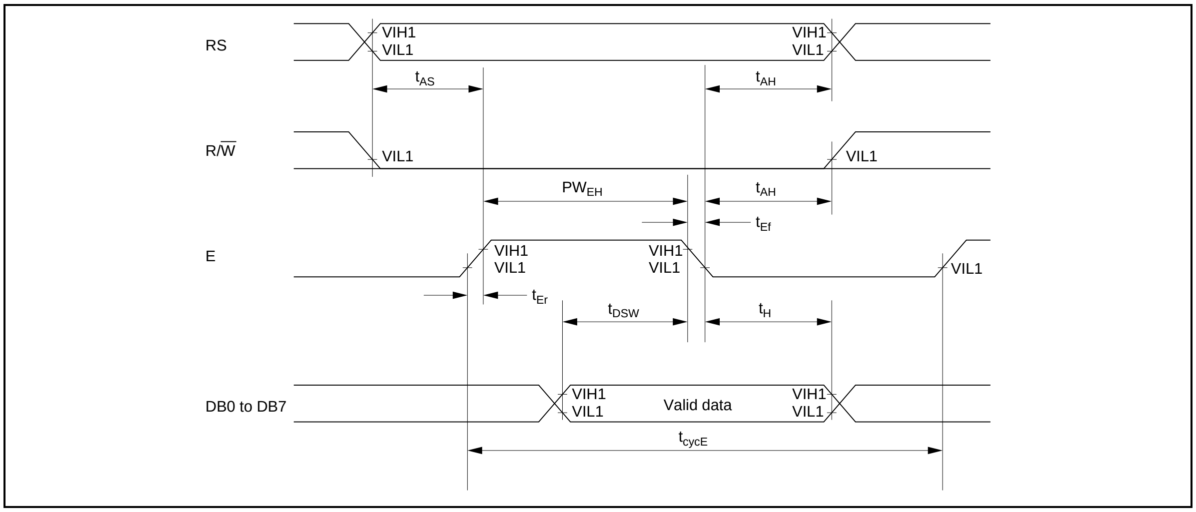


Figure 27 Write Operation

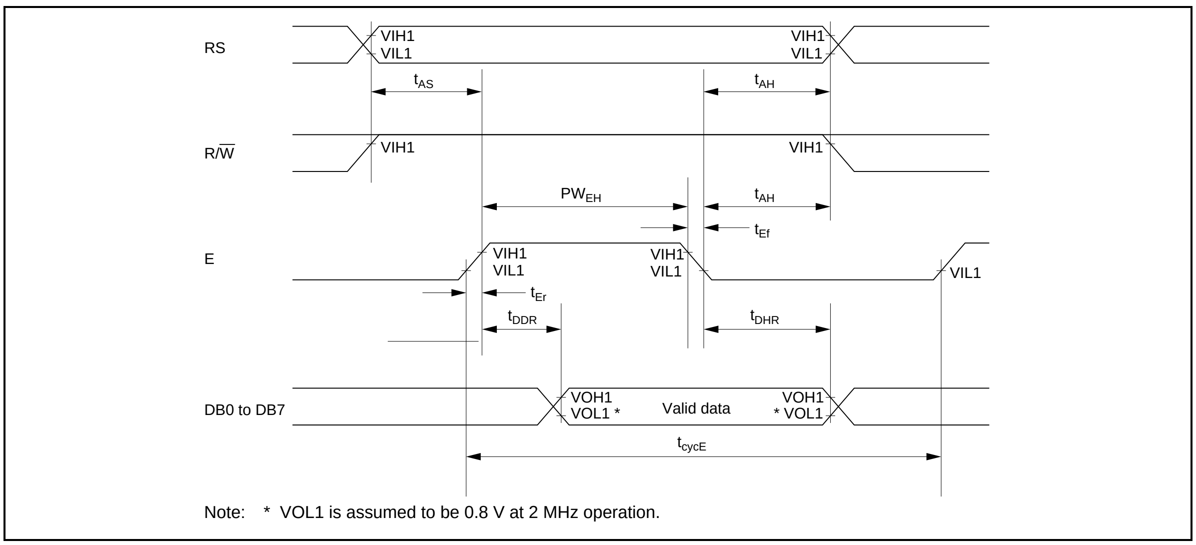


Figure 28 Read Operation

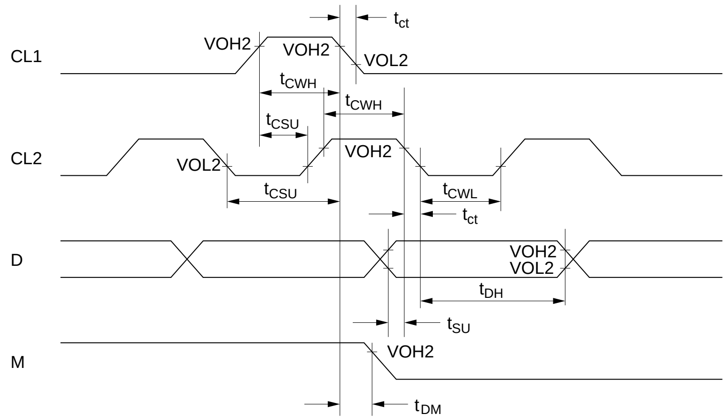
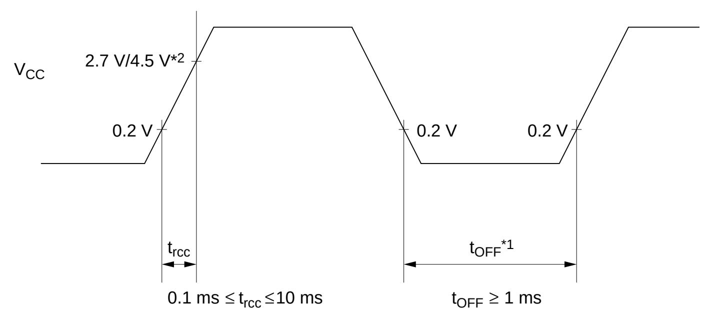


Figure 29 Interface Timing with External Driver



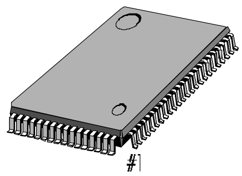
Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. For if 4.5 V is not reached during 5-V operation, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 30 Internal Power Supply Reset

INTRODUCTION

KS0066U is a dot matrix LCD driver & controller LSI whichis fabricated by low power CMOS technology.
It can display 1or 2 lines with the 5×8 dots format or 1 line with the 5×11 dots format.

80 QFP-1420C



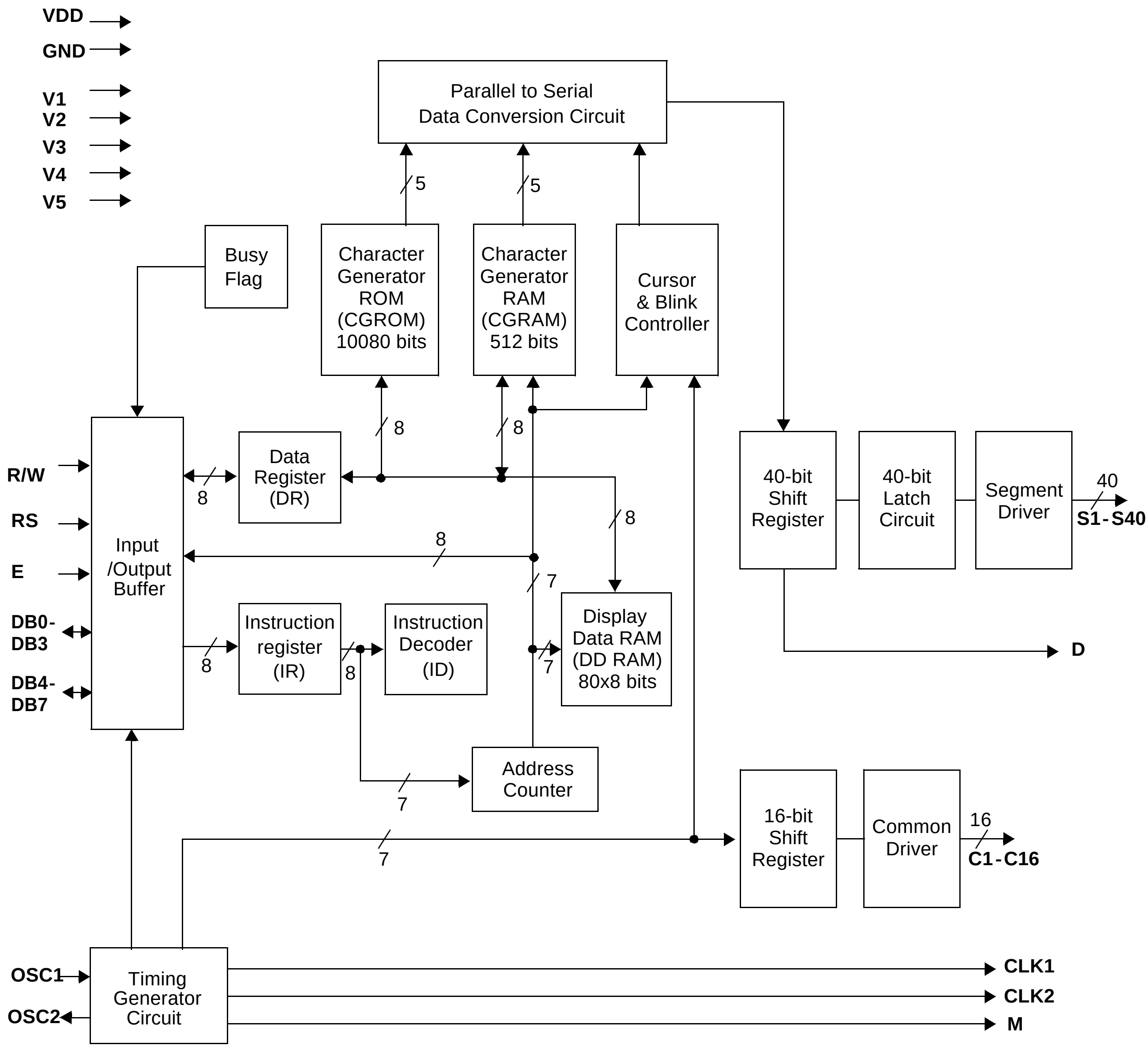
FUNCTIONS

- Character type dot matrix LCD driver & controller.
- Internal driver: 16 common and 40 segment signal output.
- Easy interface with 4-bit or 8-bit MPU.
- Display character pattern: 5×8 dots format (208 kinds) & 5×11 dots format (32 kinds).
- The Special character pattern is directly programmable by the Character Generator RAM.
- A customer character pattern is programmable by mask option.
- Programmable Driving Method by the same character font mask option: Display Waveform A-type and B-type
- It can drive a maximum at 80 characters by using the KS0065B or KS0063B externally.
- Various instruction functions.
- Built-in automatic power on reset.

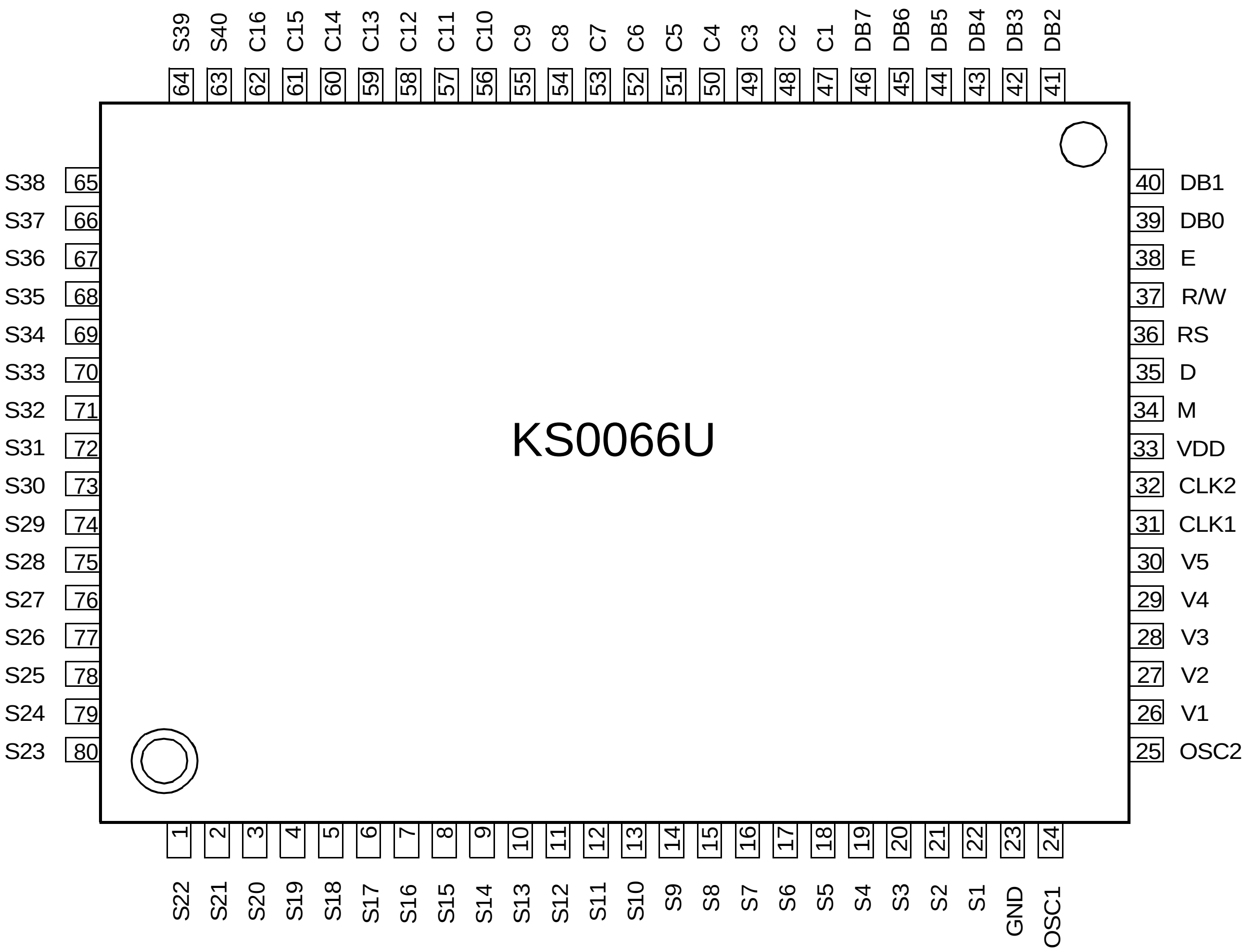
FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 10,080 bits (204 characters×5×8 dots) & (32 characters×5×11 dots)
  - Character Generator RAM (CGRAM): 64×8 bits (8 characters×5×8 dots)
  - Display Data RAM (DDRAM): 80×8 bits (80 characters max.)
- Low power operation
  - Power supply voltage range (VDD): 2.7 to 5.5 V
  - LCD Drive voltage range (VDD–V5): 3.0 to 13.0 V
- CMOS process
- Programmable duty cycle: 1/8, 1/11, 1/16
- Internal oscillator with external resistor
- Low power consumption
- 80 QFP or bare chip available

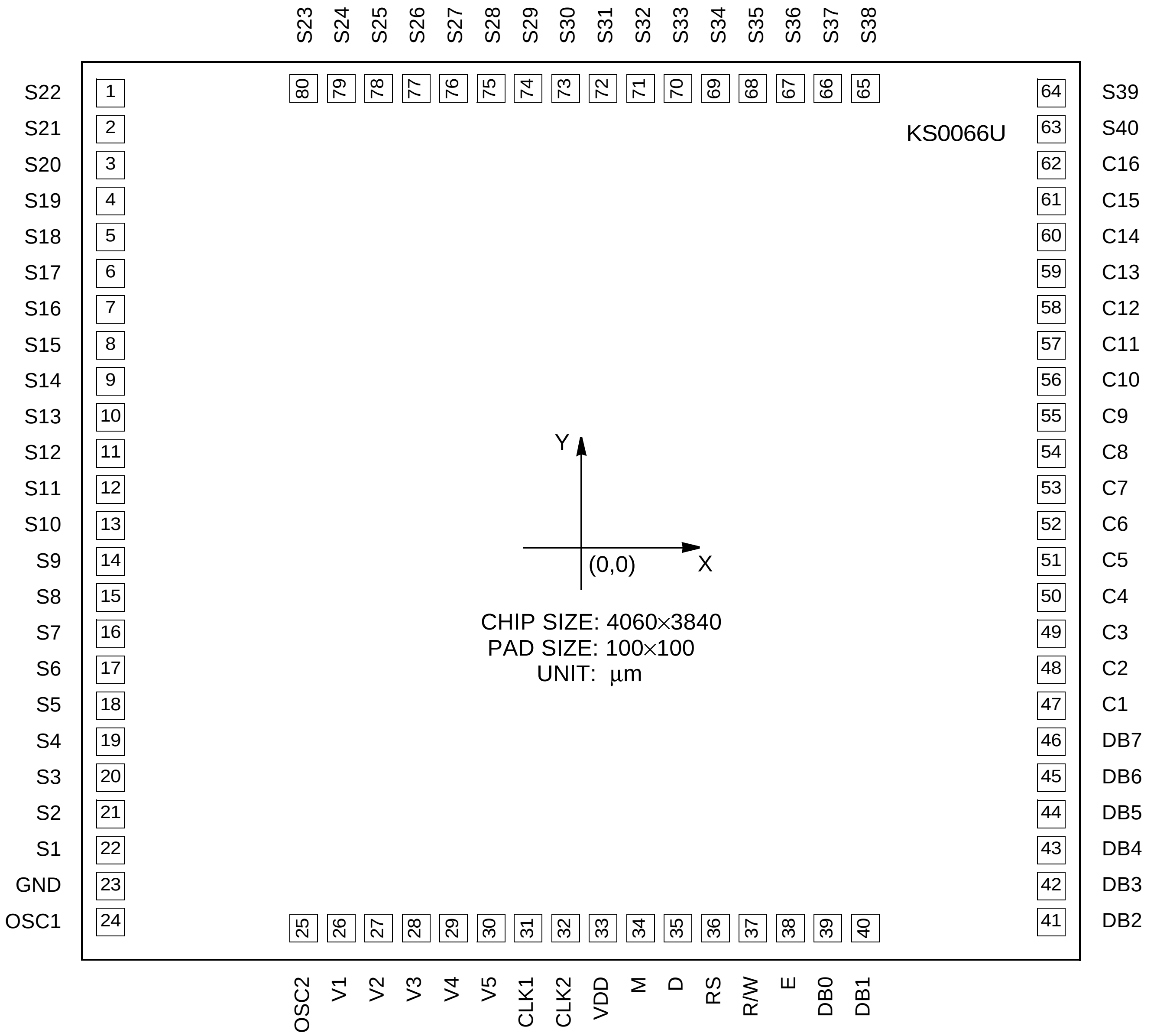
BLOCK DIAGRAM



PIN CONFIGURATION



PAD DIAGRAM



NOTE: “KS0066U” marking is to make the PAD No. 65 easy to find.

PAD LOCATION

Table 1. Pad Location **(Unit: mm)**

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y			X	Y
1	S22	-1864	1465	21	S2	-1864	-1034	41	DB2	1864	-1488	61	C15	1864	1085
2	S21	-1864	1340	22	S1	-1864	-1159	42	DB3	1864	-1362	62	C16	1864	1210
3	S20	-1864	1215	23	GND	-1864	-1285	43	DB4	1864	-1238	63	S40	1864	1341
4	S19	-1864	1090	24	OSC1	-1864	-1414	44	DB5	1864	-1112	64	S39	1864	1466
5	S18	-1864	965	25	OSC2	-1120	-1754	45	DB6	1864	-988	65	S38	886	1754
6	S17	-1864	840	26	V1	-970	-1754	46	DB7	1864	-862	66	S37	760	1754
7	S16	-1864	715	27	V2	-820	-1754	47	C1	1864	-665	67	S36	636	1754
8	S15	-1864	590	28	V3	-670	-1754	48	C2	1864	-540	68	S35	510	1754
9	S14	-1864	465	29	V4	-520	-1754	49	C3	1864	-415	69	S34	386	1754
10	S13	-1864	340	30	V5	-370	-1754	50	C4	1864	-290	70	S33	260	1754
11	S12	-1864	215	31	CLK1	-220	-1754	51	C5	1864	-165	71	S32	136	1754
12	S11	-1864	90	32	CLK2	-70	-1754	52	C6	1864	-40	72	S31	10	1754
13	S10	-1864	-35	33	VDD	80	-1754	53	C7	1864	85	73	S30	-114	1754
14	S9	-1864	-160	34	M	230	-1754	54	C8	1864	210	74	S29	-240	1754
15	S8	-1864	-285	35	D	380	-1754	55	C9	1864	335	75	S28	-364	1754
16	S7	-1864	-410	36	RS	518	-1754	56	C10	1864	460	76	S27	-490	1754
17	S6	-1864	-535	37	R/W	642	-1754	57	C11	1864	585	77	S26	-614	1754
18	S5	-1864	-660	38	E	768	-1754	58	C12	1864	710	78	S25	-740	1754
19	S4	-1864	-785	39	DB0	894	-1754	59	C13	1864	835	79	S24	-864	1754
20	S3	-1864	-910	40	DB1	1018	-1754	60	C14	1864	960	80	S23	-989	1754

PIN DESCRIPTION

Table 2. Pin Description

Pin	Pin No.	I/O	Name	Description	Interface
VDD	33	-	Supply Voltage	Supply Voltage for logical circuit (+3V ± 10%,+5V ± 10%)	Power Supply
GND	23			Ground (0V)	
V1-V5	26-30			Bias voltage level for LCD driving	
S1-S40	1-22, 63-80	O	Segment output	Segment signal output for LCD drive	LCD
C1-C16	47-62	O	Common output	Common signal output for LCD drive	LCD
OSC1	24	I	Oscillator	Oscillator. When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/oscillator (OSC1)
OSC2	25	O	Oscillator		
CLK1	31	O	Extension driver Latch clock	Extension driver latch clock	Extension driver
CLK2	32	O	Extension driver Shift clock	Extension driver shift clock	
M	34	O	Alternated signal for LCD driver output	Outputs the alternating signal to convert LCD driver waveform to AC.	Extension driver
D	35	O	Display data interface	Outputs extension driver data (the 41st dot's data)	Extension driver
RS	36	I	Register select	Used as register selection input. When RS = "High", Data register is selected. When RS = "Low", Instruction register is selected.	MPU
R/W	37	I	Read/Write	Used as read/write selection input. When RW = "High", read operation. When RW = "Low", write operation.	MPU
E	38	I	Read/Write enable	Used as read/write enable signal.	MPU
DB0-DB3	39-42	I/O	Data bus 0-7	In 8-bit bus mode, used as low order bidirectional data bus. In 4-bit bus mode, open these pins.	MPU
DB4-DB7	43-46			In 8-bit bus mode, used as high order bidirectional data bus. In 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output.	MPU

FUNCTION DESCRIPTION

System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used.
One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction.
Each internal operation, reading from or writing into RAM, is done automatically.
Thus, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction codes transferred from MPU.
MPU cannot use it to read instruction data.

To select a register, you can use RS input pin in 4-bit/8-bit bus mode.

Table 3. Various kinds of Operations according to RS and R/W bits

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy flag(DB7) and address counter (DB0 to DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

BF = “High”, indicates that the internal operation is being processed.
So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = “Low” and R/W = “High” (Read Instruction Operation).
Before executing the next instruction, be sure that BF is not “High”.

Address Counter (AC)

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = “Low” and R/W = “High”, AC can be read through ports DB0 to DB6.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80×8 bits (80 characters).
DDRAM address is set in the address counter(AC) as a hexadecimal number (Refer to Fig-1.)

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

Figure 1 . DDRAM Address

1) 1-line display
In case of 1-line display, the address range of DDRAM is 00H–4FH.
An extension driver will be used. Fig-2 shows the example with 40 segment extension driver added.

Display position

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1–COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17

SEG1 KS0066U SEG40 | SEG1 Extension Driver (40SEG) SEG40 | SEG1 Extension Driver (40SEG) SEG40

DDRAM address

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1–COM8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18

SEG1 KS0066U SEG40 | SEG1 Extension Driver (40SEG) SEG40 | SEG1 Extension Driver (40SEG) SEG40

(After Shift Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1–COM8	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16

SEG1 KS0066U SEG40 | SEG1 Extension Driver (40SEG) SEG40 | SEG1 Extension Driver (40SEG) SEG40

(After Shift Right)

Figure 2 . 1-line ´ 24 char. display with 40 SEG. extension driver

2) 2-line display

In case of 2-line display, the address range of DDRAM is 00H–27H and 40H–67H.
An extension driver will be used. Fig-3 shows the example with 40 segment extension driver added.

Display position / DDRAM address

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1–COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
COM9–COM16	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57

SEG1 KS0066U SEG40 | SEG1 Extension Driver (40SEG) SEG40 | SEG1 Extension Driver (40SEG) SEG40

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1–COM8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
COM9–COM16	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58

SEG1 KS0066U SEG40 | SEG1 Extension Driver (40SEG) SEG40 | SEG1 Extension Driver (40SEG) SEG40

(After Shift Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1–COM8	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
COM9–COM16	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	5E	4F	50	51	52	53	54	55	56

SEG1 KS0066U SEG40 | SEG1 Extension Driver (40SEG) SEG40 | SEG1 Extension Driver (40SEG) SEG40

(After Shift Right)

Figure 3 . 2-line ´ 24 char. display with 40 SEG. extension driver

CGROM(Character Generator ROM)

CGROM has a 5×8 dots 204 characters pattern and a 5×11 dots 32 characters pattern (Refer to Table 4).
CGROM has 204 character patterns of 5× 8 dots, and 32 character patterns of 5×11 dots.

CGRAM(Character Generator RAM)

CGRAM has up to 5×8 dots 8 characters.
By writing font data to CGRAM, user defined characters can be used (Refer to Table 5)

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit

LCD Driver circuit has 16 common and 40 segment signals for LCD driving.
Data from CGRAM/CGROM is transferred to a 40-bit segment latch serially, and then is stored to 40-bit shift latch.
When each common is selected by 16-bit common register, segment data is also output through segment driver from a 40-bit segment latch.
In case of 1-line display mode, COM1 to COM8 have 1/8 duty or COM1 to COM11 have 1/11 duty,
and in 2-line mode, COM1 to COM16 have a 1/16 duty ratio.

Cursor/Blink Control Circuit

It controls the cursor/blink ON/OFF at cursor position.

Table 4. CGROM Character Code Table

Table 5. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	0	1	1	1	0	pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
			⋮						⋮		0	1	1		⋮		1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
			⋮							⋮								⋮				⋮
0	0	0	0	×	1	1	1	0	0	0	0	0	0	×	×	×	1	0	0	0	1	pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
			⋮						⋮		0	1	1		⋮		1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control informations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 7).
Instructions can be divided largely into four groups:

1) KS0066U function set instructions (set display methods, set data length, etc.)
2) address set instructions to internal RAM
3) data transfer instructions with internal RAM
4) others

The address of the internal RAM is automatically increased or decreased by 1.

Note: During internal operation, Busy Flag (DB7) is read "High".
Busy Flag check must be preceded by the next instruction.
When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address,
and set DDRAM address to "00H" into AC (address counter).
Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display.
Make the entry mode increment (I/D = "High").

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

* "- ": dont care

Return Home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH = "Low", shifting of entire display is not performed.
If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value
(I/D = "High": shift left, I/D = "Low": shift right).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data remains in DDRAM.

C: Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, which performs alternately between all the "High" data and
display characters at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.(Refer to Table 6)
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

Table 6. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.

F: Display font type control bit
When F = "Low", 5 $\times$8 dots format display mode is set.
When F = "High", 5 $\times$11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = Low), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = High), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not.
If the resultant BF is "High", internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not Yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.
After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

Table 7. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc= 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.53 ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 µs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 µs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5×11dots/5×8 dots)	39 µs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 µs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 µs

* "-": dont care

NOTE: When an MPU program with checking the Busy Flag(DB7) is made, it must be necessary 1/2Fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

INTERFACE WITH MPU

1) Interface with 8-bit MPU

When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.

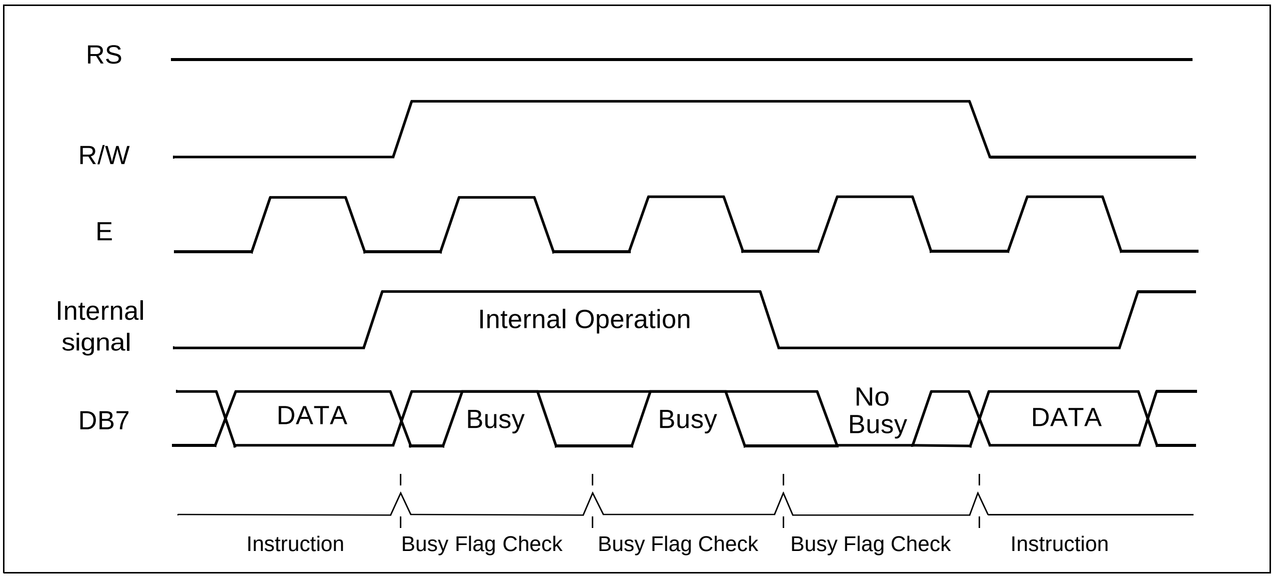


Figure 4 . Example of 8-bit Bus Mode Timing Diagram

2) Interface with 4-bit MPU

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At First, the higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7), and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed twice
Busy Flag outputs "High" after the second transfer is ended.
Example of timing sequence is shown below.

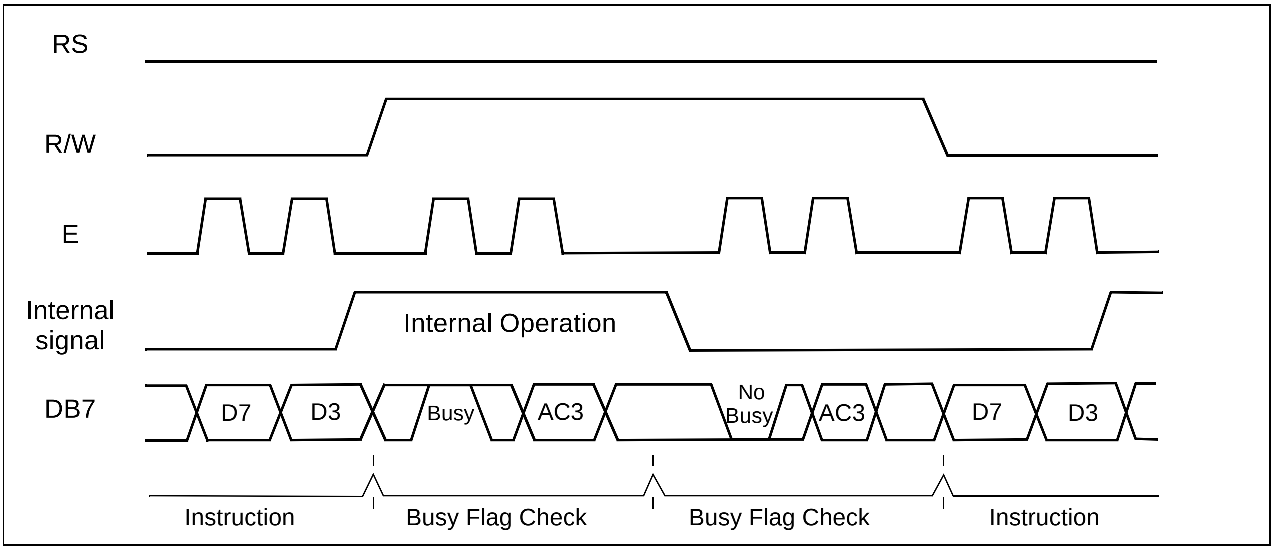
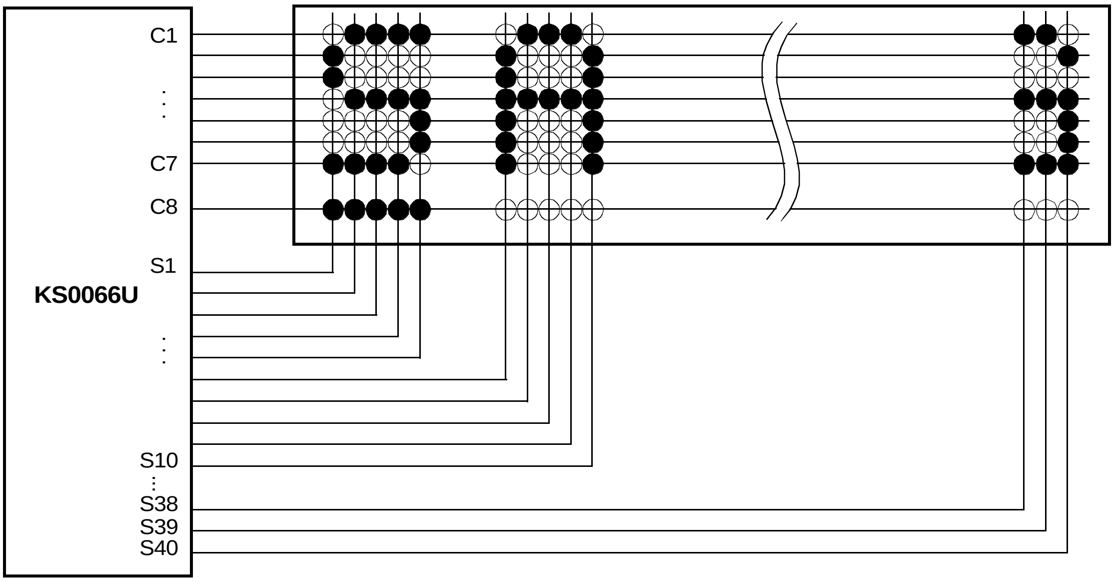


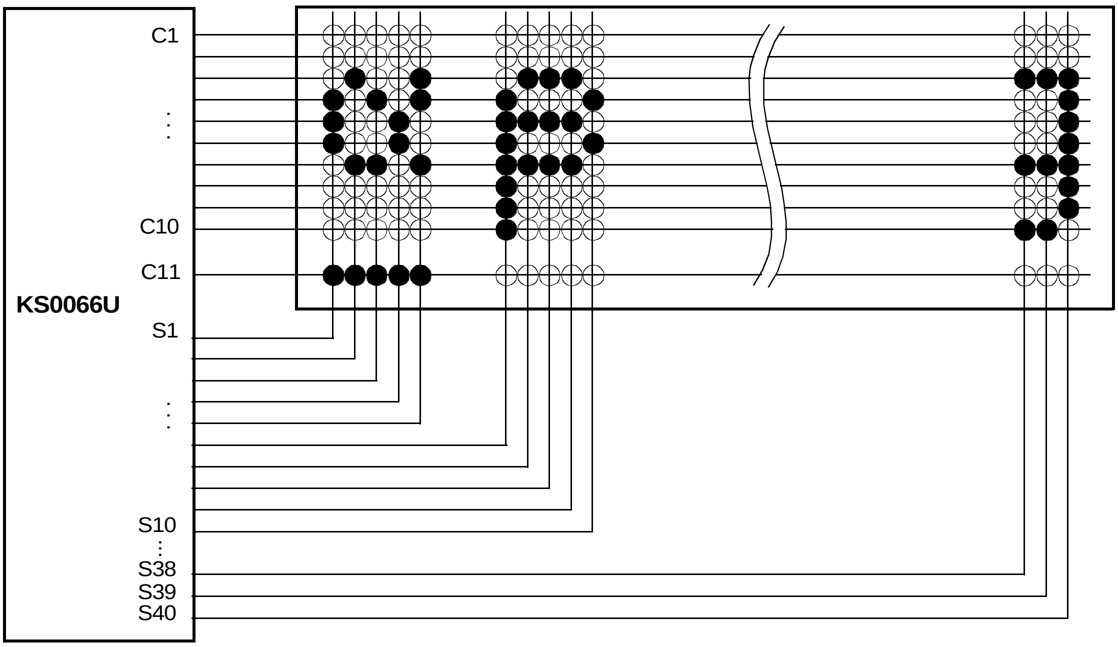
Figure 5 . Example of 4-bit Bus Mode Timing Diagram

APPLICATION INFORMATION ACCORDING TO LCD PANEL

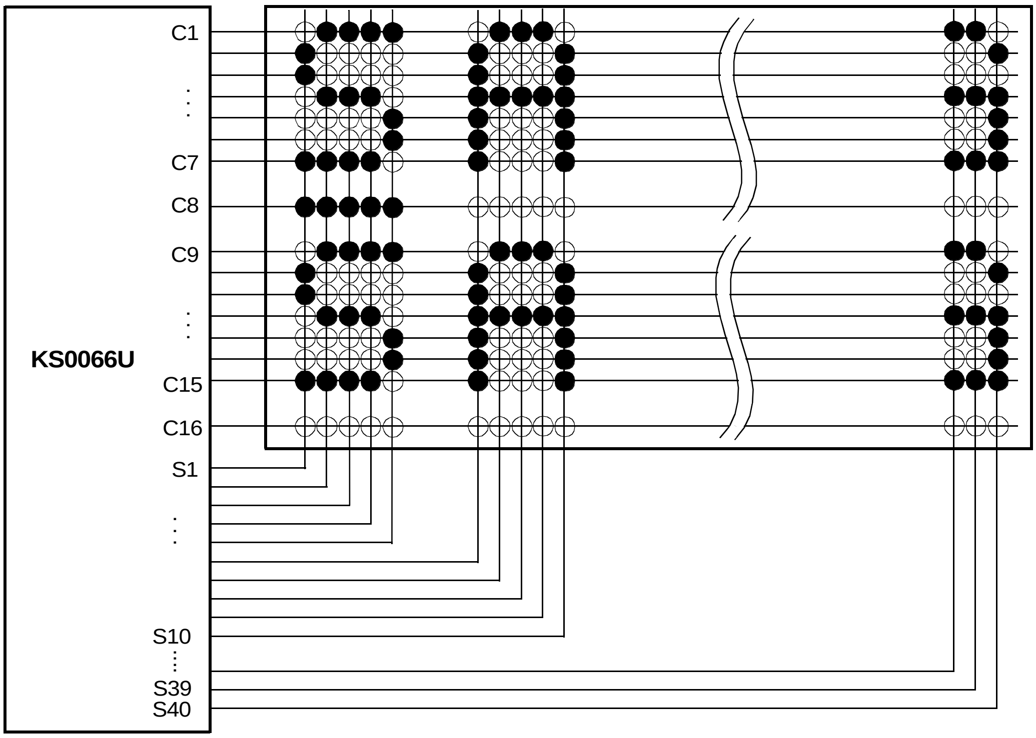
1) LCD Panel: 8 characters ×1-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)



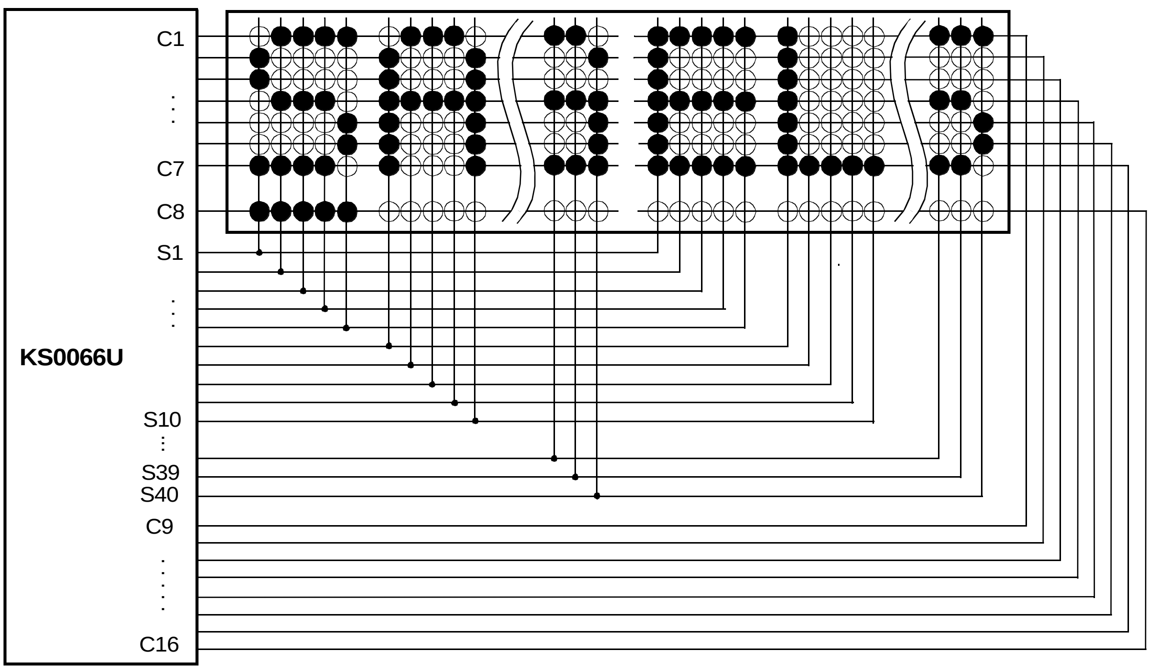
2) LCD Panel: 8 characters ×1-line format (5×10 dots + 1cursor line, 1/4 bias, 1/11 duty)



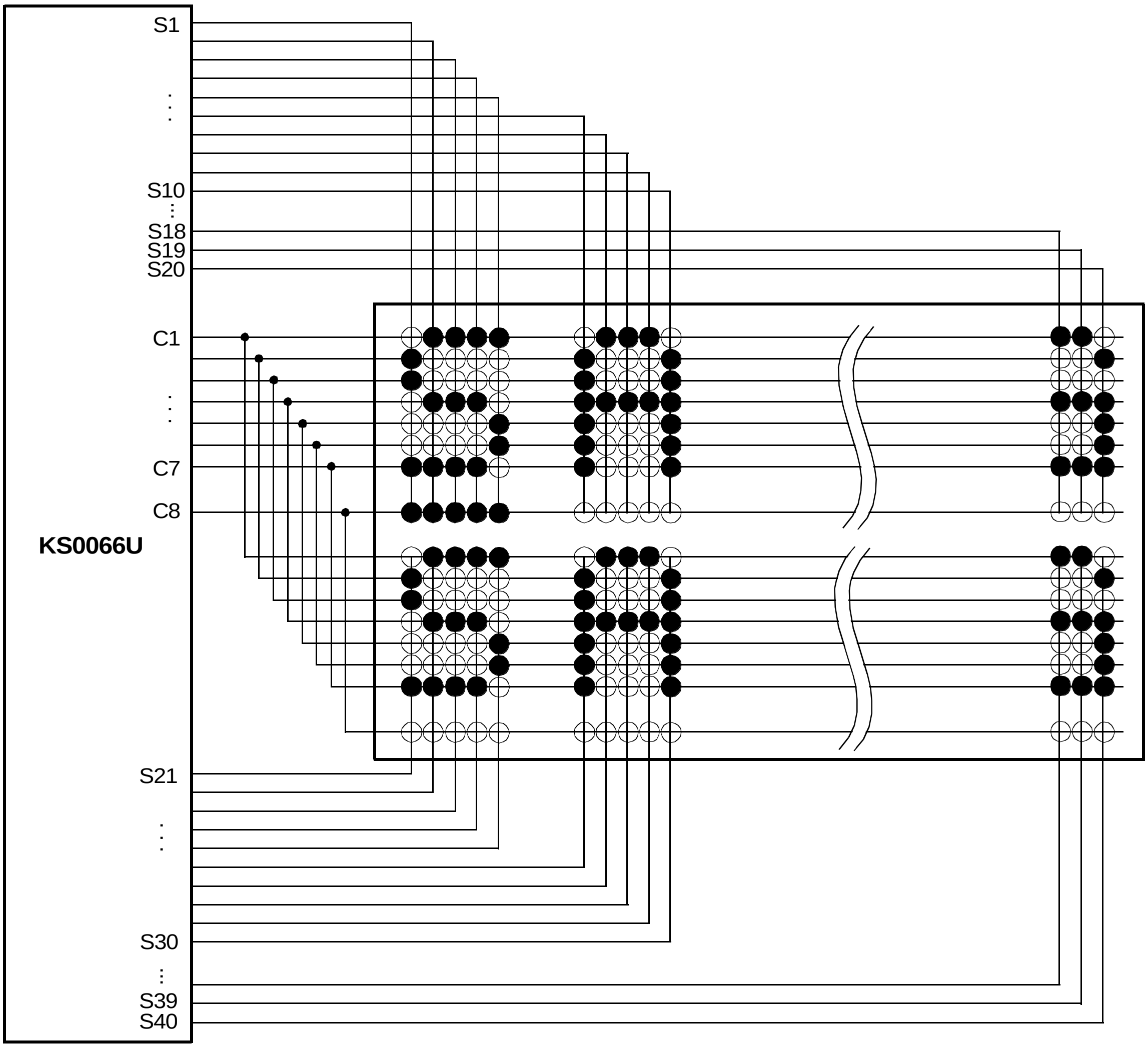
3) LCD Panel: 8 characters ×2 -line format (5×7 dots + line, 1/5 bias, 1/16 duty)



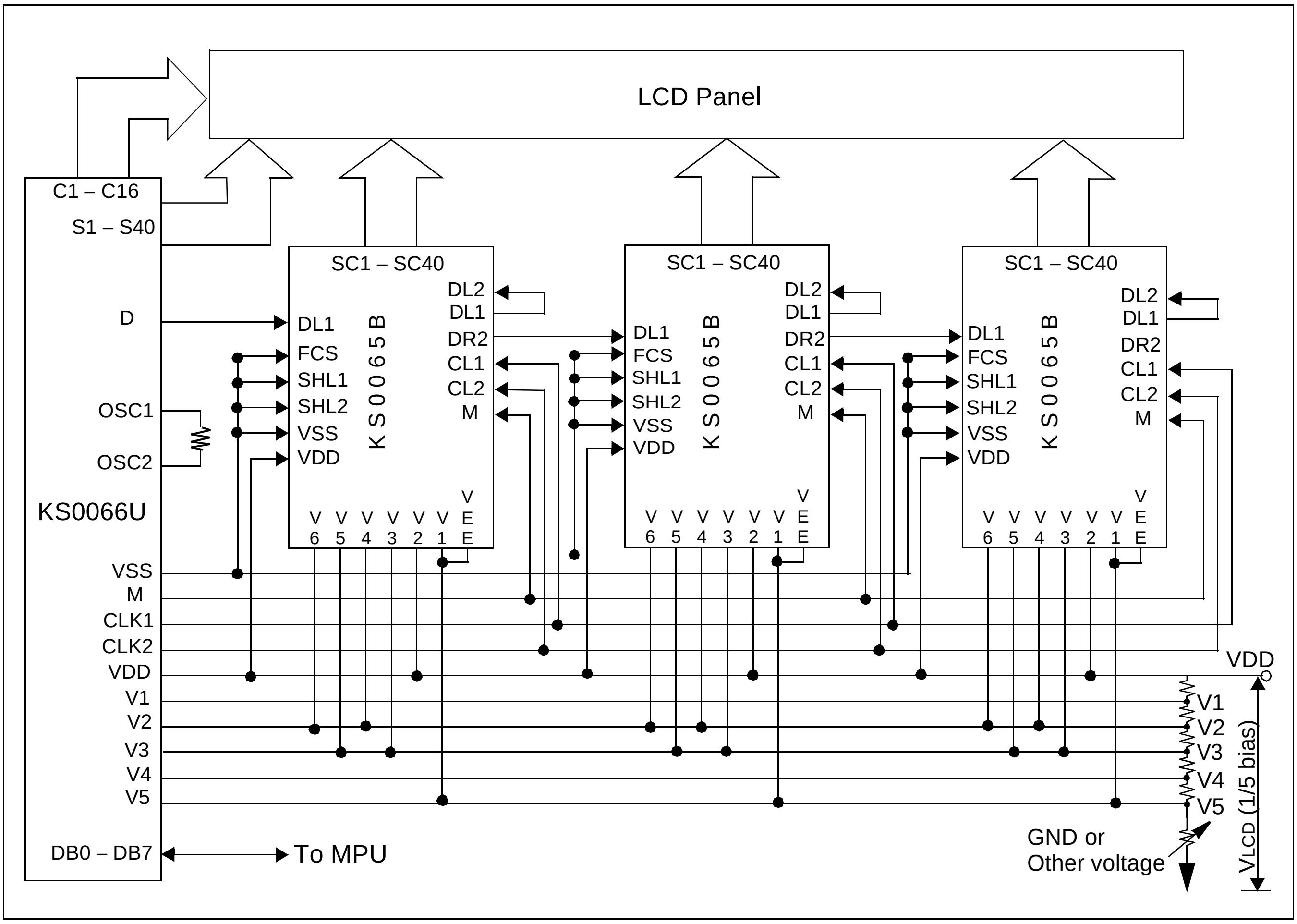
4) LCD Panel: 16 characters ×1-line format (5×7 dots + 1cursor line, 1/5 bias, 1/16 duty)



5) LCD Panel: 4 characters ×2-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)



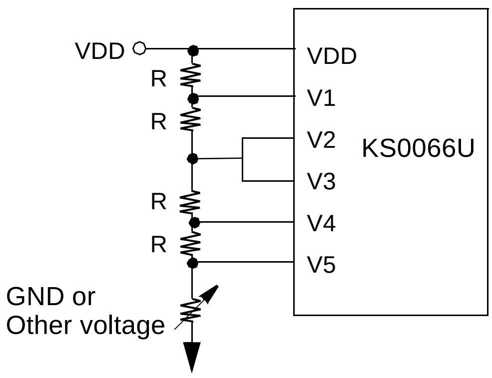
6) APPLICATION CIRCUIT



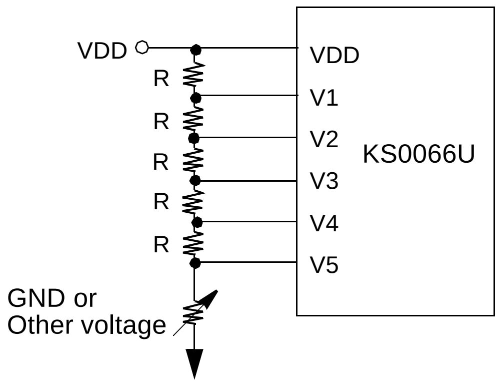
NOTE: When KS0065B is externally connected to the KS0066U, you can increase the number of display digits up to 80 characters.

BIAS VOLTAGE DIVIDE CIRCUIT

1) 1/4 bias, 1/8 or 1/11 duty



2) 1/5 bias, 1/16 duty



INITIALIZING

When the power is turned on, KS0066U is initialized automatically by power on reset circuit.
During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) to the end of initialization.

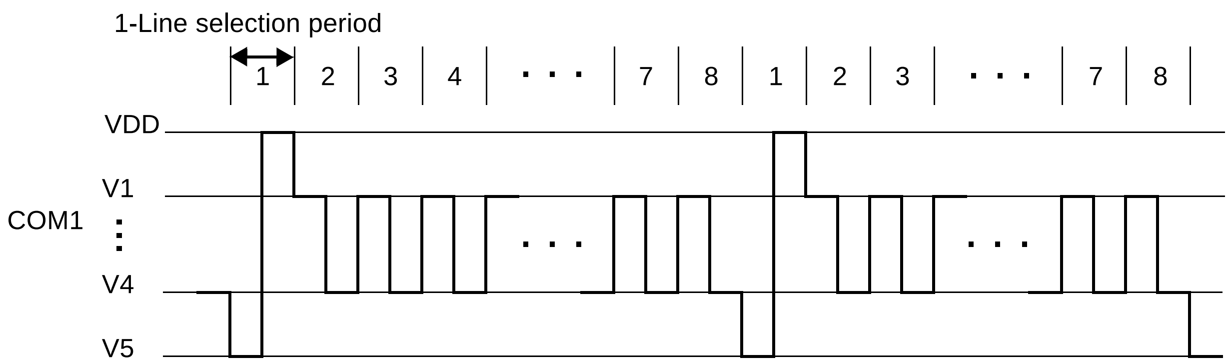
(1) Display Clear instruction: Write "20H" to all DDRAM
(2) Set Functions instruction: DL = "High": 8-bit bus mode
N = "Low": 1-line display mode
F = "Low": 5 X 8 font type
(3) Control Display ON/OFF instruction: D = "Low": Display OFF
C = "Low": Cursor OFF
B = "Low": Blink OFF
(4) Set Entry Mode instruction: I/D = "High": Increment by 1
SH = "Low": No entire display shift

FRAME FREQUENCY

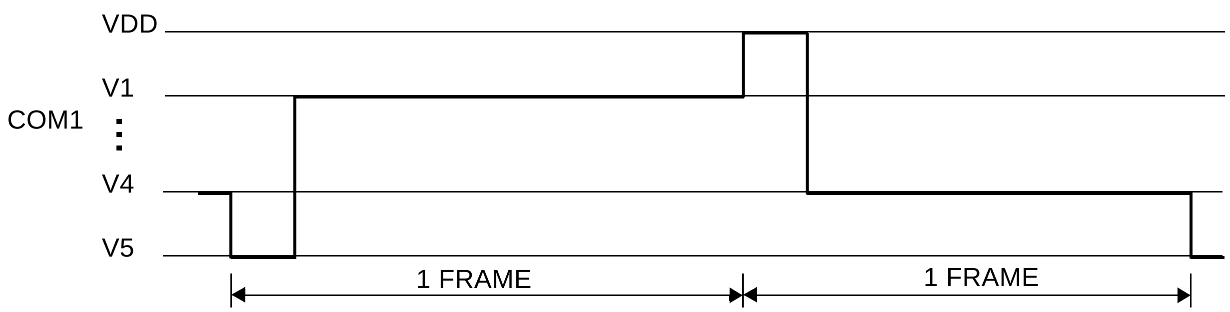
Programmable Driving Method by the same font mask option: Display waveform A-Type, B-Type

1) 1/8 duty cycle

A) A-type Waveform



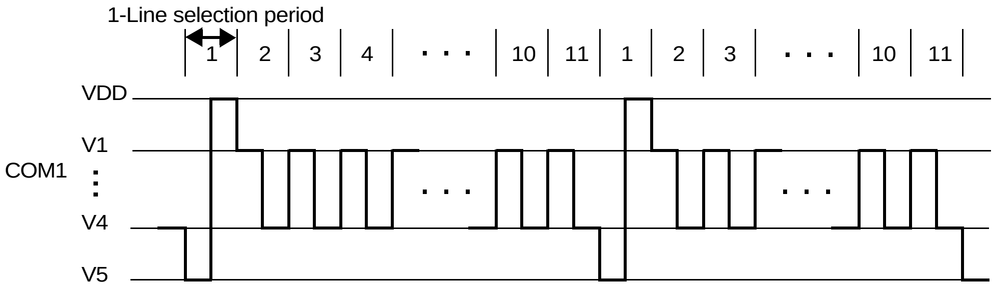
B) B-type Waveform



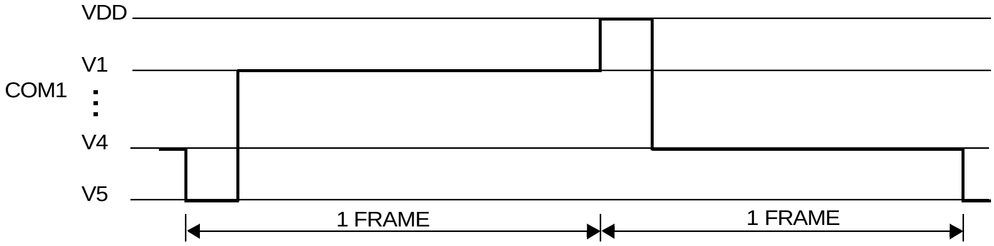
1-Line selection period = 400 clocks
1 Frame = $400 \times 8 \times 3.7$ µs = 11850 µs = 11.9 ms (1 clock=3.7 µs, fosc=270 kHz)
Frame frequency = 1 / 11.9 ms = 84.4 Hz

2) 1/11 duty cycle

A) A-type Waveform



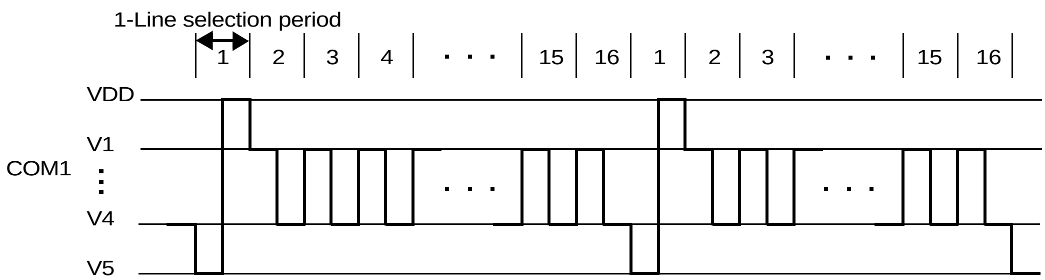
B) B-type Waveform



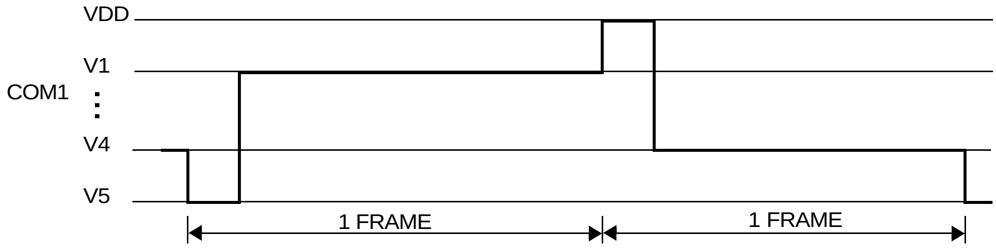
1-Line selection period = 400 clocks
1 Frame = 400×11×3.7 μs = 16300 μs = 16.3 ms (1 clock=3.7 μs, fosc=270 kHz)
Frame frequency = 1 / 16.3 ms = 61.4 Hz

3) 1/16 duty cycle

A) A-type Waveform



B) B-type Waveform



1-Line selection period = 200 clocks
1 Frame = 200×16×3.7 μs = 11850 μs = 11.9 ms (1 clock=3.7 μs, fosc=270 kHz)
Frame frequency = 1 / 11.9 ms = 84.3 Hz

INITIALIZING BY INSTRUCTION

1) 8-bit interface mode (Condition: fosc = 270KHZ)

Power on

↓

Wait for more than 30 ms after V_{DD} rises to 4.5 v

↓

Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	X	X

N	0	1-line mode
	1	2-line mode

F	0	display off
	1	display on

↓

Wait for more than 39 μs

↓

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D	0	display off
	1	display on

C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

↓

Wait for more than 39 μs

↓

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

↓

Wait for more than 1.53 ms

↓

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift on

↓

Initialization end

2) 4-bit interface mode (Condition: fosc = 270KHZ)

Power on

↓

Wait for more than 30 ms after Vdd rises to 4.5 v

↓

Function set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

N	0	1-line mode
	1	2-line mode

F	0	display off
	1	display on

↓

Wait for more than 39 µs

↓

Display ON/OFF Control									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

D	0	display off
	1	display on

C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

↓

Wait for more than 39 µs

↓

Display Clear									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

↓

Wait for more than 1.53 ms

↓

Entry Mode Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	SH	X	X	X	X

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift on

↓

Initialization end

MAXIMUM ABSOLUTE LIMIT

Table 8. Maximum Absolute Power Ratings

Characteristic	Symbol	Unit	Value
Power Supply Voltage(1)	V_{DD}	V	-0.3 ~ +7.0
Power Supply Voltage(2)	V_{LCD}	V	V_{DD}-15.0 ~ V_{DD}+0.3
Input Voltage	V_{IN}	V	-0.3 ~ V_{DD}+0.3

NOTE: Voltage greater than above may damage the circuit.

$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

Table 9. Temperature characteristics

Characteristic	Symbol	Unit	Value
Operating Temperature	T_{OPR}	°C	-30 ~ +85
Storage Temperature	T_{STG}	°C	-55 ~ +125

ELECTRICAL CHARACTERISTICS

DC Characteristics

Table 10. DC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85^{o}C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-	4.5	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=5.0 V, fosc = 270 kHz)	-	0.35	0.6	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	2.2	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (2) (OSC1)	V_{IH2}	-	V_{DD}-1.0	-	V_{DD}	V
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.205 mA	2.4	-	-	V
	V_{OL1}	I_{OL} = 1.2 mA	-	-	0.4	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O = -40 μA	0.9V_{DD}	-	-	V
	V_{OL2}	I_O = 40 μA	-	-	0.1V_{DD}	
Voltage Drop	Vd_{COM}	I_O = ± 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IKG}	V_{IN} = 0 V to V_{DD}	-1	-	1	μA
Input Low Current	I_{IL}	V_{IN} = 0 V, V_{DD} = 5 V (PULL UP)	-50	-125	-250	
Internal Clock (external Rf)	f_{OSC1}	Rf = 91 kΩ ± 2% (V_{DD} = 5 V)	190	270	350	kHz
External Clock	f_{OSC}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R, t_F		-	-	0.2	μs
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 Bias)	3.0	-	13.0	V

Table 11. DC Characteristic (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85^{o}C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-	2.7	-	4.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=3.0 V, fosc = 270 kHz)	-	0.15	0.3	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	$0.7V_{DD}$	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.55	
Input Voltage (2) (OSC1)	V_{IH2}	-	$0.7V_{DD}$	-	V_{DD}	V
	V_{IL2}	-	-	-	$0.2V_{DD}$	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.1 mA	$0.75V_{DD}$	-	-	V
	V_{OL1}	I_{OL} = 0.1 mA	-	-	$0.2V_{DD}$	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O = -40 μA	$0.8V_{DD}$	-	-	V
	V_{OL2}	I_O = 40 μA	-	-	$0.2V_{DD}$	
Voltage Drop	Vd_{COM}	$I_O = \pm$ 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IKG}	V_{IN} = 0 V to V_{DD}	-1	-	1	μA
Input Low Current	I_{IL}	V_{IN} = 0 V, V_{DD} = 3 V (PULL UP)	-10	-50	-120	
Internal Clock (external Rf)	f_{OSC1}	Rf = 75 kΩ $\pm$ 2% (V_{DD} = 3 V)	190	270	350	kHz
External Clock	f_{OSC2}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R,t_F		-	-	0.2	μs
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 Bias)	3.0	-	13.0	V

NOTE: LCD Driving Voltage

Power	Duty	1/8, 1/11 Duty	1/16 Duty
	Bias	1/4 Bias	1/5 Bias
V_{DD}		V_{DD}	V_{DD}
V_1		V_{DD}-V_{LCD}/4	V_{DD}-V_{LCD}/5
V_2		V_{DD}-V_{LCD}/2	V_{DD}-2V_{LCD}/5
V_3		V_{DD}-V_{LCD}/2	V_{DD}-3V_{LCD}/5
V_4		V_{DD}-3V_{LCD}/4	V_{DD}-4V_{LCD}/5
V_5		V_{DD}-V_{LCD}	V_{DD}-V_{LCD}

AC Characteristics

Table 12. AC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85^{o}C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Table 13. AC Characteristics (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85^{o}C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_Rt_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

Table 14. AC Characteristics (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85^{o}C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Interface Mode with Extension Driver (Refer to Fig-8)	Clock Pulse Width (High, Low)	tc	800	-	-	ns
	Clock Rise / Fall Time	t_R,t_F	-	-	25	
	Clock Setup Time	tsu1	500	-	-	
	Data Setup Time	tsu2	300	-	-	
	Data Hold Time	t_{DH}	300	-	-	
	M Delay Time	t_{DM}	-1000	-	1000	

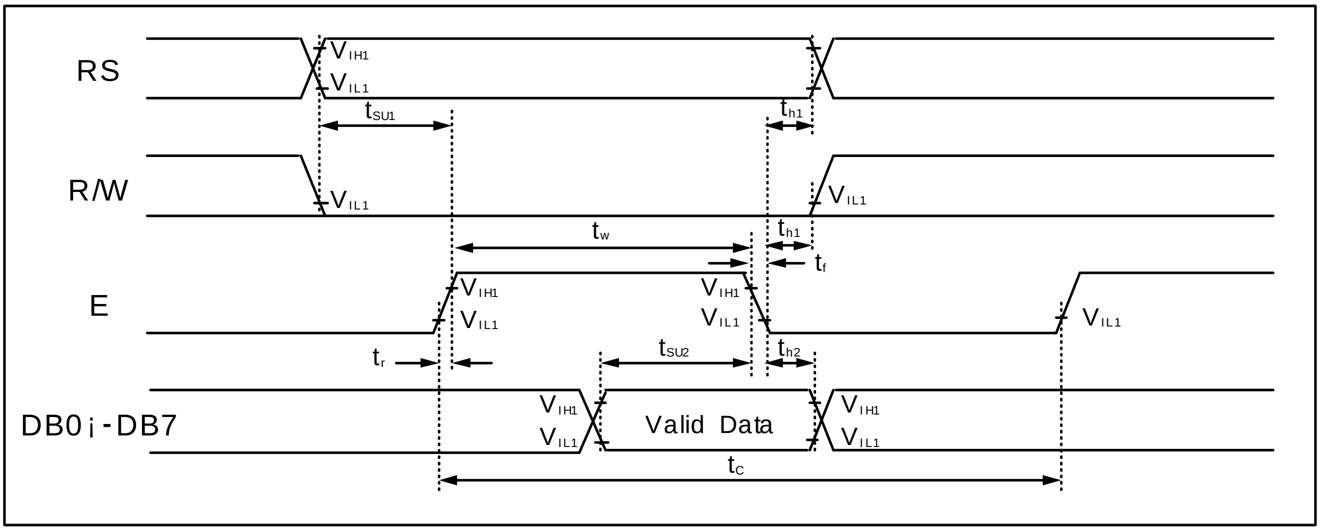


Figure 6 . Write Mode Timing Diagram

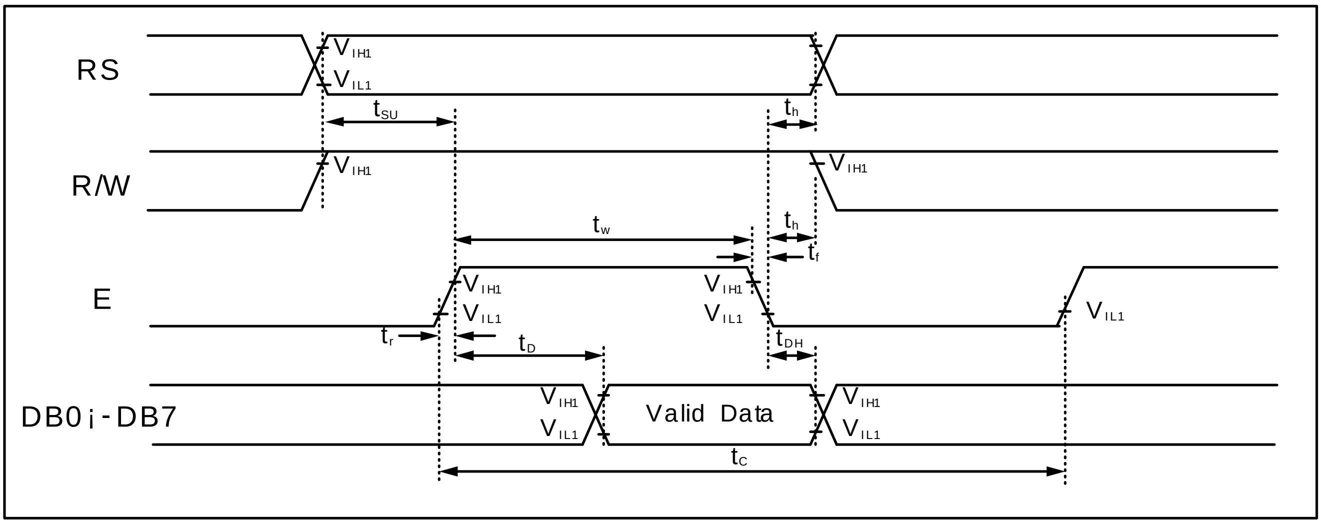


Figure 7 . Read Mode Timing Diagram

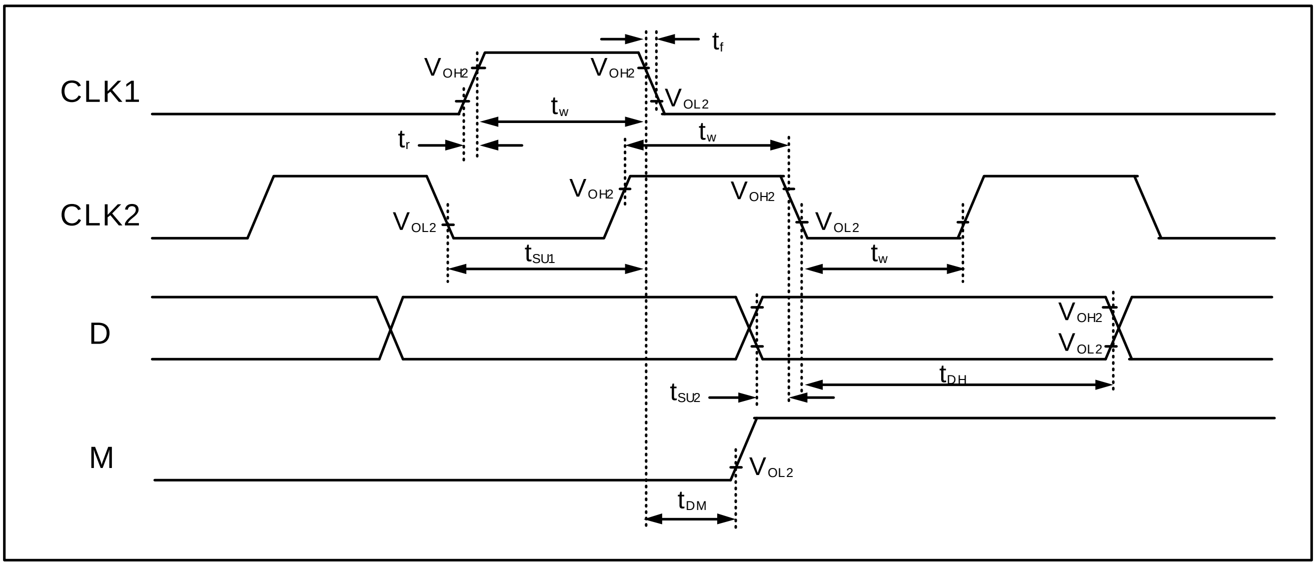
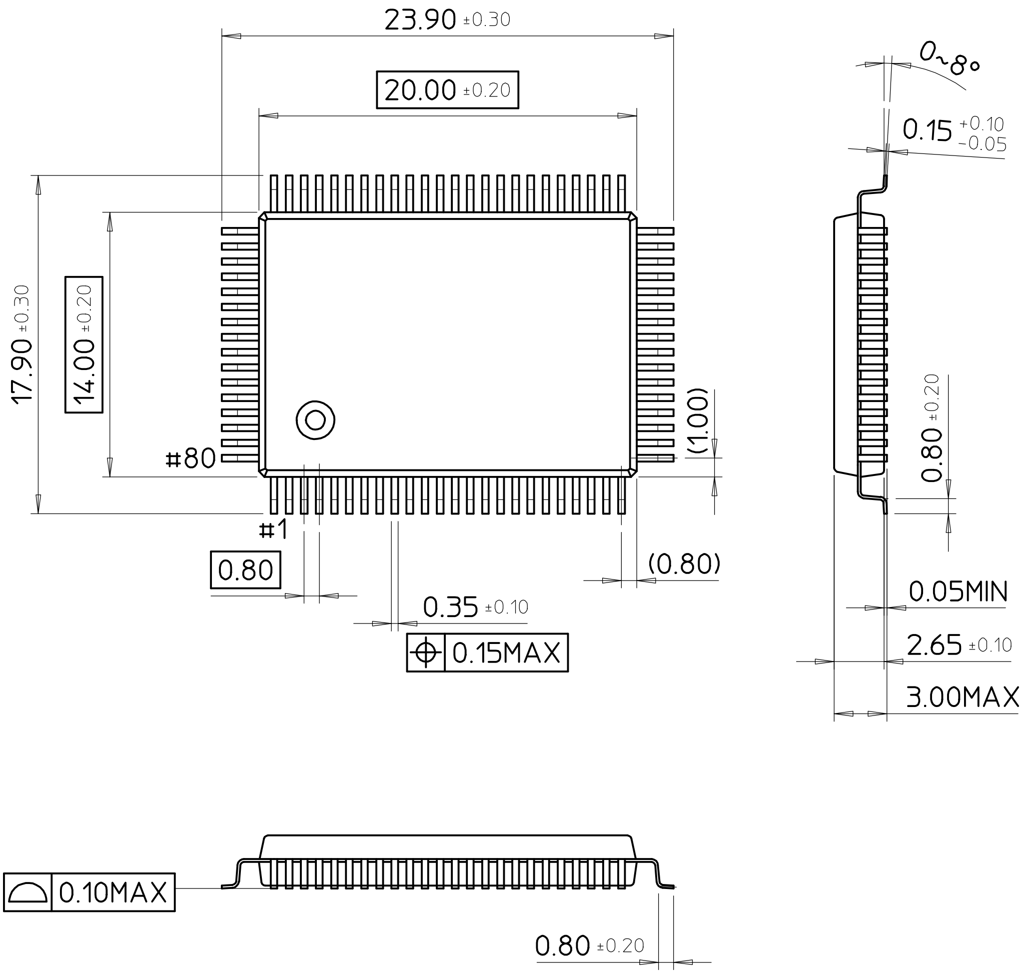


Figure 8 . Interface Mode With Extension Driver Timing Diagram

80-QFP-1420C

Dimensions in Milimeters



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