~\MobaXterm\home\QuartusProjects\Homework\hw8\hw8_square_wave\sqrWv_tb.vhd

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use work.all;
4
5  entity sqrWv_tb is
6  end sqrWv_tb;
7
8  architecture tb of sqrWv_tb is
9
10     constant period_c   : time := 10 ns;
11     signal clock_net    : std_logic;
12     signal RST_net : std_logic;
13     signal H_net : std_logic_vector(3 downto 0);
14     signal L_net : std_logic_vector(3 downto 0);
15     signal wave_out_net : std_logic;
16
17     component sqrWv
18         port (
19             clock : in std_logic;
20             RST : in std_logic;
21             H : in std_logic_vector(3 downto 0);
22             L : in std_logic_vector(3 downto 0);
23             wave_out : out std_logic
24         );
25     end component sqrWv;
26
27
28 begin
29
30     sqrWv_instance: sqrWv
31     port map(
32         clock => clock_net,
33         RST => RST_net,
34         H => H_net,
35         L => L_net,
36         wave_out => wave_out_net
37     );
38
39     tb_clk: process
40     begin
41         clock_net <= '1';
42         wait for period_c / 2;
43         clock_net <= '0';
44         wait for period_c / 2 ;
45     end process tb_clk;
46
47     tb_p: process
48     begin
49
50         H_net <= "0011";
51         L_net <= "0011";
52         RST_net <= '1';
```

```
53          wait for 4 * period_c;
54          RST_net <= '0';
55
56          wait for 1600 ns;
57
58          assert false
59          report "End of TestBench"
60          severity failure;
61
62      end process tb_p;
63
64  end tb;
```