2024 Digital IC Design
Homework 3: matrix multiplier

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Simulation Result

Functional simulation	100	Gate-level simulation	100	Clock width	21ns	Gate-level simulation time	130158 ns

```
Pattern 3 pass
---------------------------- Simulation FINISH !!---------------------------
score =         100/100
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
** Note: $stop    : D:/DIC/HW3/testfixture.v(351)
   Time: 130158 ns  Iteration: 0  Instance: /testfixture1
Break in Module testfixture1 at D:/DIC/HW3/testfixture.v line 351
```

```
// `define SDFFILE    "../SYN/SET_syn.sdf"    // Modify your sdf file name here
`define cycle 21.0
`define terminate_cycle 400000 // Modify your terminate cycle here
```

```
Pattern 3 pass
---------------------------- Simulation FINISH !!---------------------------
score =         100/100
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
** Note: $stop    : D:/DIC/HW3/testfixture.v(351)
   Time: 130158 ns  Iteration: 0  Instance: /testfixture1
Break in Module testfixture1 at D:/DIC/HW3/testfixture.v line 351
```

Synthesis Result

Total logic elements	1810
Total memory bit	0
Embedded multiplier 9-bit element	1

Flow Status	Successful - Mon May 13 14:00:52 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	HW3
Top-level Entity Name	MM
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	1,810 / 55,856 (3 %)
Total registers	1059
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

在這次 LAB 要實作一個矩陣成法器電路，一開始我宣告兩個 2 維 4*4 矩陣，在接收資料的狀態中用於依序存取資料，接著利用矩陣 1 的 j 與矩陣 2 的 i 是否相等判斷兩個矩陣是否可以相乘，若可以相乘則進入下一個狀態，依序將兩個 reg 裡面的資料進行相乘，最後輸出，我總共利用 1810 個邏輯閘與 1 個乘法器，雖然時間較長但因為只使用一個乘法器，因此可以減少面積。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*