2024 Digital IC Design

Homework 3: matrix multiplier

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NAME | | 黃奕淳 | | | | | | |
| Student ID | | N26112291 | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | 100 | | Gate-level simulation | 100 | Clock  width | 21ns | Gate-level simulation time | 130158 ns |
|  | | | | |  | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 1810 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 1 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 在這次LAB要實作一個矩陣成法器電路，一開始我宣告兩個2維4\*4矩陣，在接收資料的狀態中用於依序存取資料，接著利用矩陣1的j與矩陣2的i是否相等判斷兩個矩陣是否可以相乘，若可以相乘則進入下一個狀態，依序將兩個reg裡面的資料進行相乘，最後輸出，我總共利用1810個邏輯閘與1個乘法器，雖然時間較長但因為只使用一個乘法器，因此可以減少面積。 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*