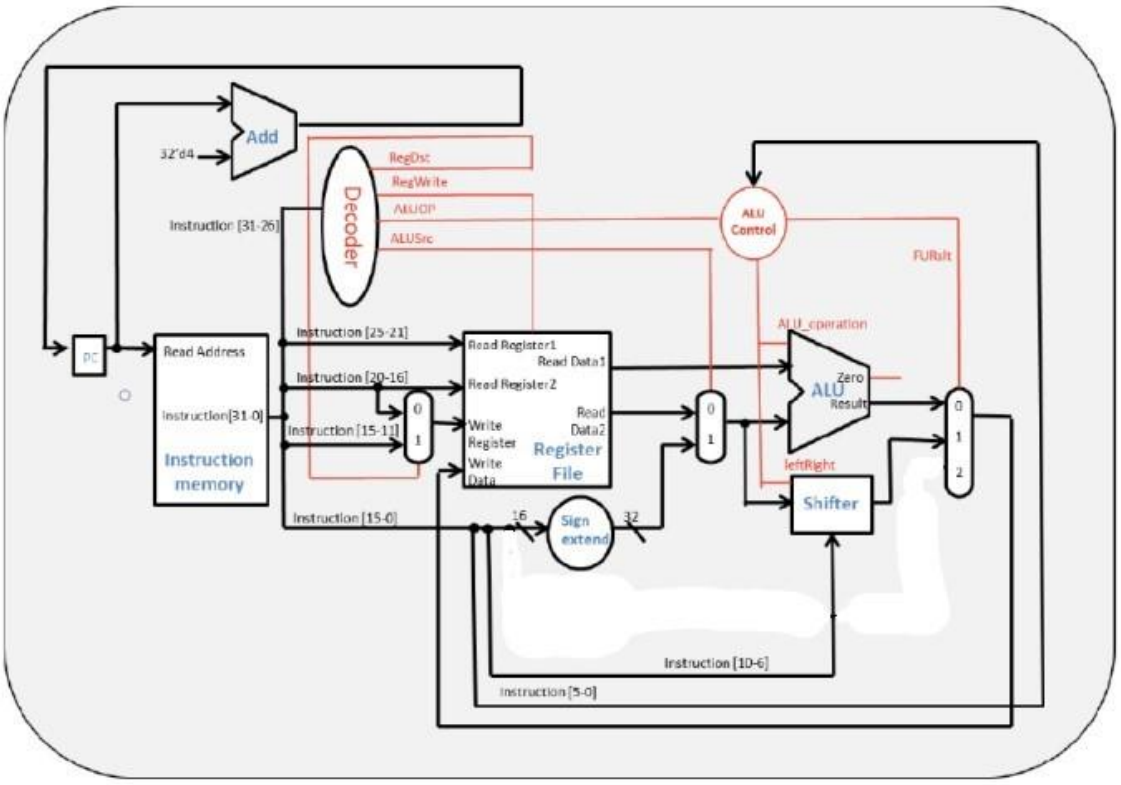
Computer Organizaion

1. Architecture Diagrams :



I didn't use modulo Zero_Filled, and didn't connect its wire.

2.Hardware modulo analysis :

Adder：add two 32bits input source and output a 32bits sum, used for doing PC = PC + 4

ALU_1bit：a one bit alu from hw2, inside I separate the largest bit from other bit, create 2 modulo, used for making a 32bits ALU

ALU_Ctrl：read ALUop from Decoder and funct code from instruction to decide the ALU function and the value needed to write back to reg

ALU：a 32bits ALU from hw2, the main calculation of cpu

Decoder：decode the instruction and output control signals

Mux2to1：a 2 to 1 multiplexer, choose the write register and the second source of ALU, control by control signals

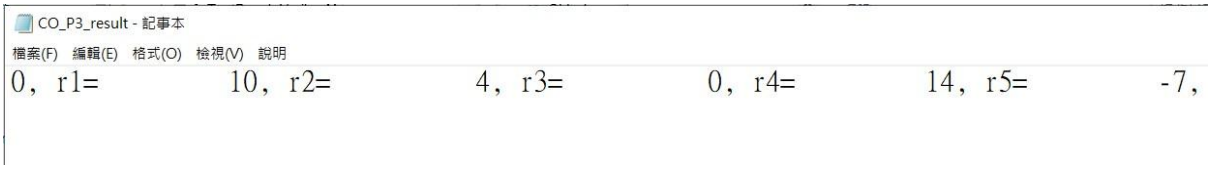
Mux3to1：a 3 to 1 multiplexer, choose the result that is going to write back, control by FURslt, control signal from ALU_Ctrl

Shifter：shift the input by a given number and output the result, used for sll / slr instr.

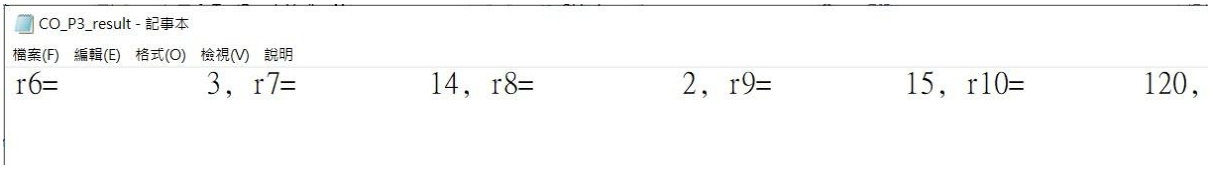
Sign_Extend：extend the input, used for extending the constant of immediate instr.

3. Finished Part：

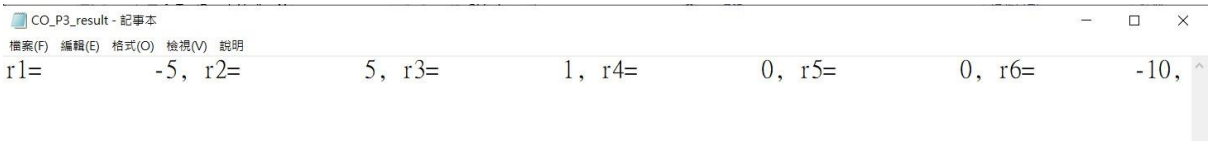
test data 1：



test data 2：



test data 3：



4. Problems you met and solutions：

(1) put the txt. into the project

solution：I try to put them in design source and simulation source, and find out that I should put them in simulation source.

(2) using ?: as a wrong way

I use nested structure, and it shows errors. Then I think for a long time and find out that I miss the value when none of the conditions fit.

(3) connect wrong wire

I draw a diagram on the paper and check through every block’s input and output, then can easily find out the wrong wire.

5. Summary

(1) I learned how to implement a simple cycle cpu and connect wires. Also use assign in a proper way.

(2) more debugging ways, like debug block by block, and I display the wire data to check if the answer is correct or not.