Computer Organizaion

1. Finished Part:

CO_P4_result - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

```
Register==========================================================
r0=          0, r1=          1, r2=          2, r3=          2,

r4=          4, r5=         -2, r6=          2, r7=         -2,

r8=          4, r9=          0, r10=         1, r11=         3,

r12=         0, r13=         3, r14=         0, r15=         1,

r16=         0, r17=         0, r18=         0, r19=         0,

r20=         0, r21=         0, r22=         0, r23=         0,

r24=         0, r25=         0, r26=         0, r27=         0,

r28=         0, r29=       128, r30=         0, r31=         0,

Memory============================================================
m0=          2, m1=         -2, m2=          1, m3=          0,

m4=          1, m5=          4, m6=          0, m7=          4,

m8=          0, m9=          4, m10=         0, m11=         0,

m12=         0, m13=         0, m14=         0, m15=         0,

m16=         0, m17=         0, m18=         0, m19=         0,

m20=         0, m21=         0, m22=         0, m23=         0,

m24=         0, m25=         0, m26=         0, m27=         0,

m28=         0, m29=         0, m30=         0, m31=         0,
```

2. Problems you met and solutions:
I met the problem that the testbench cannot include .v files, and I ask for help and know that I should put all source files at the same place with the testbench. Then I solve it.

3. If you create additional module, please give a short explanation here :
I created an ALU_1bit.v, inside are two modules.

(1) ALU_1bit module, it is going to do 1-bit ALU calculation.

(2) ALU_for_31 module, it is going to do 1-bit ALU calculation for the maximum bit, so that I can output overflow and set.

Then is a Full_adder.v file. It is a module that does 32-bits addition.