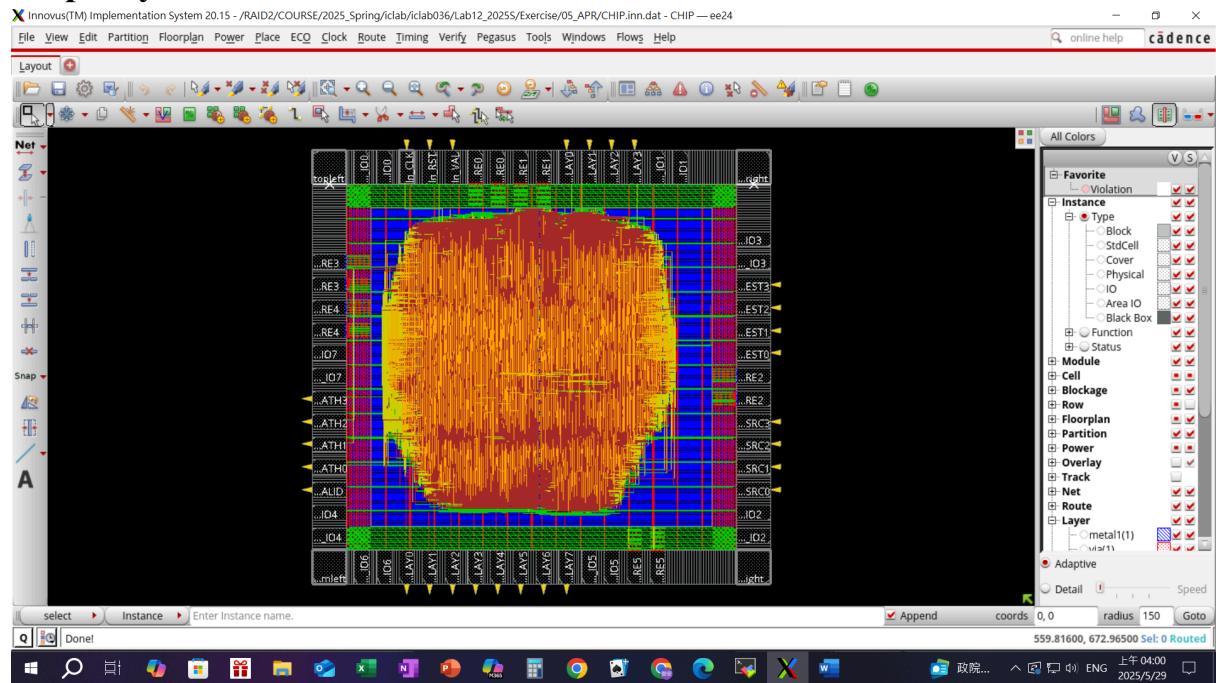
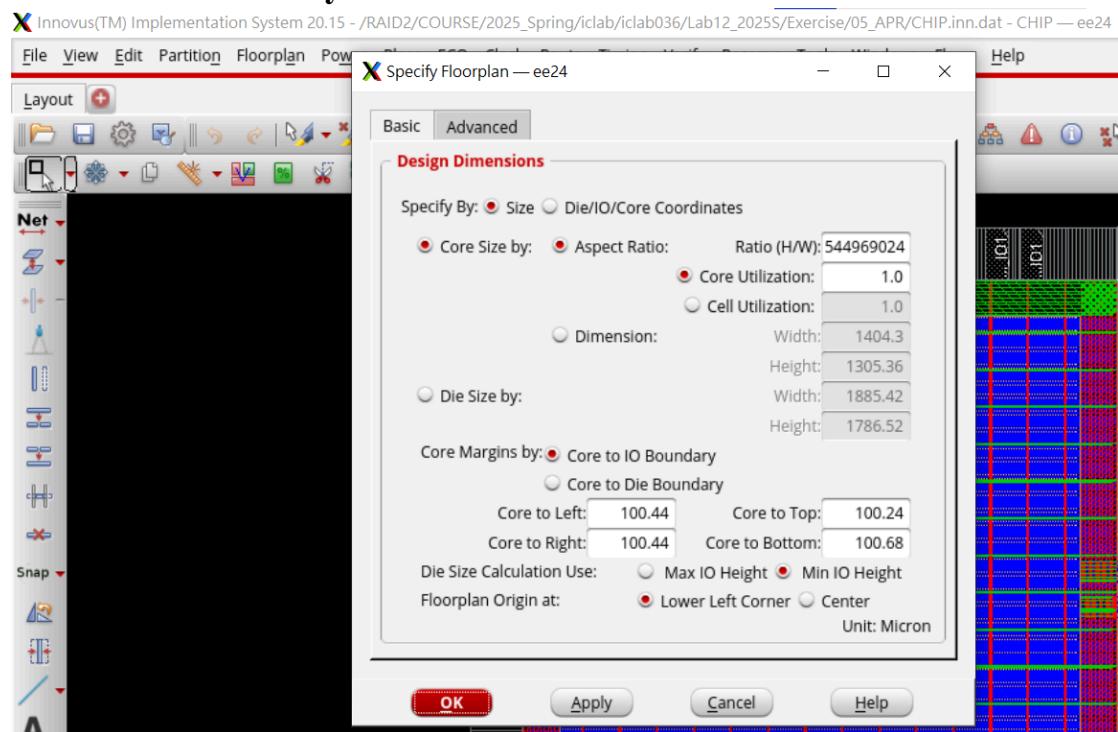


Report

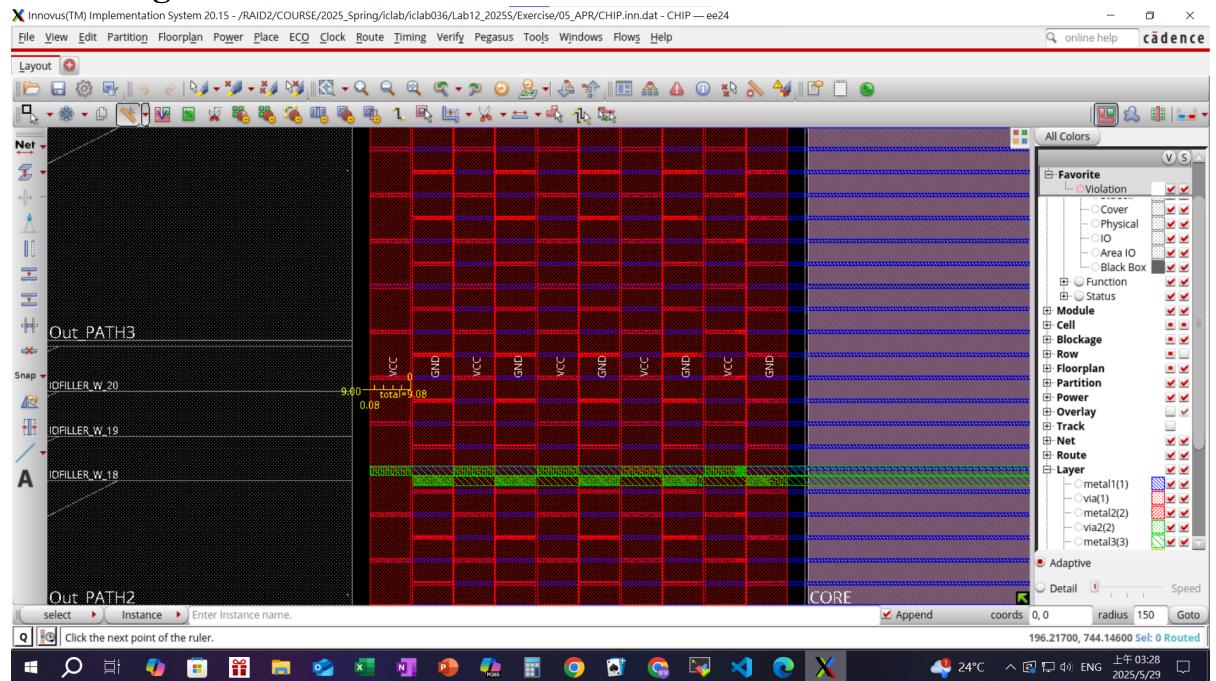
1. Chip Layout View :



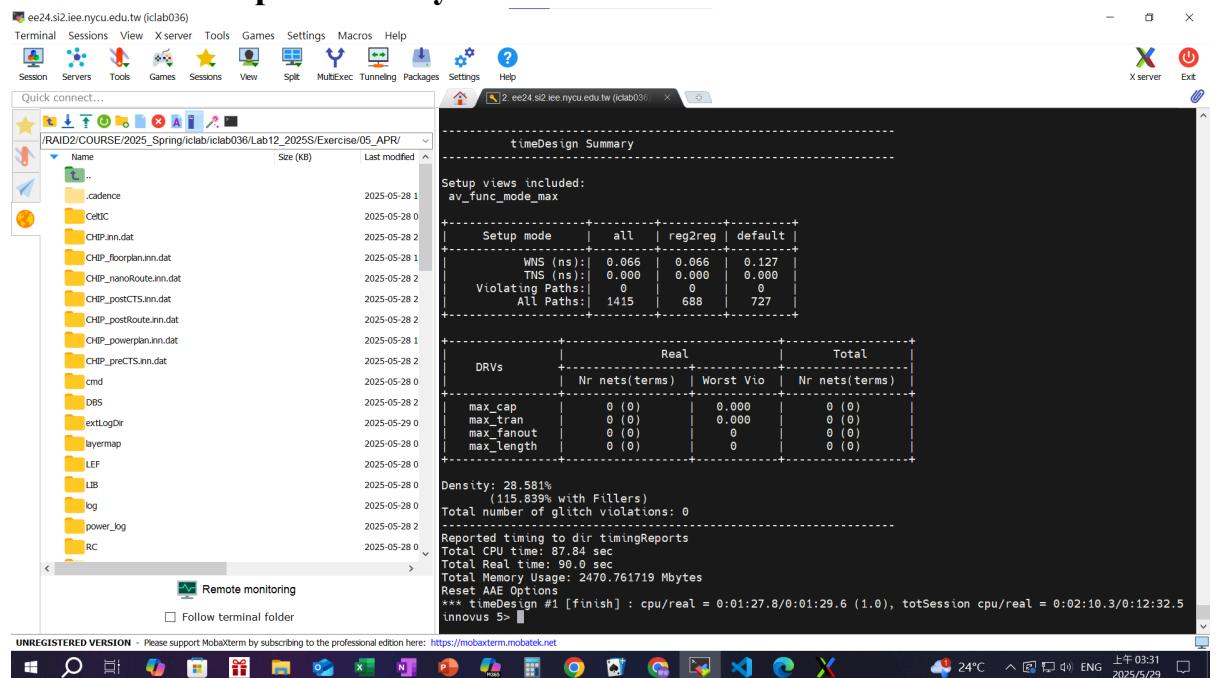
2. Core to IO boundary :



3. Core Ring :



4. Post-Route setup time analysis :



5. Post-Route hold time analysis :

```

ee24.siz.iee.nycu.edu.tw (clab036)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
[RAID2/COURSE/2025_Spring/clab/clab036/Lab12_2025S/Exercise/05_APR/]
Name Size (KB) Last modified
.. 2025-05-28 1
.cadence 2025-05-28 0
.Chip.inn.dat 2025-05-28 2
.Chip_floorplan.inn.dat 2025-05-28 1
.Chip_nanoRoute.inn.dat 2025-05-28 2
.Chip_postCTS.inn.dat 2025-05-28 2
.Chip_postRoute.inn.dat 2025-05-28 1
.Chip_powerplan.inn.dat 2025-05-28 2
.Chip_preCTS.inn.dat 2025-05-28 2
.cmd 2025-05-28 0
.DBS 2025-05-28 2
extLogDir 2025-05-29 0
layermap 2025-05-28 0
.LEF 2025-05-28 0
.LIB 2025-05-28 0
.log 2025-05-28 0
power_log 2025-05-28 2
.RC 2025-05-28 0

Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 2491.9M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2460)
Glitch Analysis: View av_func_mode_mtn -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_mtn -- Total Number of Nets Analyzed = 26562.
Total Number of Fetched objects: 26562.
AAE_INFO-618: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets for which stage creation was skipped for all views 0
End delay calculation (fullDC). (MEM=2500.18 CPU=0:00:01.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2500.18 CPU=0:00:01.2 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:09.6 real=0:00:09.0 totSessionCpu=0:02:24 mem=2500.2M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_mtn

+---+ Hold mode +---+ all +---+ reg2reg +---+ default +---+
| | +-----+ | +-----+ | +-----+ | +-----+ |
| WNS (ns): | 0.276 | 0.276 | 5.065 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 1415 | 688 | 727 |

+---+ +---+ +---+ +---+
Density: 28.581% (115.839% with Fillers)
-----
Reported timing to dir timingReports
Total CPU time: 11.44 sec
Total Real time: 11.0 sec
Total Memory Usage: 2426.441406 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:11.4/0:00:11.8 (1.0), totSession cpu/real = 0:02:24.6/0:13:45.2 (0.2), mem = 2426.4M
innovus 5>

```

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6. DRC result :

```

ee24.siz.iee.nycu.edu.tw (clab036)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
[RAID2/COURSE/2025_Spring/clab/clab036/Lab12_2025S/Exercise/05_APR/]
Name Size (KB) Last modified
.. 2025-05-28 1
.cadence 2025-05-28 0
.Chip.inn.dat 2025-05-28 2
.Chip_floorplan.inn.dat 2025-05-28 1
.Chip_nanoRoute.inn.dat 2025-05-28 2
.Chip_postCTS.inn.dat 2025-05-28 2
.Chip_postRoute.inn.dat 2025-05-28 0
.Chip_powerplan.inn.dat 2025-05-28 1
.Chip_preCTS.inn.dat 2025-05-28 2
.cmd 2025-05-28 0
.DBS 2025-05-28 0
extLogDir 2025-05-29 0
layermap 2025-05-28 0
.LEF 2025-05-28 0
.LIB 2025-05-28 0
.log 2025-05-28 0
power_log 2025-05-28 2
.RC 2025-05-28 0

VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1363.200 1029.120 1635.840 1286.400} 34 of 49
VERIFY DRC ..... Sub-Area: {34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1635.840 1029.120 1885.420 1286.400} 35 of 49
VERIFY DRC ..... Sub-Area: {35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1000.560 1286.400 272.640 1543.680} 36 of 49
VERIFY DRC ..... Sub-Area: {36 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {272.640 1286.400 545.280 1543.680} 37 of 49
VERIFY DRC ..... Sub-Area: {37 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {545.280 1286.400 817.920 1543.680} 38 of 49
VERIFY DRC ..... Sub-Area: {817.920 1286.400 1090.560 1543.680} 39 of 49
VERIFY DRC ..... Sub-Area: {1090.560 1286.400 1263.200 1543.680} 40 of 49
VERIFY DRC ..... Sub-Area: {40 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1363.200 1286.400 1635.840 1543.680} 41 of 49
VERIFY DRC ..... Sub-Area: {41 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {545.280 1543.680 817.920 1786.520} 42 of 49
VERIFY DRC ..... Sub-Area: {42 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1543.680 272.640 1786.520} 43 of 49
VERIFY DRC ..... Sub-Area: {43 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {272.640 1543.680 545.280 1786.520} 44 of 49
VERIFY DRC ..... Sub-Area: {44 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {545.280 1543.680 817.920 1786.520} 45 of 49
VERIFY DRC ..... Sub-Area: {817.920 1543.680 1090.560 1786.520} 46 of 49
VERIFY DRC ..... Sub-Area: {1090.560 1543.680 1363.200 1786.520} 47 of 49
VERIFY DRC ..... Sub-Area: {1363.200 1543.680 1635.840 1786.520} 48 of 49
VERIFY DRC ..... Sub-Area: {1635.840 1543.680 1885.420 1786.520} 49 of 49
VERIFY DRC ..... Sub-Area : 49 complete 0 Viols.

Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:03.9 ELAPSED TIME: 4.00 MEM: 43.0M) ***
innovus 5>

```

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7. LVS result :

The screenshot shows a terminal window titled "2. ee24.si2.lee.nycu.edu.tw (iclab036)" running on a Windows operating system. The terminal interface includes a top menu bar with options like Terminal, Sessions, View, Xserver, Tools, Games, Settings, Macros, Help, and a gear icon for Settings. Below the menu is a toolbar with icons for Session, Servers, Tools, Games, Sessions, View, Split, MultiExec, Tunneling, and Packages. The main area of the terminal displays the output of a "VERIFY DRC" command. The output indicates that the verification was successful with 0 violations (Viols) and 0 wrongs (Wrngs). It also shows the elapsed time as 4.00 seconds and memory usage as 43.0M. The terminal window has a standard Windows title bar with minimize, maximize, and close buttons.

8. Post Layout simulation result :

ee24.si2.iee.nycu.edu.tw (iclab036)

Terminal Sessions View Xserver Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

X server Exit

Quick connect...

/RAID2/COURSE/2025_Spring/iclab/iclab036/Lab12_2025S/Exercise/06_POST/

Name	Size (KB)	Last modified
..		
cadence		2025-05-28 1
CetiIC		2025-05-28 0
CHIP.inn.dat		2025-05-28 2
CHIP_floorplan.inn.dat		2025-05-28 1
CHIP_handRoute.inn.dat		2025-05-28 2
CHIP_postCTS.inn.dat		2025-05-28 2
CHIP_postRoute.inn.dat		2025-05-28 2
CHIP_powerPlan.inn.dat		2025-05-28 1
CHIP_preCTS.inn.dat		2025-05-28 2
cmd		2025-05-28 0
DBS		2025-05-28 2
extLogDir		2025-05-29 0
layermap		2025-05-28 0
LEF		2025-05-28 0
LIB		2025-05-28 0
log		2025-05-28 0
power_bdg		2025-05-28 2
RC		2025-05-28 0

***** Congratulations! *****
execution cycles = 50000
clock period = 11.00000ns
*****\$finish called from file "PATTERN.V", line 118.
\$finish at simulation time 1003228500
VCS Simulation Report
Time: 1003228500 ps
CPU Time: 19.590 seconds; Data structure size: 8.1Mb
Thu May 29 03:52 2025
CPU time: 3.960 seconds to compile + 1.404 seconds to elaboration + .993 seconds to link + 20.018 seconds in simulation
3:52 iclab036@ee24~/Lab12_2025S/Exercise/06_POST\$

Remote monitoring

Follow terminal folder

9. Power result :

A screenshot of a terminal window titled "ee24.s12.iee.nycu.edu.tw (iclab036)". The window includes a top menu bar with "Terminal", "Sessions", "View", "Xserver", "Tools", "Games", "Settings", "Macros", and "Help". Below the menu is a toolbar with icons for "Session", "Servers", "Tools", "Games", "Sessions", "View", "Split", "MultiExec", "Tunneling", and "Packages". A "Settings" icon is also present. On the right side, there are "X server" and "Exit" buttons. The main area contains a "Quick connect..." search bar and a file browser. The browser shows a directory path: "/RAID2/COURSE/2025_Spring/iclab/iclab036/Lab12_2025S/Exercise/05_APR/". Inside this directory, several files are listed: "..", ".cadence", "CetiC", "CHP.jnn.dat", "CHP_floooran.jnn.dat", "CHP_nanoRoute.inn.dat", and "CHP_posiCTS.inn.dat". The "CHP.jnn.dat" file was modified on 2025-05-28 at 1:25 PM. To the right of the file list, a message box displays a warning: "/* WARN: (EMS-27): Message (VOLTUS_PWR-2152) has exceeded the current message display limit of 20. To increase the message display limit, refer to the product command reference manual." Below the message box, a "Total Power" section provides detailed power consumption data:

	Total Internal Power:	55.7196%
Total Switching Power:	2.98829508	43.9379%
Total Leakage Power:	0.02325016	0.3425%
Total Power:	6.78865778	

10. IR Drop Results :

I separated the power pads, so that every side of the core has at least one core power pad. For I/O power pads, my strategy was to let a I/O power pad support 3~4 I/O ports.

