48 LINE SYSTEM BUS OUTLINE

B1 - low true WAIT When pulled low by a system board, causes processor clock to slow down to speed of approximately 500KHz on most processor boards. This is used to service slow memory and I/O devices.

B2 - NMI (non-maskable interrupt) When brought low, a non-blockable interrupt occurs, causing the processor to stop its operation and service this interrupt, that is, go to a specific memory location and start executing an interrupt service routine.

B3 - IRQ (interrupt request) An interrupt which can be masked by the processor, that is, the processor can choose to ignore this interrupt under program control. If the interrupt is not masked, it will cause the processor to stop executing the program it is in, and jump to a different location.

B4 - DD (data direction) When pulled low by system board, it changes the direction of the 8T26 buffers on the CPU board, and thus switches the processor from outputing data to the bus to listening to the bus.

B5 - D0
B6 - D1
B7 - D2
B8 - D3
B9 - D4
B10 - D5
B11 - D6
B12 - D7

Bi-directional eight-bit wide data bus for communication of data between the processor and system boards.

B13
B14
B15
B16

Upper data bits on some systems

B17 Optional reset line used to clear all PIAs and similar I/O circuitry in the system.

B18 spare line

B19
B20
B21
B22

Memory management address lines: Lines 21 and 22 are used on systems with a 500 CPU Board; all 4 are used with the 510.

B23 +12 Power connection

B24 -9 Power connection

B25
B26

+5 Power connection

B27
B28

Ground Connection

B29 - A6
B30 - A7
B31 - A5
B32 - A8
B33 - A9
B34 - A1
B35 - A2
B36 - A3
B37 - A4
B38 - A0

Ten low-order address lines

B39 - Ø2 Used to clock external circuits or external I/O interfaces, such as the A/D converter.

B40 - R/W (read/write) Originates at the microprocessor and specifies read or write operations on the data bus.