M5T 4044 P-20, S-20; P-30, S-30; P-45, S-45

4096-BIT (4096-WORD BY 1-BIT) STATIC RAM

DESCRIPTION

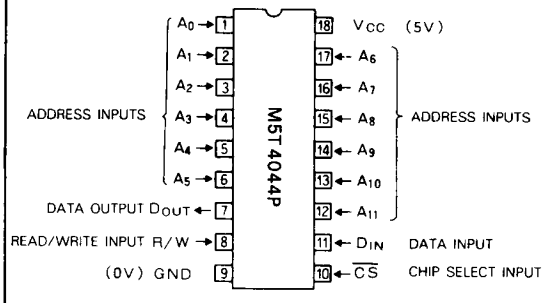
This is a family of 4096-word by 1-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. They operate with a single 5V supply, as does TTL, and are directly TTL-compatible.

FEATURES

Parameter	M5T 4044 P,S-20	M5T 4044 P,S-30	M5T 4044 P,S-45
Access time (max)	200ns	300ns	450ns
Cycle time (min)	200ns	300ns	450ns

- Low power dissipation: 50μw/bit (typ)
- Single 5V supply (±10% tolerance)
- Requires no clocks or refreshing
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state and have OR-tie capability
- Simple memory expansion by chip-select ($\overline{CS}$) input
- Interchangeable with TI's TMS4044 in pin configuration and electrical characteristics

PIN CONFIGURATION (TOP VIEW)



Outline 18P1 (M5T4044P)
18S1 (M5T4044S)

APPLICATION

- Small-capacity memory units

FUNCTION

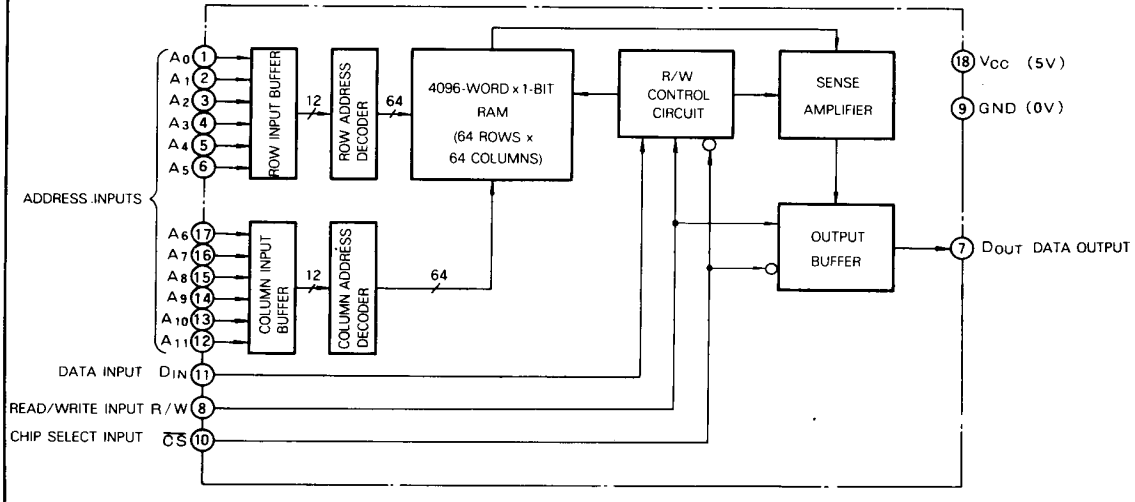
These devices are very convenient to use, as they feature static circuits which require neither external clocks nor refreshing, and all inputs and outputs are directly compatible with TTL.

During a write cycle, when a location is designated by address signals $A_0 \sim A_{11}$ and the R/W signal goes low, the D_{IN} signal data at that time is written.

During a read cycle, when the R/W signal goes high and a location is designated by address signals $A_0 \sim A_{11}$, the data of the designated address is available at the D_{OUT} terminals.

When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

BLOCK DIAGRAM



M5T 4044 P-20, S-20; P-30, S-30; P-45, S-45

4096-BIT (4096-WORD BY 1-BIT) STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.5～7	V
V_I	Input voltage			−0.5～7	V
V_O	Output voltage			−0.5～7	V
P_d	Maximum power dissipation	M5T 4044P	Ta=25℃	700	mW
		M5T 4044S	Ta=25℃	1000	mW
Topr	Operating free-air ambient temperature range			0～70	℃
Tstg	Storage temperature range	M5T 4044P		−40～125	℃
		M5T 4044S		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Units
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −200μA, V_{CC} = 4.5V	2.4			V
V_{OH}	High-level output voltage	I_{OH} = −1.0mA, V_{CC} = 4.75V	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1mA			0.4	V
I_I	Input current	V_I = 0 ~ 5.5V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS})}$ = 2V, V_O = 2.4V ~ V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS})}$ = 2V, V_O = 0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I = 5.5V, (all inputs), output open, Ta = 25°C		40	65	mA
C_i	Input capacitance, all inputs	V_I = GND, V_i = 25mVrms, f = 1MHz		3	5	pF
C_o	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz		5	8	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (Ta = 0 ~ 70℃, V_{CC} = 5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5T 4044P-20,S-20			M5T 4044P-30,S-30			M5T 4044P-45,S-45			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	200			300			450			ns
$t_{SU(AD)}$	Address setup time with respect to write pulse	0			0			0			ns
$t_{W(WR)}$	Write pulse width	120			150			200			ns
t_{WR}	Write recovery time	0			0			0			ns
$t_{SU(DA)}$	Data setup time	120			150			200			ns
$t_{H(DA)}$	Data hold time	0			0			0			ns
$t_{SU(\overline{CS})}$	Chip select setup time	120			150			200			ns
$t_{PXZ(WR)}$	Output disable time with respect to write pulse			40			80			100	ns

SWITCHING CHARACTERISTICS (For Read Cycle) (Ta = 0 ~ 70℃, V_{CC} = 5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5T 4044P-20,S-20			M5T 4044P-30,S-30			M5T 4044P-45,S-45			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	200			300			450			ns
$t_{a(AD)}$	Address access time			200			300			450	ns
$t_{a(\overline{CS})}$	Chip select access time			70			100			100	ns
$t_{PXZ(\overline{CS})}$	Output disable time with respect to chip select			40			80			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	50			50			50			ns

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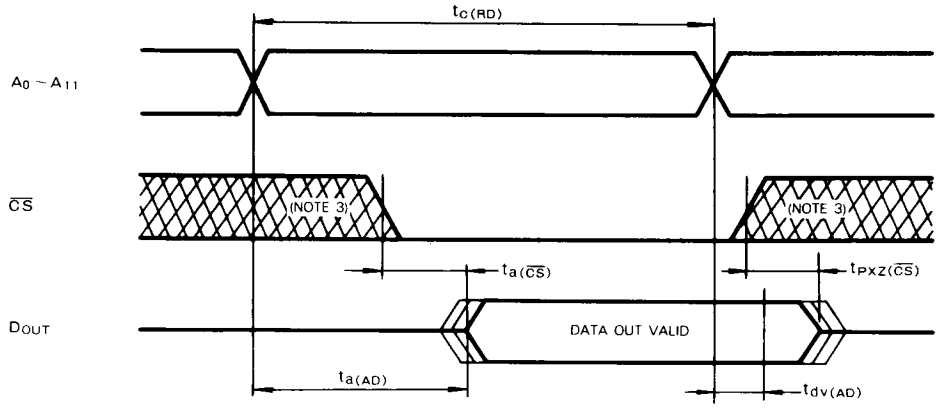
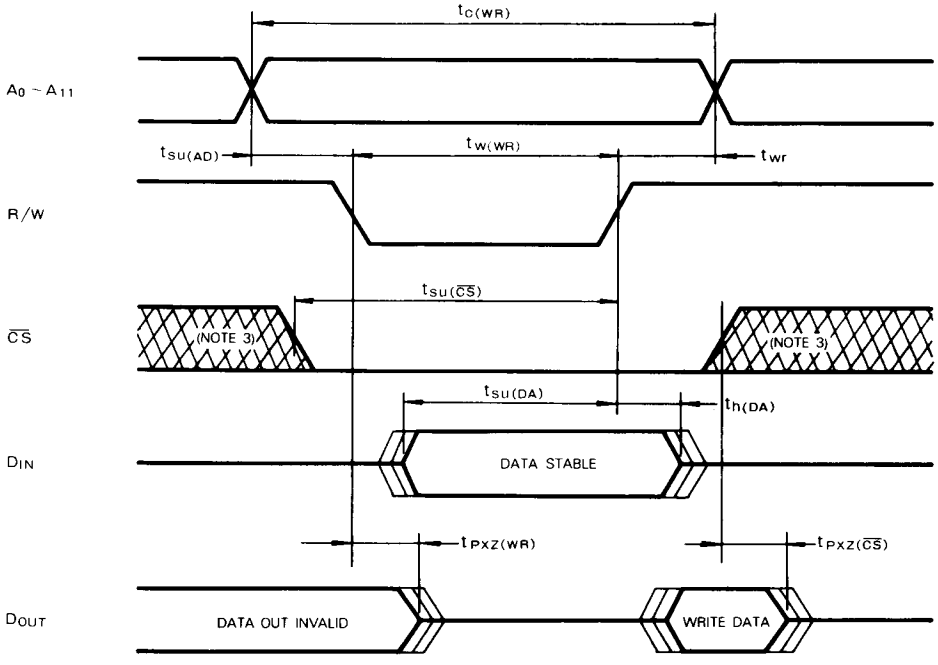
TIMING DIAGRAMS

Read Cycle



Write Cycle

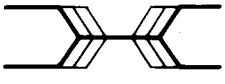


Note : 2 Test conditions

Input pulse level	0.8 ~ 2 V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level	
Input	1.5 V
Output	1.5 V

Load = 1TTL, C_L = 100pF

Note 3 : Hatching indicates the state is don't care.

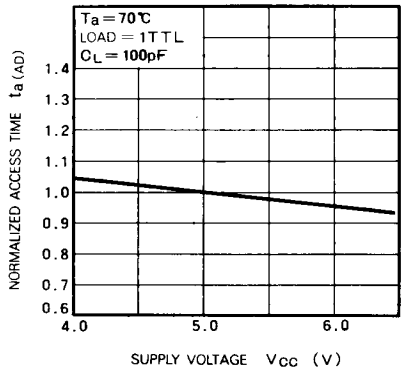


The center line indicates a floating (high-impedance) state.

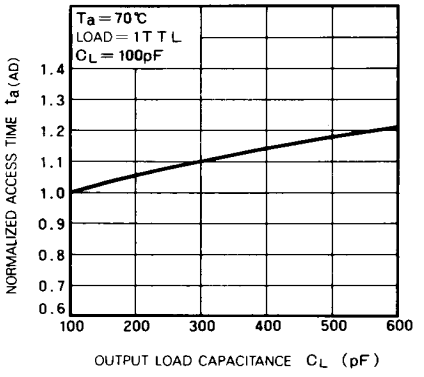
4096-BIT (4096-WORD BY 1-BIT) STATIC RAM

TYPICAL CHARACTERISTICS

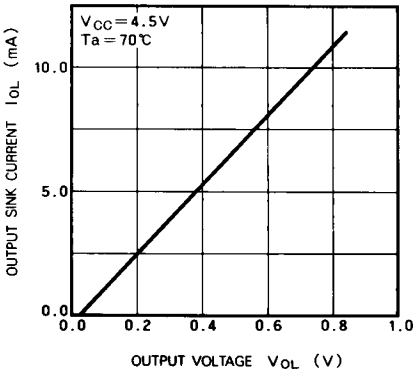
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



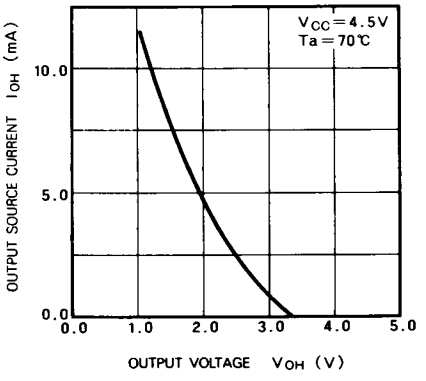
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

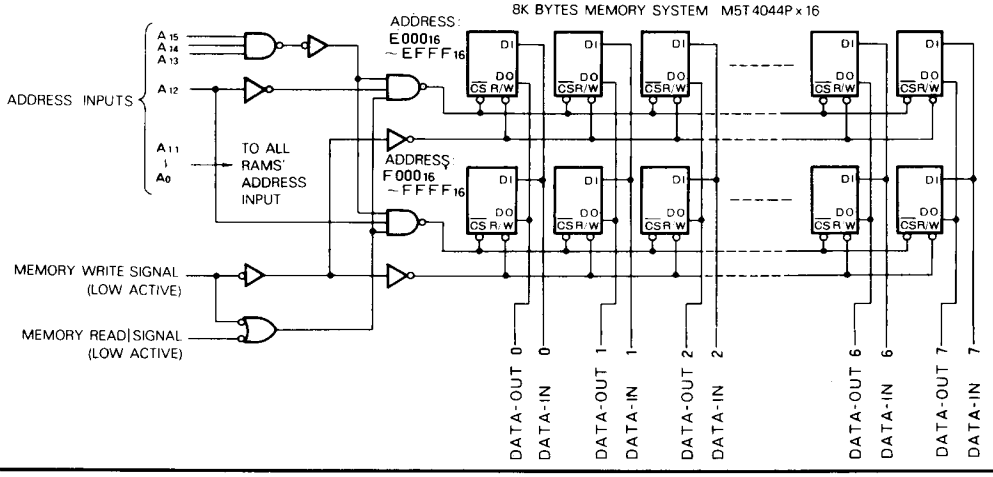


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL APPLICATION (for 8K-Byte Memory System)

This circuit is designed for a separate data bus application; and input can be tied.
if a common data bus application is required, the output



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