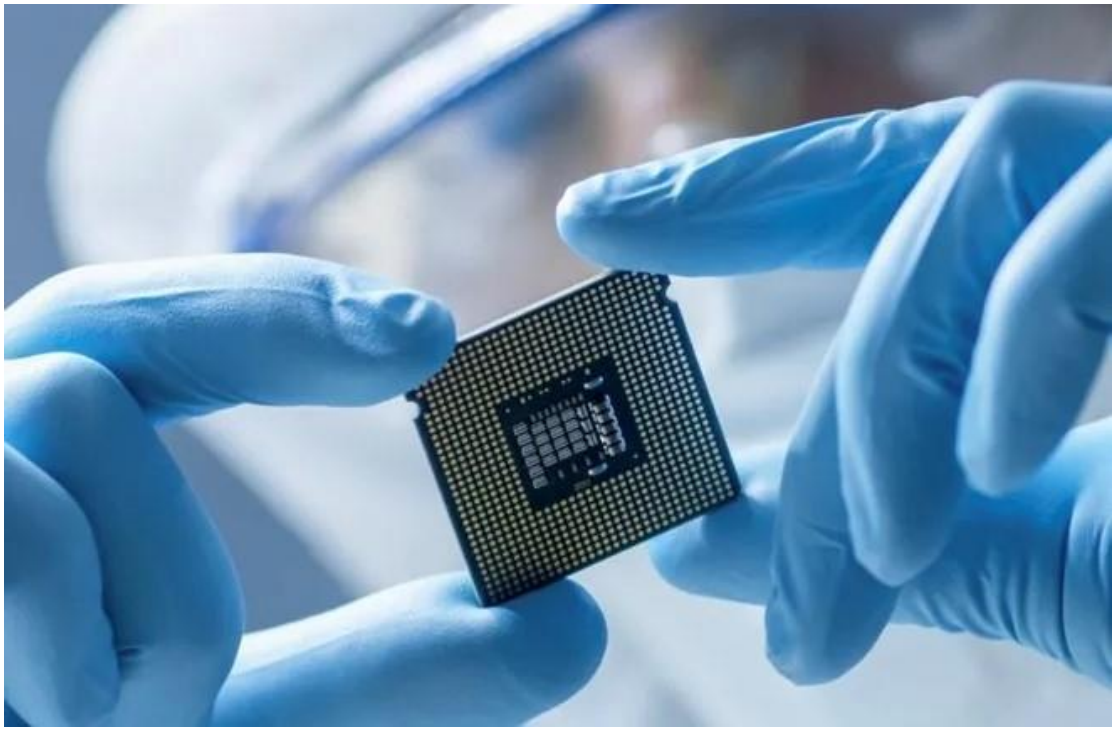

數位系統設計作業

HW1

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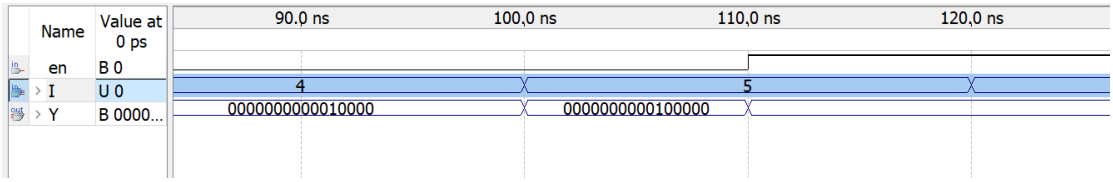
題目: 用 2 to 4 decoder with en 組成 4 to 16 decoder with en

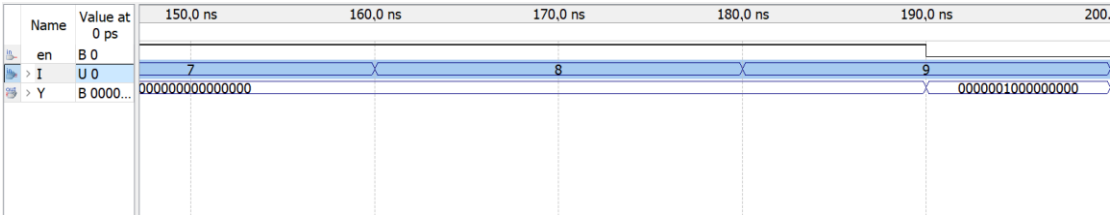
程式碼

```vhdl
library IEEE;
use ieee.std_logic_1164.all;

entity decorder2to4_enComdecorder4to16 is
    port(
        I:in std_logic_vector(3 downto 0);          --輸入
        en:in std_logic;                            --是否運作
        Y:out std_logic_vector(15 downto 0)         --輸出
    );
end decorder2to4_enComdecorder4to16;

architecture decorder2to4_enComdecorder4to16 of decorder2to4_enComdecorder4to16 is
        signal decorder2to4_out:std_logic_vector(3 downto 0);          --設定 two to four decorder 的輸出
begin
        decorder2to4_out <= "1111" when en = '1' else                  --設定 0 work，當 enable 為 1 ，輸出為1111
                            "1110" when I(3 downto 2) = "00" else
                            "1101" when I(3 downto 2) = "01" else
                            "1011" when I(3 downto 2) = "10" else
                            "0111" when I(3 downto 2) = "11";

                    Y <= "0000000000000001" when (I(1 downto 0) = "00" and decorder2to4_out(0) = '0') else --當LSB為 0，就啟動該decorder
                         "0000000000000010" when (I(1 downto 0) = "01" and decorder2to4_out(0) = '0') else
                         "0000000000000100" when (I(1 downto 0) = "10" and decorder2to4_out(0) = '0') else
                         "0000000000001000" when (I(1 downto 0) = "11" and decorder2to4_out(0) = '0') else

                         "0000000000010000" when (I(1 downto 0) = "00" and decorder2to4_out(1) = '0') else --當LSB左方bit為 0，啟動該decorder
                         "0000000000100000" when (I(1 downto 0) = "01" and decorder2to4_out(1) = '0') else
                         "0000000001000000" when (I(1 downto 0) = "10" and decorder2to4_out(1) = '0') else
                         "0000000010000000" when (I(1 downto 0) = "11" and decorder2to4_out(1) = '0') else

                         "0000000100000000" when (I(1 downto 0) = "00" and decorder2to4_out(2) = '0') else --當MSB右方bit為 0，啟動該decorder3
                         "0000001000000000" when (I(1 downto 0) = "01" and decorder2to4_out(2) = '0') else
                         "0000010000000000" when (I(1 downto 0) = "10" and decorder2to4_out(2) = '0') else
                         "0000100000000000" when (I(1 downto 0) = "11" and decorder2to4_out(2) = '0') else

                         "0001000000000000" when (I(1 downto 0) = "00" and decorder2to4_out(3) = '0') else --當MSB為 0，啟動該decorder
                         "0010000000000000" when (I(1 downto 0) = "01" and decorder2to4_out(3) = '0') else
                         "0100000000000000" when (I(1 downto 0) = "10" and decorder2to4_out(3) = '0') else
                         "1000000000000000" when (I(1 downto 0) = "11" and decorder2to4_out(3) = '0') else
                         "0000000000000000";
end decorder2to4_enComdecorder4to16;
```

波形圖

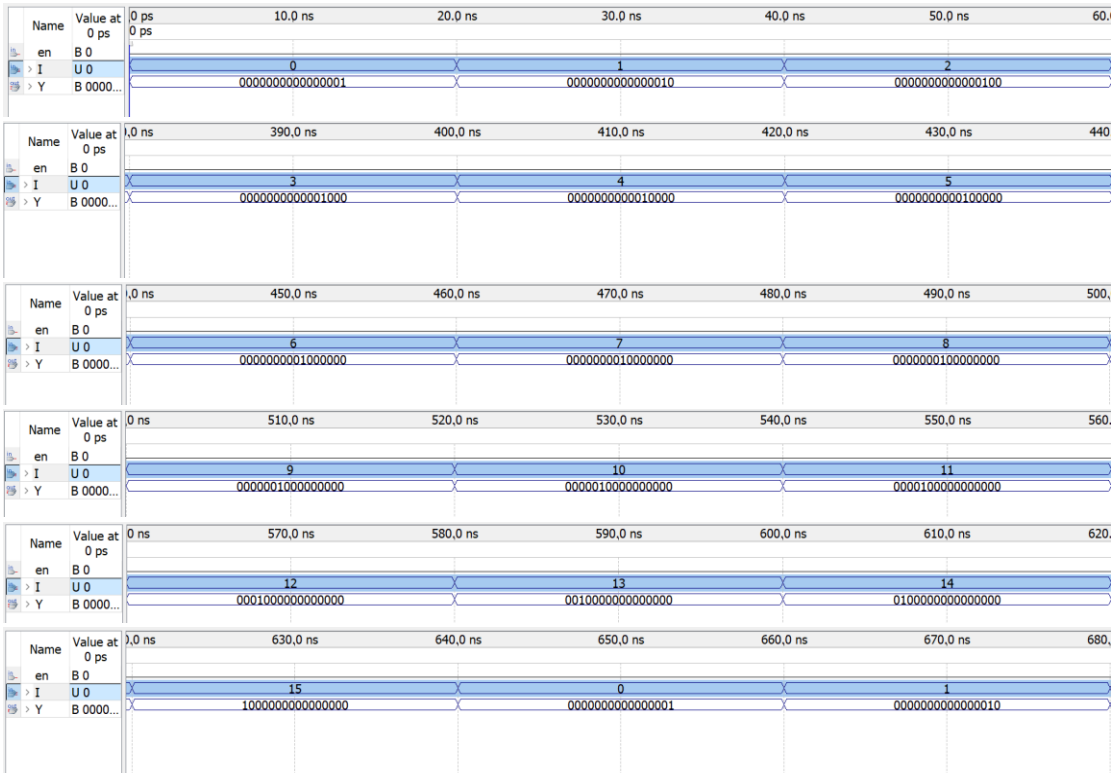
1. 例外處理：





顯現出如果 enable 為 1，全部輸出皆為 0，而非保留上一狀態

2. 全部：



表現出全部輸出皆符合預先預期，在第 I 個 bit 上輸出為 1

心得：

從此次實驗的過程中，我更熟悉如何撰寫 VHDL 語言，知悉其語法。上方波型圖也有明確表現出例外處理，關於如果在執行中途遇到 enable 觸發，確實如同程式碼表達的全部位元皆為 0，而非保留上一狀態的結果。

也了解到如果並非像本人所寫全部 bit 都一次輸入，而是分成四段分別判斷，需要在 enable 為觸發時將上一結果全部清為 0，否則結果會出現多於一個 1 的狀況。