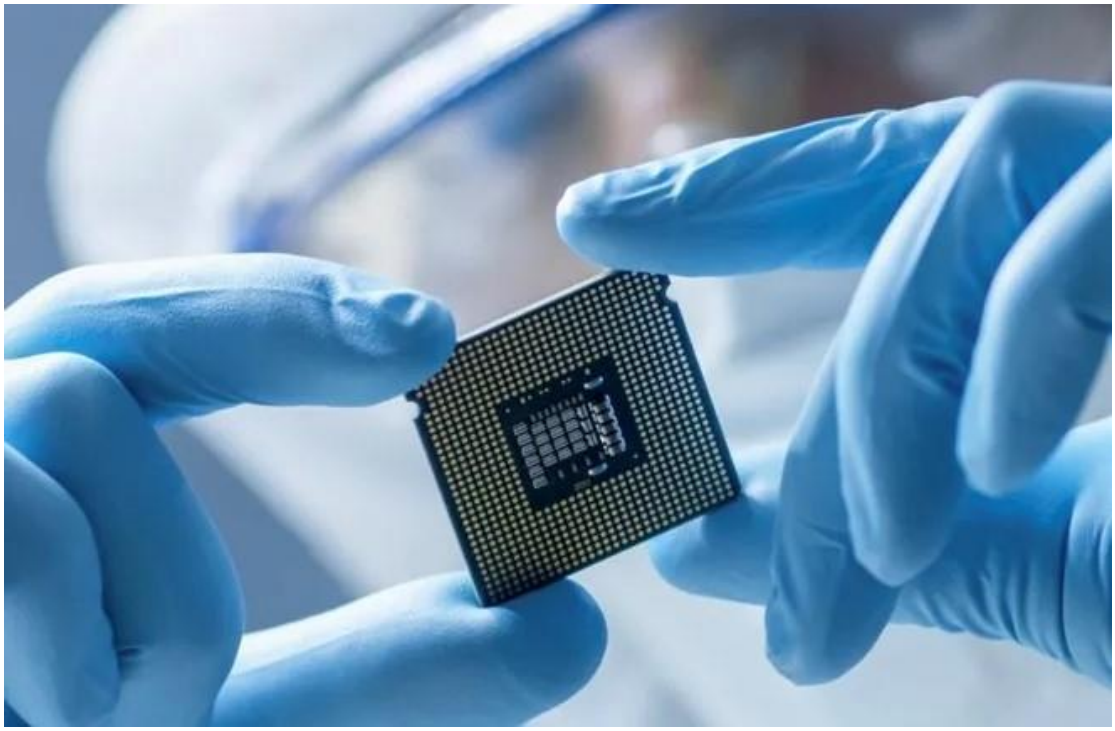

數位系統設計作業

HW3

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第一題

程式碼

可能 1：

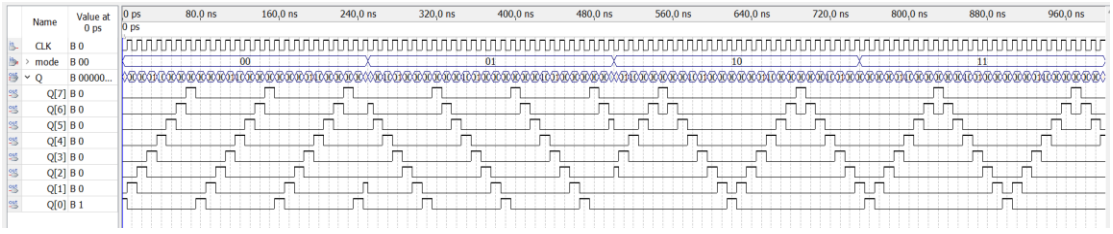
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity counter is
    port(
        CLK:in std_logic;
        mode:in std_logic_vector(1 downto 0);
        Q:out std_logic_vector(7 downto 0)
    );
end counter;

architecture counter of counter is
    signal cnt:std_logic_vector(3 downto 0);                    --計數器
begin
    process(CLK)
    begin
        if rising_edge(CLK) then
            if (mode="10" or mode="11") and (cnt=x"D") then      --只有當模式"10"和"11"會在D結束一個週期
                cnt <= (others => '0');
            else
                cnt <= cnt + '1';                               --除了歸零即計數器上數
            end if;
        end if;
    end process;
```

```vhdl

    process(mode)
    begin
        if mode="00" then                                       --令模式"00"為波型Q輸出
            case cnt is
                when x"0" => Q <= "00000001";
                when x"1" => Q <= "00000010";
                when x"2" => Q <= "00000100";
                when x"3" => Q <= "00001000";
                when x"4" => Q <= "00010000";
                when x"5" => Q <= "00100000";
                when x"6" => Q <= "01000000";
                when x"7" => Q <= "10000000";
                when x"8" => Q <= "00000001";
                when x"9" => Q <= "00000010";
                when x"A" => Q <= "00000100";
                when x"B" => Q <= "00001000";
                when x"C" => Q <= "00010000";
                when x"D" => Q <= "00100000";
                when x"E" => Q <= "01000000";
                when others => Q <= "10000000";
            end case;
```

```
49          elsif mode="01" then                                    --令模式"01"為波型Q輸出
50              case cnt is
51                  when x"0" => Q <= "10000000";
52                  when x"1" => Q <= "01000000";
53                  when x"2" => Q <= "00100000";
54                  when x"3" => Q <= "00010000";
55                  when x"4" => Q <= "00001000";
56                  when x"5" => Q <= "00000100";
57                  when x"6" => Q <= "00000010";
58                  when x"7" => Q <= "00000001";
59                  when x"8" => Q <= "10000000";
60                  when x"9" => Q <= "01000000";
61                  when x"A" => Q <= "00100000";
62                  when x"B" => Q <= "00010000";
63                  when x"C" => Q <= "00001000";
64                  when x"D" => Q <= "00000100";
65                  when x"E" => Q <= "00000010";
66                  when others => Q <= "00000001";
67              end case;
```

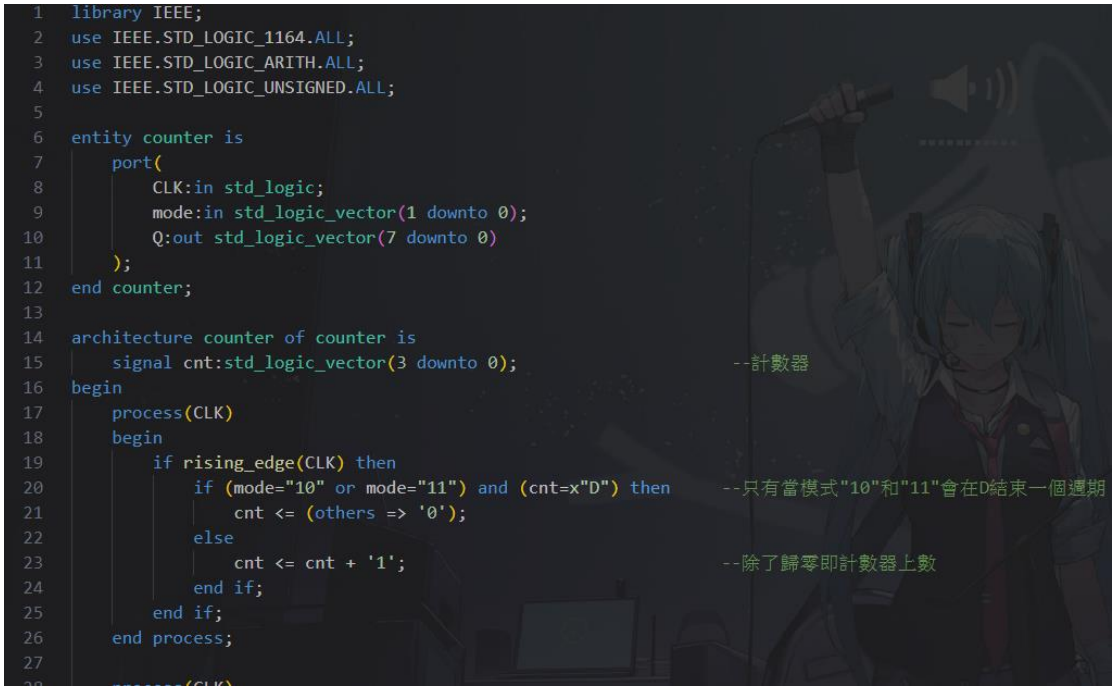
```
68          elsif (mode="10" or mode="11") then                     --令模式"10"和"11"為波型Q輸出
69              case cnt is
70                  when x"0" => Q <= "00000001";
71                  when x"1" => Q <= "00000010";
72                  when x"2" => Q <= "00000100";
73                  when x"3" => Q <= "00001000";
74                  when x"4" => Q <= "00010000";
75                  when x"5" => Q <= "00100000";
76                  when x"6" => Q <= "01000000";
77                  when x"7" => Q <= "10000000";
78                  when x"8" => Q <= "01000000";
79                  when x"9" => Q <= "00100000";
80                  when x"A" => Q <= "00010000";
81                  when x"B" => Q <= "00001000";
82                  when x"C" => Q <= "00000100";
83                  when others => Q <= "00000010";
84              end case;
85          end if;
86      end process;
87  end counter ; -- counter
```

已知計數最多 15，選用 4 bits 計數



問題：猜測老師給 clk 應該為正緣接受改變

可能二：



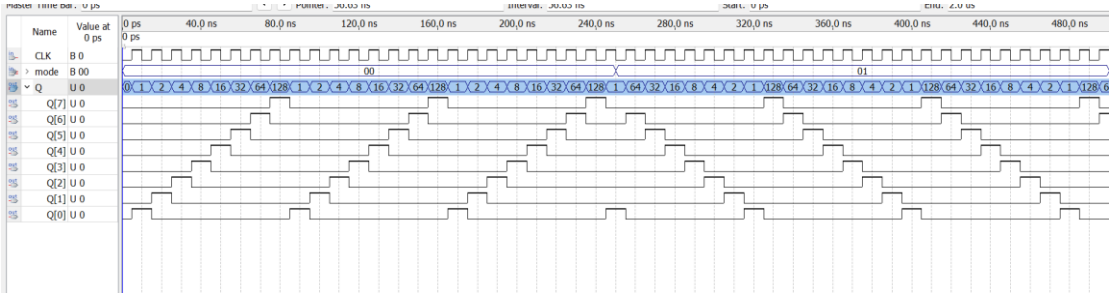
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity counter is
    port(
        CLK:in std_logic;
        mode:in std_logic_vector(1 downto 0);
        Q:out std_logic_vector(7 downto 0)
    );
end counter;

architecture counter of counter is
    signal cnt:std_logic_vector(3 downto 0);                    --計數器
begin
    process(CLK)
    begin
        if rising_edge(CLK) then
            if (mode="10" or mode="11") and (cnt=x"D") then      --只有當模式"10"和"11"會在D結束一個週期
                cnt <= (others => '0');
            else
                cnt <= cnt + '1';                               --除了歸零即計數器上數
            end if;
        end if;
    end process;
```

```vhdl
    process(CLK)
    begin
        if rising_edge(CLK) then                                --令A正緣才觸發
            if mode="00" then                                   --令模式"00"為波型Q輸出
                case cnt is
                    when x"0" => Q <= "00000001";
                    when x"1" => Q <= "00000010";
                    when x"2" => Q <= "00000100";
                    when x"3" => Q <= "00001000";
                    when x"4" => Q <= "00010000";
                    when x"5" => Q <= "00100000";
                    when x"6" => Q <= "01000000";
                    when x"7" => Q <= "10000000";
                    when x"8" => Q <= "00000001";
                    when x"9" => Q <= "00000010";
                    when x"A" => Q <= "00000100";
                    when x"B" => Q <= "00001000";
                    when x"C" => Q <= "00010000";
                    when x"D" => Q <= "00100000";
                    when x"E" => Q <= "01000000";
                    when others => Q <= "10000000";
                end case;
```

```
50              elsif mode="01" then                                    --令模式"01"為波型Q輸出
51                  case cnt is
52                      when x"0" => Q <= "10000000";
53                      when x"1" => Q <= "01000000";
54                      when x"2" => Q <= "00100000";
55                      when x"3" => Q <= "00010000";
56                      when x"4" => Q <= "00001000";
57                      when x"5" => Q <= "00000100";
58                      when x"6" => Q <= "00000010";
59                      when x"7" => Q <= "00000001";
60                      when x"8" => Q <= "10000000";
61                      when x"9" => Q <= "01000000";
62                      when x"A" => Q <= "00100000";
63                      when x"B" => Q <= "00010000";
64                      when x"C" => Q <= "00001000";
65                      when x"D" => Q <= "00000100";
66                      when x"E" => Q <= "00000010";
67                      when others => Q <= "00000001";
68                  end case;
```

```
69              elsif (mode="10" or mode="11") then                     --令模式"10"和"11"為波型Q輸出
70                  case cnt is
71                      when x"0" => Q <= "00000001";
72                      when x"1" => Q <= "00000010";
73                      when x"2" => Q <= "00000100";
74                      when x"3" => Q <= "00001000";
75                      when x"4" => Q <= "00010000";
76                      when x"5" => Q <= "00100000";
77                      when x"6" => Q <= "01000000";
78                      when x"7" => Q <= "10000000";
79                      when x"8" => Q <= "01000000";
80                      when x"9" => Q <= "00100000";
81                      when x"A" => Q <= "00010000";
82                      when x"B" => Q <= "00001000";
83                      when x"C" => Q <= "00000100";
84                      when others => Q <= "00000010";
85                  end case;
86              end if;
87          end if;
88      end process;
89  end counter ; -- counter
```

波形圖



確實在模式切換處依然等待正緣才更改該區間結果

加分題

程式碼

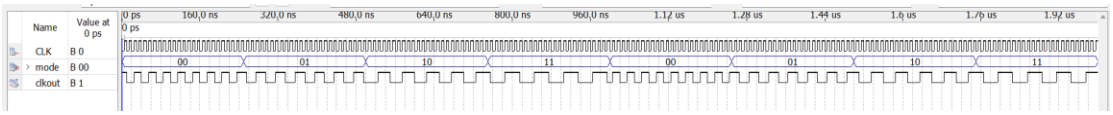
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity divClock is
    port(
        CLK:in std_logic;
        mode:in std_logic_vector(1 downto 0);
        clkout:out std_logic
    );
end divClock;
```

```
13
14  architecture divClock of divClock is
15      signal cnt:std_logic_vector(2 downto 0);            --最多數到6，3 bits計數器
16  begin
17      process(CLK)                                        --規定各區間計數器區間
18      begin
19          if rising_edge(CLK) then
20              if mode="00" then
21                  if cnt>="010" then
22                      cnt <= (others => '0');
23                  else
24                      cnt <= cnt+'1';
25                  end if;
26              elsif mode="01" then
27                  if cnt>="011" then
28                      cnt <= (others => '0');
29                  else
30                      cnt <= cnt+'1';
31                  end if;
32              elsif mode="10" then
33                  if cnt>="100" then
34                      cnt <= (others => '0');
35                  else
36                      cnt <= cnt+'1';
37                  end if;
38              elsif mode="11" then
39                  if cnt>="101" then
40                      cnt <= (others => '0');
41                  else
42                      cnt <= cnt+'1';
43                  end if;
44              end if;
45          end if;
46      end process;
```

```
47
48      process(mode, cnt)
49      begin
50          case mode is
51              when "00" =>                        --觀察發現如果需要copy CLK，1與0的設定不能交換
52                  if cnt<1 then
53                      clkout <= '1';
54                  elsif cnt>1 then
55                      clkout <= '0';
56                  else
57                      clkout <= CLK;
58                  end if;
59              when "01" =>                        --不需要複製CLK，偶數可整除2
60                  if cnt<2 then
61                      clkout <= '1';
62                  elsif cnt>=2 then
63                      clkout <= '0';
64                  end if;
65              when "10" =>
66                  if cnt<2 then
67                      clkout <= '1';
68                  elsif cnt>2 then
69                      clkout <= '0';
70                  else
71                      clkout <= CLK;
72                  end if;
73              when others =>
74                  if cnt<3 then
75                      clkout <= '1';
76                  elsif cnt>=3 then
77                      clkout <= '0';
78                  end if;
79          end case;
80      end process;
81  end divClock ; -- divClock
```

波形圖

確實每個區間街與設定的相同，在 00 以 3 clocks 為一週期，01 以 4 clocks 為一週期，10 以 5 clocks 為一週期，11 以 6 clocks 為一週期。



旨在說明 11 與 00 銜接處並無異常

心得

在此次實驗中，我學會了一個使用計數器根據不同的模式來改變輸出的波形。計數器在時鐘信號 CLK 的上升沿進行計數，並在不同模式下產生不同的波形。

也學會根據模式來決定計數器的最大值以生成不同的時鐘信號。每個模式對應一個不同的分頻比，通過計數器的上升沿進行累加，來分割輸入時鐘訊號。

感謝此次的實驗讓我學會在數位設計中如何利用計數器和分頻技術來控制時鐘和輸出信號。