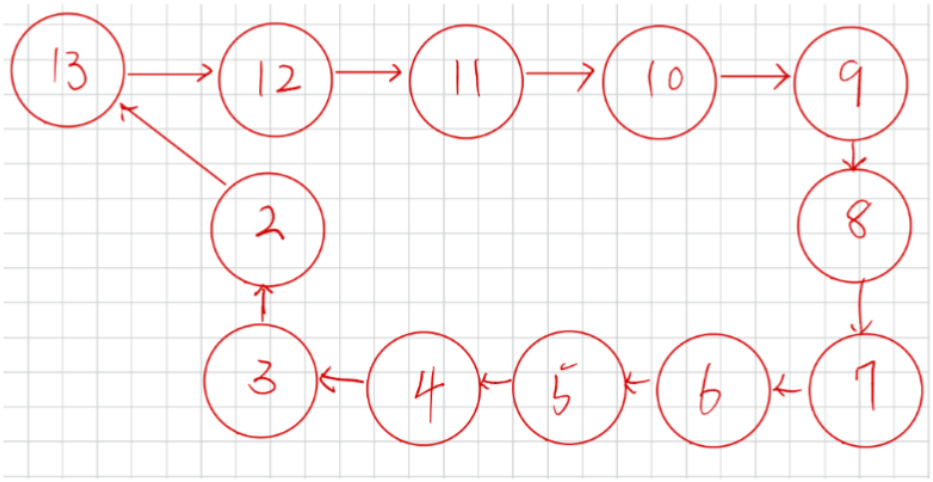
Digital Logic Design
Quiz 08
2024/05/28

姓名: 學號: 系級:

1. Design a 4-bit synchronous binary counter using four D flip-flops that counts from 13 to 2 and then restarts. Provide the following:
   a. State diagram (10%)
   b. State table (30%)
   c. Equation (60%)

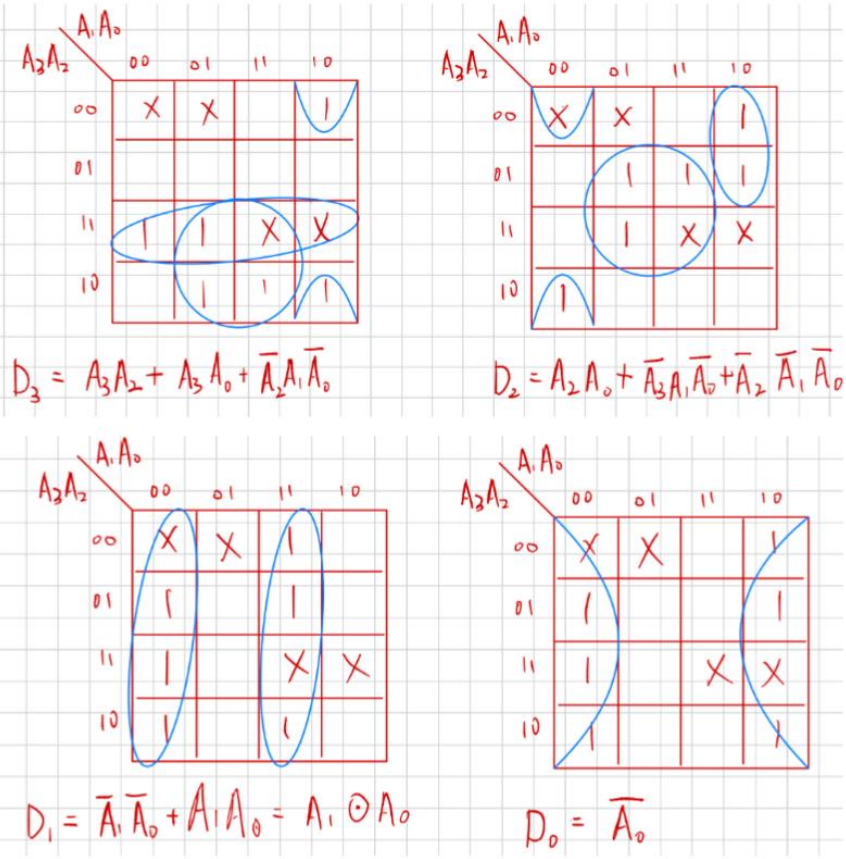
State diagram



State table

PS				NS			
A_3	A_2	A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	x	x	x	x
0	0	0	1	x	x	x	x
0	0	1	0	1	1	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	1	1	1
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	1
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	0	0
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

Equation


A1A0
A3A2
00 01 11 10
D3 = A3A2 + A3A0 + Ā2A1Ā0
D2 = A2A0 + Ā3A1Ā0 + Ā2Ā1Ā0
D1 = Ā1Ā0 + A1A0 = A1 ⊙ A0
D0 = Ā0