

# Digital Logic Design

## Quiz 07

2024/05/21

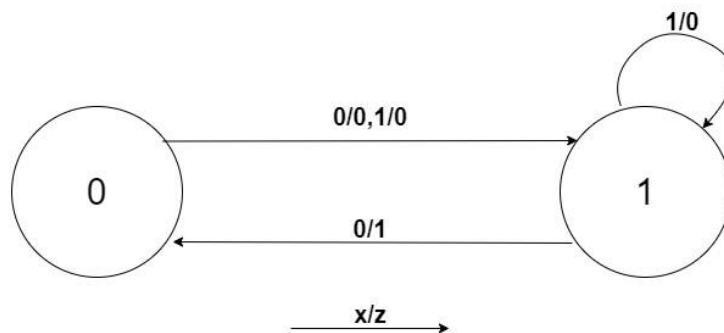
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1. Implement the following state diagram. Design a Sequential Circuit with one **T flip-flop**. You need to provide the **State Table**(20%), **Equation**(20%) and **Circuit Diagram** (20%).

Hint : present state :  $A(t)$  ; next state :  $A(t+1)$  ; input  $X$  ; output  $Z$  ;  
T flip-flops inputs :  $T_A$



2. Design and draw a four-bit shift register, the function as shown in table.

Hint : Register output :  $A_0A_1A_2A_3$  ; Load data :  $L_0L_1L_2L_3$  ; (40 %)

S1	S0	Register Operation
0	0	Load parallel data
0	1	Complement the four outputs
1	0	Left Rotation ex. $A_0A_1A_2A_3 \rightarrow A_1A_2A_3A_0$
1	1	If $A_i == L_i$ then register input equal 1, Else then register input equal 0.

(1)

### State Table

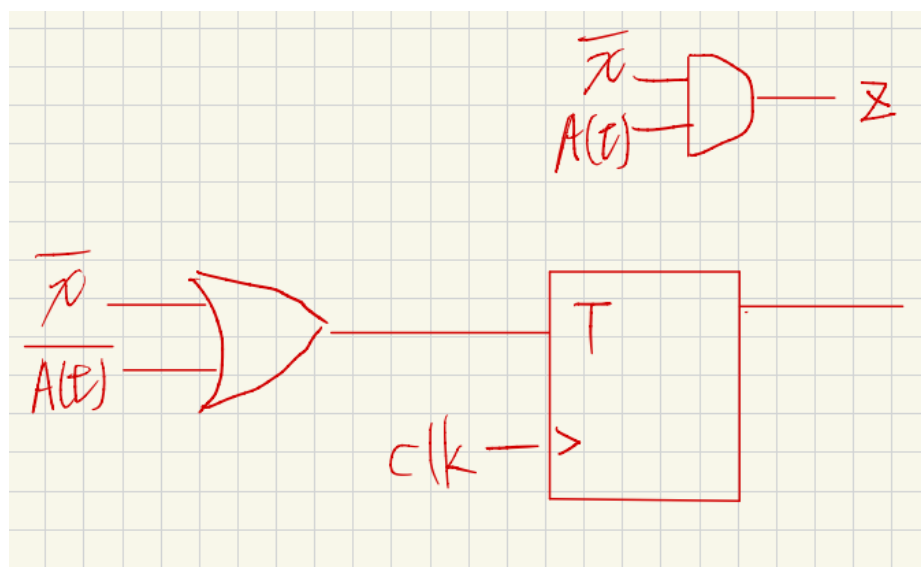
input $x$	PS $A(t)$	NS $A(t+1)$	output $z$	$T_A$
0	0	1	0	1
0	1	0	1	1
1	0	1	0	1
1	1	1	0	0

### Equation

$$Z = x'A(t)$$

$$T_A = x' + A(t)'$$

### Circuit Diagram



(2)

