Digital Logic Design
Quiz 05
2024/05/07

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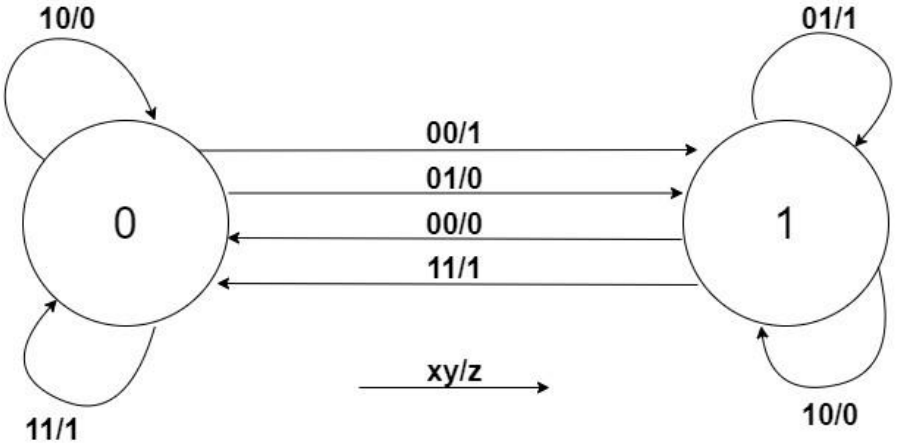
1. Implement the following state diagram



Hint : present state : A(t) ; next state : A(t+1) ; input X, Y ; output Z ; JK flip-flops inputs : J_A, K_A ;

(a) Design a **Sequential Circuit** with one **JK flip-flop**. You need to provide the **State Table** (40%), **Equations** (30%) and **Circuit Diagram** (30%).

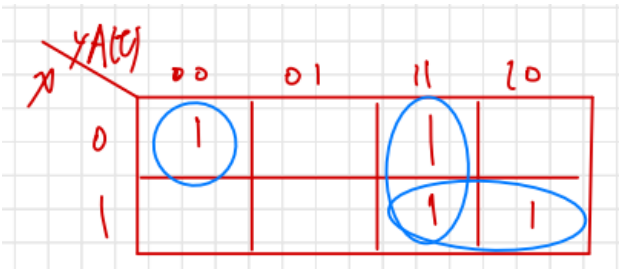
(a)

State Table

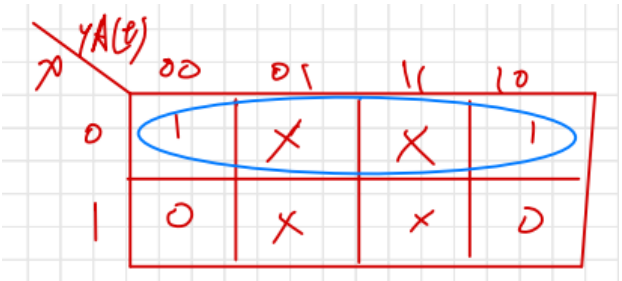
input x	input y	PS A(t)	NS A(t+1)	output z	J_A	K_A
0	0	0	1	1	1	X
0	0	1	0	0	X	1
0	1	0	1	0	1	X
0	1	1	1	1	X	0
1	0	0	0	0	0	X
1	0	1	1	0	X	0
1	1	0	0	1	0	X
1	1	1	0	1	X	1

Equation

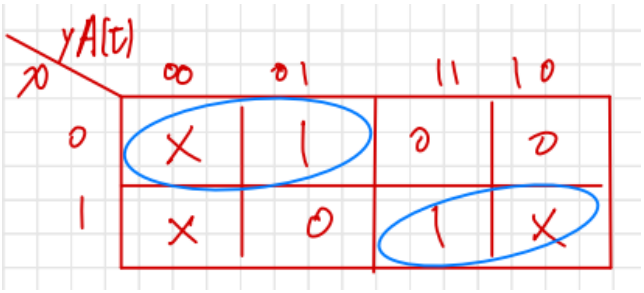
$$Z = yA(t) + xy + x'y'A(t)'$$



$$J_A = x'$$



$K_A = (x \oplus y)'$



Circuit Diagram