# RTL FILE of SAP1 Processor Project

## (Modifed Processor)


***Group:-*** *G7*

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### *Instructions Table:-*

| Instruction | Opcode | Memory Access | Meaning |
|---|---|---|---|
| **LDA** | *000* | *Yes (5-bit address)* | *Load Memory Word to ACC* |
| **ADD** | *001* | *Yes (5-bit address)* | *Add Memory Word to ACC* |
| **SUB** | *010* | *Yes (5-bit address)* | *Sub Memory Word from ACC* |
| **SHIFT LEFT** | *011* | *No* | *Shift the ACC to Left* |
| **SHIFT RIGHT** | *100* | *No* | *Shift the ACC to Right* |
| **OUT** | *101* | *No* | *Move the ACC content to Out register* |
| **HLT** | *111* | *No* | *Stop program execution* |

| Instruction | Time Signal | Phase | Micro-Operation | CP H | EP H | LM L | CE L | LI L | EI L | LA L | EA H | SU ALU | EU H | LB L | LO L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| XXX | *T1* | *Fetch* | *MAR* ← *PC* | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 00 | 0 | 1 | 1 |
| | *T2* | *Fetch* | *PC* ← *PC+1*<br>*IR* ← *RAM[MAR]* | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 00 | 0 | 1 | 1 |
| LDA | *T3* | *Execute* | *MAR* ← *IR(4..0)* | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 00 | 0 | 1 | 1 |
| | *T4* | *Execute* | *A* ← *RAM[MAR]*<br>*SC* ← *0* | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 00 | 0 | 1 | 1 |
| ADD | *T3* | *Execute* | *MAR* ← *IR(4..0)* | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 00 | 0 | 1 | 1 |
| | *T4* | *Execute* | *B* ← *RAM[MAR]* | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 00 | 0 | 0 | 1 |
| | *T5* | *Execute* | *A* ← *A + B*<br>*SC* ← *0* | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 00 | 1 | 1 | 1 |
| SUB | *T3* | *Execute* | *MAR* ← *IR(4..0)* | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 00 | 0 | 1 | 1 |
| | *T4* | *Execute* | *B* ← *RAM[MAR]* | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 00 | 0 | 0 | 1 |
| | *T5* | *Execute* | *A* ← *A + B' + 1*<br>*SC* ← *0* | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 11 | 1 | 1 | 1 |
| SHIFT LEFT | *T3* | *Execute* | *A* ← *SLL A*<br>*SC* ← *0* | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 10 | 1 | 1 | 1 |
| SHIFT RIGHT | *T3* | *Execute* | *A* ← *SRL A*<br>*SC* ← *0* | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 01 | 1 | 1 | 1 |
| OUT | *T3* | *Execute* | *OUT* ← *A*<br>*SC* ← *0* | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 00 | 0 | 1 | 0 |
| HLT | *T3* | *Execute* | *HALT* ← *1* | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 00 | 0 | 1 | 1 |