

Design and Performance of a Novel Miniaturized LTCC Wilkinson Power Divider

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Abstract—This paper presents the design and fabrication of a novel miniaturized low temperature co-fired ceramic (LTCC) Wilkinson power divider. By using the even-odd mode impedance theory, the analysis of this Wilkinson power divider is transformed to solve problems of impedance matching. LC impedance transformer is used to replace conventional transmission line to reduce the volume of the power divider. Build and optimize the schematic diagram through Agilent advanced design system (ADS) and then use Agilent high frequency structure simulator (HFSS) to build the 3D model. Finally, LTCC technology is used to manufacture the power divider. The test curves of the samples match well with the simulated curves. The insertion loss is less than 0.4dB from 3.1 GHz to 3.5 GHz, the return loss is better than 18dB and the isolation is better than 20dB. The size of the power divider is only 3.2mm × 1.6mm × 0.9mm.

Index Terms — power divider, miniaturization, even-odd mode, lumped elements, low temperature co-fired ceramics.

I. INTRODUCTION

The Wilkinson power divider plays an important role in communication systems [1], such as transceivers, phase arrays, and power amplifiers, owing to its ease of design and good performance. The conventional Wilkinson power divider provides perfect input and output port matching, high isolation and low insertion loss[2]. Due to the large size of Wilkinson power divider in lower frequencies, it's not applicable in many compact systems, such as handheld devices or airborne equipment. Many researches have been reported about how to reduce the size of Wilkinson power divider, they mostly use the method of step impedance transmission line [3].

In this paper, the lumped elements are used to replace conventional quarter-wavelength transmission lines in order to reduce the size of conventional Wilkinson power divider [4][5]. At the same time, LTCC technology which has the advantages of lower insertion loss, higher quality factors and more flexible way to embed passive components compared with PCB technique has been adopted to fabricate the power divider.

The specific indexes of the power divider are as follows

- 1) The insertion loss should be less than 0.5dB from 3.1GHz to 3.5GHz.
- 2) The return loss and isolation between two output ports should be better than 15dB.
- 3) The size of the power divider should be 3.2mm× 1.6mm ×0.9mm.

II. THEORETICAL ANALYSIS

The configuration of the proposed Wilkinson power divider is shown in Fig.1. It basically consists of two symmetrical inductors L_1 , L_1 , a ground capacitor C_1 , a capacitor C_2 and a resistor $2Z_0$ between the port 2 and port 3. The termination resistance of the input and output ports are Z_0 ($Z_0=50\Omega$) without using additional ports-matching networks. The S parameters of the three ports should satisfy

$$\begin{aligned} S_{11} &= S_{22} = S_{33} = 0 \\ |S_{21}|^2 &= |S_{31}|^2 = 1/2 \\ \angle S_{21} &= \angle S_{31} \end{aligned} \quad (1)$$

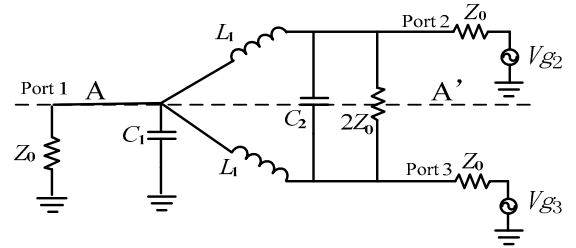


Fig.1 The layout of the proposed Wilkinson power divider

In order to analyze the operating modes of this power divider, we can use the method of even-odd mode excitation [6][7]. Firstly, we should define two separated excitation modes, where $V_{g2}=V_{g3}=2V_0$ is the even mode excitation and $V_{g2}=-V_{g3}=2V_0$ is the odd mode excitation. Subsequently, we combine the two modes to get the valid excitation as $V_{g2}=4V_0$, $V_{g3}=0$. Thus, The S parameters of this network can be obtained.

Under even-mode excitation, there is no current flowing through $2Z_0$ and C_2 . Therefore, we can split this power divider by center axis A-A' into two parts. The equivalent circuit is given in Fig.2. The input impedance of port 2 should be written as

$$\begin{aligned} Z_{2in}^e &= 2Z_0 // \frac{1}{j\omega C_1/2} + j\omega L_1 \\ &= \frac{2Z_0 - \omega^2 L_1 C_1 Z_0 + j\omega L_1}{j\omega C_1 Z_0 + 1} \end{aligned} \quad (2)$$

Where ω is the center angular frequency of operation frequency.

According to (1), the input impedance of Port 2 should satisfy

$$Z_{2in}^e = Z_0 \quad (3)$$

Therefore, the value of L_1 and C_1 can be deprived based on (2) and (3) as

$$\begin{aligned} L_1 &= \frac{Z_0}{\omega} \\ C_1 &= \frac{1}{\omega Z_0} \end{aligned} \quad (4)$$

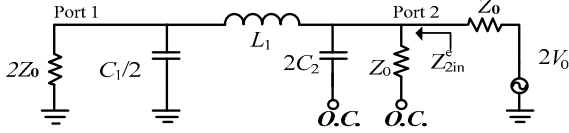


Fig.2 The equivalent circuit of the proposed power divider under even-mode excitation

Under odd-mode excitation, the node voltage on the center axis A-A' is zero. Where the equivalent circuit of the proposed power divider can be modified as is shown in Fig.3. The input impedance of port 2 is

$$\begin{aligned} Z_{2in}^o &= j\omega L_1 // \frac{1}{j\omega 2C_2} // Z_0 \\ &= \frac{j\omega L_1 Z_0}{Z_0 - 2\omega^2 L_1 C_2 Z_0 + j\omega L_1} \end{aligned} \quad (5)$$

According to (1), (4), the value of C_2 can be obtained as

$$C_2 = \frac{1}{2\omega^2 L_1} = \frac{1}{2\omega Z_0} \quad (6)$$

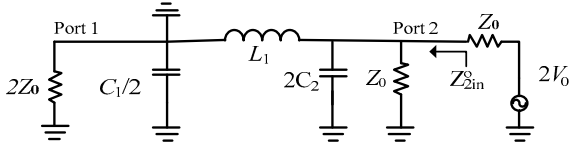


Fig.3 The equivalent circuit of the proposed power divider under odd-mode excitation

Finally, we should verify whether the input port is matched when both the output ports are matched [8]. In this condition, it seems to be like under even-mode excitation. Since $V_{port2} = V_{port3}$, there is no current flowing through C_2 and $2Z_0$. We can remove these two components for the sake of simplicity. The equivalent circuit is shown in Fig.4. By using (4), the input impedance of Port 1 can be obtained as

$$\begin{aligned} Z_{1in} &= \frac{1}{j\omega C_1} // (j\omega L_1 + Z_0) // (j\omega L_1 + Z_0) \\ &= Z_0 \end{aligned} \quad (7)$$

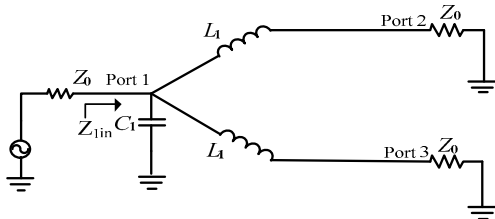


Fig.4 The layout of the proposed power divider when the output ports are matched

Therefore, when the values of L_1 , C_1 , C_2 satisfy (4) and (6), all the ports of the proposed power divider will be matched, only signals come from port 2 or port 3 will be consumed by the isolation resistor.

II. DESIGN AND SIMULATION

Calculate the values of L_1 , C_1 and C_2 according to (4) and (6), then use ADS to build the ideal schematic diagram. However, the values of the lumped components we calculated may not be the best. Thus, the optim widget in ADS can be used to get the optimized values. The values of the components are

$$L_1 = 2.412nH; C_1 = 0.960pF; C_2 = 0.483pF \quad (8)$$

Consequently, we will build the 3D model of this power divider in HFSS, the electrical constant and the loss angle of ceramic substrate we use is 6.2 and 0.002. The internal structure of the power divider is shown in Fig.5. pin 1, pin 3 and pin 5 are used to connect the common ground, pin 2 is used to input the signal, pin 4 and pin 6 are used to output the signal. All the components are labeled in Fig.5, respectively.

On account of the parasitic effects of lumped elements in SHF band, we still need to tune the values of the elements to counteract the parasitic effects and interference between different elements. Through a lot work of debugging, the simulated performance in HFSS is excellent which is shown in Fig.6. The insertion loss is less than 0.2 dB, the return loss and isolation are both better than 20dB and the phase unbalance between pin 4 and pin 6 is less than 1.4°.

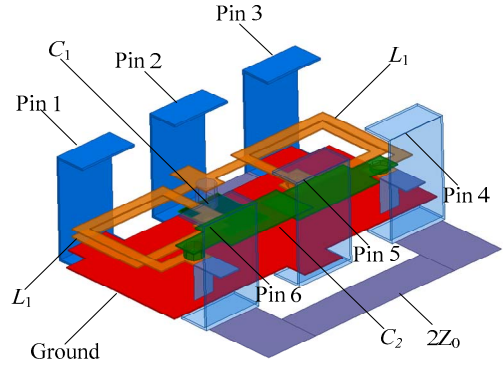


Fig.5 3D model of the proposed power divider

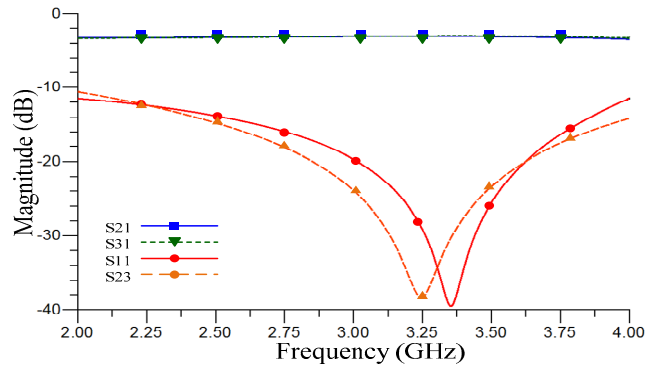


Fig.6 The simulated frequency responses of the power divider

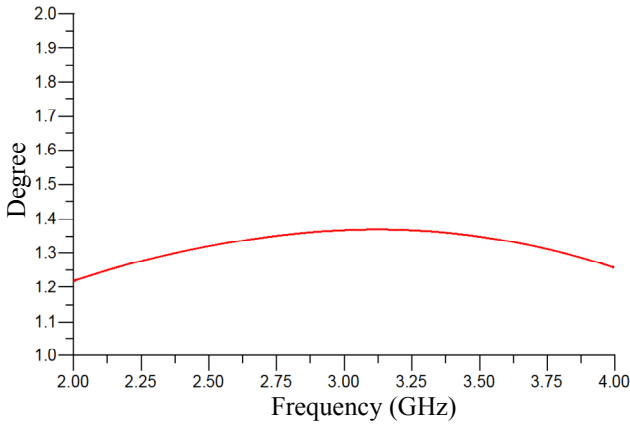


Fig.7 The simulated phase unbalance between out put ports

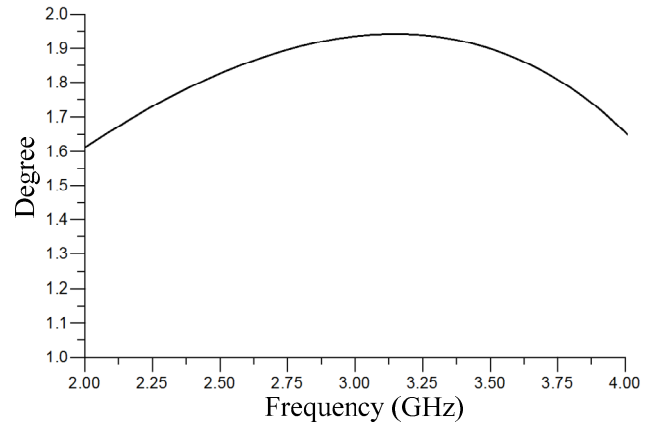


Fig.10 The measured phase unbalance between output ports

III. FABRICATION AND MEASUREMENT

After the overall design of the power divider, LTCC technology is used to fabricate this power divider to verify the effectiveness of design method. The fabricated sample and test fixture are shown in Fig.8. The size of the power divider is only $3.2\text{mm} \times 1.6\text{mm} \times 0.9\text{mm}$. Agilent 8719T Vector network analyzer is used to test the performance of the power divider which is shown in Fig.9 and Fig.10. Good agreement between simulated and measured results has been observed. From 3.1GHz to 3.5GHz, the insertion loss is less than 0.4dB, the return loss is better than 18dB and isolation between two output ports is better than 20dB, the phase unbalances between output ports is less than 2° .



Fig.8 The fabricated samples and test fixture of the power divider

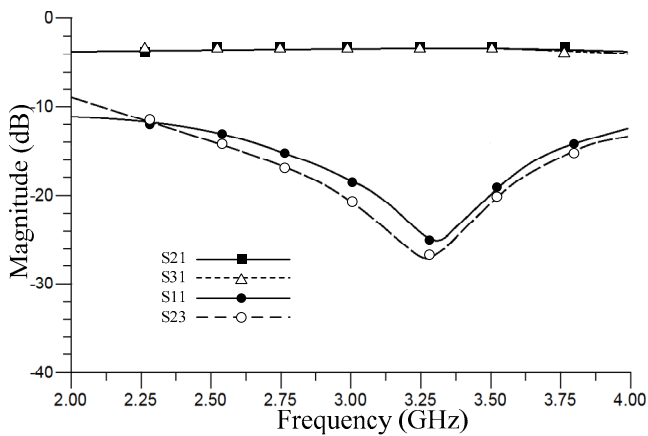


Fig.9 The measured performance of the power divider

IV. CONCLUSION

This paper presents a novel miniaturized Wilkinson power divider. By using lumped LC impedance transformer substitute for conventional quarter-wavelength transmission line and adopting LTCC technology, the size of the power divider is greatly reduced. The tested performance confirms well with simulated. It has the advantages of simple structure, easy fabrication, good compatibility. In general, it shows a broad application prospect in the microwave communication system.

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