Miniaturized Microstrip Wilkinson Power Divider with EBG Structure

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***Abstract*-A novel miniaturized microstrip Wilkinson power divider with capacitor loading is presented in this paper. The new divider not only effectively reduces the occupied area to 50% of the conventional one at 1.0 GHz, but also has good harmonic suppression performance. Furthermore, the new structure has only two variable parameters and can be easily designed. The design is validated both by simulation and measurement.**

I. INTRODUCTION

Power dividers are frequently used in microwave and millimeter-wave circuits. Research on dual-band and miniaturized power divider is of great interest in recent times. A conventional Wilkinson power divider is composed of two quarter-wavelength transmission-line (TLIN) sections at the designed frequency, which result in a large occupied area. Accordingly, many methods were proposed to minimize the divider's size, such as lumped element [1], defected ground structure (DGS) [2], microstrip electromagnetic bandgap (EBG) [3]-[4], and capacitor loading [5]-[7].

The EBG structure proposed in [4] can be seen as a middle capacitor loading structure, for the open-stub loading can be classified as capacitor loading when the electrical length of the stub is shorter than quarter wavelength. The Wilkinson power divider is a reciprocal 3-port network, and it can work both as power divider and power combiner. The higher harmonics suppression declared in [4] is for the power divider case, but not for the power combiner case. In [5], CLC type (both sides capacitor loading) power divider is studied and compared with LCL type (middle capacitor loading) power divider. And the problem of higher harmonics suppression for power combiner case can be solved using both sides capacitor loading. In this paper, a microstrip compact power divider with EBG structure is designed on the base of the work of [5]. It will be found that the new power divider proposed in this paper has simpler structure and can be easier designed than that of [5]. Furthermore, it occupied less area.

II. MINIATURIZED POWER DIVIDER

Fig. 1 shows the layout of a compact microstrip power divider with capacitor loading. The substrate is F4B with a relative dielectric constant of $\varepsilon_r = 2.65$ and a thickness of $h = 1.5\text{mm}$. The centre frequency is 1.0 GHz. The widths of the TLINs with characteristic impedances 50 ohm and 70.71ohm are 4.102mm and 2.308mm , respectively. Rectangular patch capacitors are loaded on high impedance line. The space between the stubs is 1.1 mm for mounting 100 ohm isolation resistance of 0805 size. The other spaces, the width of the high impedance line, the widths and the lengths of the interconnect stub shown in Fig. 1 are 0.4 mm for easy fabrication. There are only two variable parameters: the width W and the length L of the outer rectangular patch capacitors. The two variable parameters can be optimized with the aid of the Agilent's Advanced Design System (ADS) under conditions: $\text{dB}(S_{11})<-30\text{dB}$, $\text{dB}(S_{22})<-30\text{dB}$, and $\text{dB}(S_{32})<-30\text{dB}$ at the centre frequency. The optimized dimensions of the structure are $W = 2.12\text{mm}$ and $L = 11.73\text{mm}$.

The thin line is a high impedance TLIN, and therefore inductive. The patches are capacitively coupled to the ring. Thus, the structure appears to be equivalent to the capacitively loaded TLINs. So, the quarter-wavelength TLIN section at the designed frequency of a conventional divider is substituted by one cell of EBG structure.

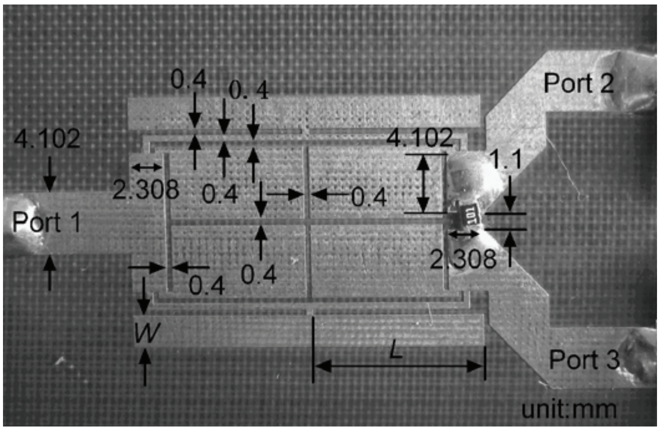

Figure 1. Layout of the miniaturized microstrip power divider.

Fig. 2 shows the size comparison of the compact and conventional dividers. It can be seen that the occupied areas of the new divider and the conventional one are 399mm^2 and 793mm^2, respectively, and it means that the proposed divider effectively reduces the occupied area to 50% of the conventional one. Our new divider also occupies less area than those given in [4] and [5], which are about 61% and 51.2% of the conventional divider.

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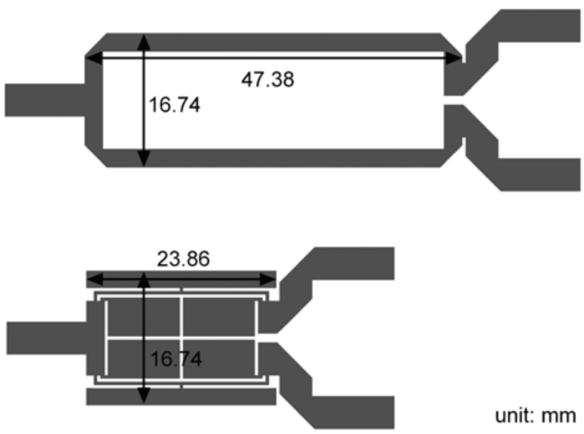

Figure 2. Size comparison of the proposed and conventional dividers.

III. Simulation and Measurement

The simulated S-parameters of the conventional divider are shown in Fig. 3. There is no harmonic suppression for conventional divider according to Fig. 3. The simulated and measured S-parameters of the new divider are shown in Figs. 4 and 5. It can be seen that the measured results are in good agreement with the simulated ones. It effectively rejects the harmonics over the bands of 3.2 - 4.2GHz and 4.4 - 5GHz to a level lower than -10dB either it works as a power divider or it works as a power combiner, according to the S_{11}, S_{22}, S_{32}, and S_{21} in Fig. 5. The insertion loss is 3.3dB at 0.975GHz. The return losses and the isolation are better than -20dB in the operation frequency range from 0.81 to 1.14 GHz, and the appropriate frequency bandwidth is 33% of the centre frequency of 0.975GHz according to the S_{11}, S_{22}, and S_{32} in Fig. 5. The simulated and measured phase is shown in Fig. 6, the phase delay of SMA connector can explain the difference between the simulated phase and measured phase.

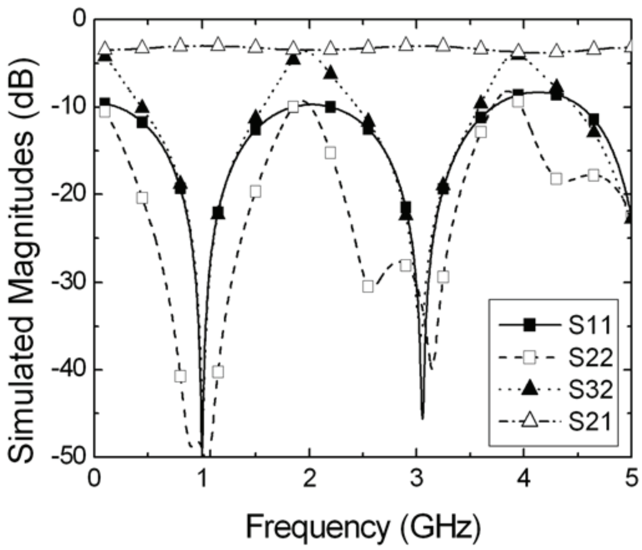

Figure 3. Simulated magnitudes of the conventional divider.

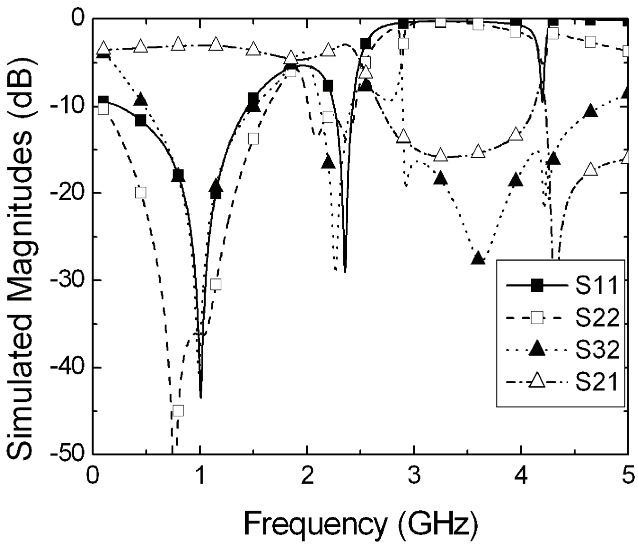

Figure 4. Simulated magnitudes of the proposed divider.

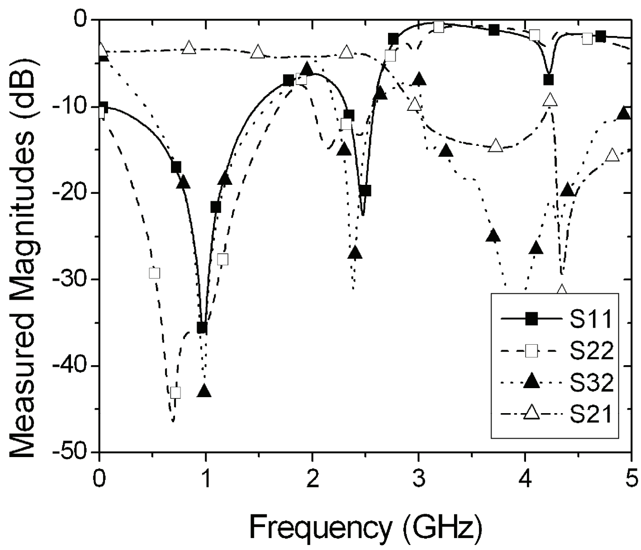

Figure 5. Measured magnitudes of the proposed divider.

IV. Conclusion

A novel miniaturized microstrip power divider with capacitor loading is presented in this paper. The new divider can effectively reduce the occupied area and has good harmonic suppression performance over a wide band. The new divider is simple and can be easily designed.

Acknowledgment

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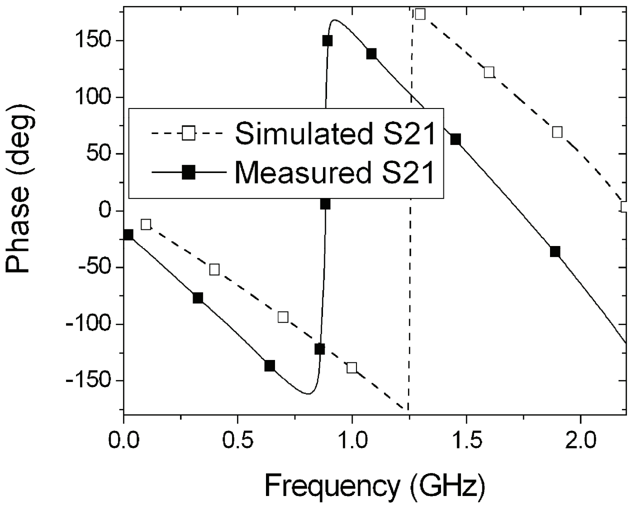

Figure 6. Simulated and measured phase of the proposed divider.

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