Novel Ultra-Wideband (UWB) Multilayer Slotline Power Divider With Bandpass Response

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***Abstract*—A novel ultra-wideband (UWB) multilayer slotline power divider with bandpass filtering response is presented. In the proposed structure, a single isolation resistor is properly placed between the two output ports. Based on the transmission-line equivalent-circuit method, the design equations of the proposed UWB power divider has been derived with the even and odd mode analyses. Experimental results show that excellent impedance matching at all three ports, amplitude and phase balance at the two output ports, isolation between the two output ports, and out-of-band rejection are observed at the UWB band.**

***Index Terms*—Power divider, ultra-wideband (UWB), slotline, multilayer, bandpass response.**

I. Introduction

SINCE the ultra-wideband (UWB: 3.1–10.6 GHz) spectrum was regulated for unlicensed use in 2002, many UWB devices and circuits have been presented and investigated extensively [1]–[8]. The UWB power divider is one of the key passive components in UWB systems. A few UWB power dividers with different geometries and design methodologies have been developed [5]–[8]. In [8], a Wilkinson power divider with symmetric defected ground structure having frequency band-notch characteristic was proposed. Based on the multilayer broadside-coupled structure, a three-way power divider with UWB performance is presented in [6]. According to [7], a compact UWB out-of-phase uniplanar power divider is presented, which shows low insertion loss and good return loss performance. Recently, a UWB microstrip power divider using a pair of stepped-impedance open-circuited stubs and parallel coupled lines in two output ports was developed with the sharp roll-off skirt [5].

In this letter, a novel UWB in-phase power divider with bandpass filtering response is presented and analyzed. This power divider is constructed by introducing multilayer microstrip line-slotline coupling structure, which cannot only divide/combine the power of microwave signals, but also reject unwanted frequency signals to better regulate the UWB performance. In addition, only a single resistor needs to be placed between the two output ports for isolation. The simulated and measured results of the fabricated UWB power divider have shown that the proposed UWB power divider has good impedance matching, excellent amplitude and phase balance, and perfect isolation over the UWB band.

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II. Design of the Proposed UWB Power Divider

The configuration of the proposed UWB multilayer power divider is shown in Fig. 1. The input port (port 1) is located on the top layer of the structure, whereas the output ports are at the top layer (port 3) and bottom layer (port 2). The ground plane, which also includes the one-wavelength long slotline resonator, is at the mid layer of the structure. The one-wavelength slotline resonator can generate the first three resonant frequencies placed evenly within the desired UWB passband [4]. This divider employs the microstrip line to slotline transition, which is composed of the open-circuited microstrip line with a length of $l_{m1} \approx l_{m2} \approx \lambda_m/4$ (λ_m is the guided wavelength of microstrip line at the center frequency of 6.85 GHz) and the short-circuited slotline with a length of $l_s \approx \lambda_s/4$ (λ_s is the guided wavelength of slotline at the center frequency of 6.85 GHz). Further, a hole from the top layer to the bottom layer is drilled, which is used to contain an isolation resistor of R to prevent signal transmission between ports 2 and 3.

The field matching between a microstrip mode and a slotline mode can be achieved by the virtual short caused by an open-circuited microstrip line with one quarter-wavelength. The narrow slotline at the ground plane (mid layer) acts as a guide to couple a microwave signal from the input microstrip port to the two output microstrip ports. The arrangement shown in Fig. 1 aims at equal signal division (3 dB) between two output ports with same phase. The even- and odd-mode analysis method can be applied to this UWB power divider.

The equivalent-circuit model of the proposed UWB multilayer slotline power divider is shown in Fig. 2. Fig. 2(a) shows the even-mode circuit model for a bisection of the UWB divider, which is a two-port network. Since two signals with the same magnitude and phase are applied to each output port, no current flows through the isolation resistor. Hence, the circuit element, R, can be omitted. The characteristic impedances at port 1 and the slotline are double Z_0 and Z_s, respectively. Thus, the input impedance at port 1 and port 2 can be given by

$$Z^e_{\text{in}1} = -j2Z_0 \cot\theta_{m1} + \frac{2Z_s \tan\theta_s \left(Z^e_{s1} + j2Z_s \tan\theta_l\right)}{Z^e_{s1}(1-\tan\theta_s \tan\theta_l) + j2Z_s(\tan\theta_s + \tan\theta_l)} \tag{1}$$

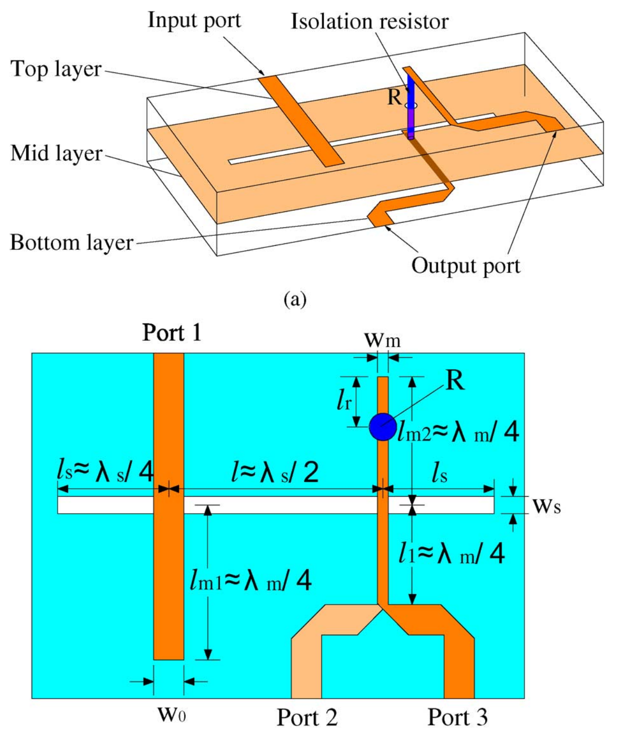


Fig. 1. Configuration of the proposed UWB multilayer slotline power divider. (a) 3-D view (b) top view.

$$Z_{\text{in2}}^e = Z_1\frac{Z_t^e + jZ_1\tan\theta_1}{Z_1 + jZ_t^e\tan\theta_1} \tag{2}$$

where

$$Z_{s1}^e = \frac{\frac{2Z_s\tan\theta_s(jZ_0 - Z_1\tan\theta_1)}{Z_1 + jZ_0\tan\theta_1} - 2Z_s\tan\theta_s\cot\theta_{m2}}{\frac{Z_0 + jZ_1\tan\theta_1}{Z_1 + jZ_0\tan\theta_1} + j2\tan\theta_s\frac{Z_s}{Z_1} + j\cot\theta_{m2}}$$

$$Z_t^e = \frac{2Z_s\tan\theta_s\,(Z_{s2}^e + j2Z_s\tan\theta_l)}{Z_{s2}^e(1 - \tan\theta_s\tan\theta_l) + j2Z_s(\tan\theta_s + \tan\theta_l)} - jZ_1\cot\theta_{m2}$$

$$Z_{s2}^e = \frac{2Z_0Z_s\tan\theta_s(j - \cot\theta_{m1})}{Z_0(1 + j\cot\theta_{m1}) + jZ_s\tan\theta_s}.$$

When $Z_{\text{in1}}^e = 2Z_0$ and $Z_{\text{in2}}^e = Z_0$, good impedance matching can be obtained. In this case, if $\theta_1 = \theta_s = \theta_{m1} = \theta_{m2} = \pi/2$ and $\theta_l = \pi$, the following expression can be derived by

$$Z_1 = \sqrt{2}Z_0 \tag{3}$$

Equation (3) provides a simple guideline in selection of Z_1. Under the odd-mode excitation, a bisection of the divider is expressed as a one-port network shown in Fig. 2(b). In this case, port 1 can be simply considered as a short circuit. The input impedance at port 2 is expressed by

$$Z_{\text{in}}^o = Z_1\frac{Z_t^o + jZ_1\tan\theta_1 + \frac{j2Z_sZ_s^o\tan\theta_s}{Z_s^o + j2Z_s\tan\theta_s}}{Z_1 + j\tan\theta_1\left(Z_t^o + \frac{j2Z_sZ_s^o\tan\theta_s}{Z_s^o + j2Z_s\tan\theta_s}\right)} \tag{4}$$

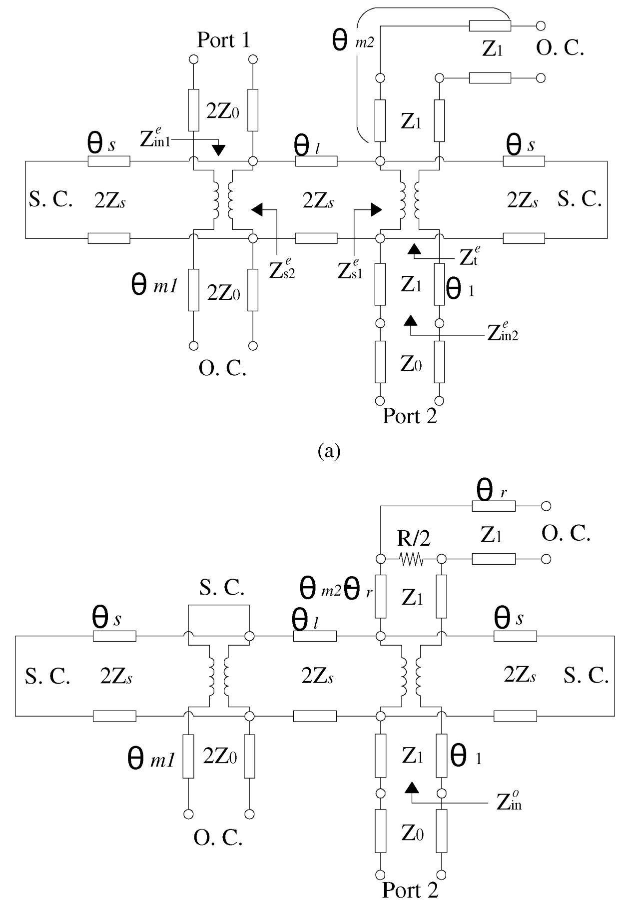


Fig. 2. Equivalent circuit of the proposed UWB slotline power divider (a) Even-mode circuit model (b) Odd-mode circuit model.

where

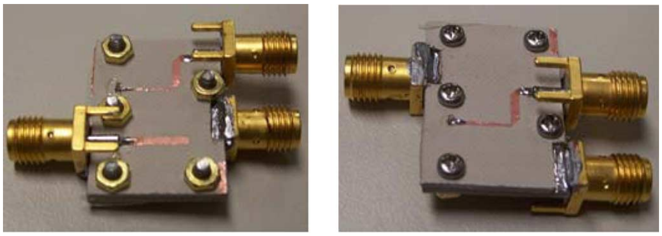
$$Z_t^o = \frac{2Z_1^2\cot\theta_r\tan(\theta_{m2} - \theta_r)}{R + R\cot\theta_r\tan(\theta_{m2} - \theta_r) + j2Z_1\cot\theta_r} + \frac{jZ_1R[\tan(\theta_{m2} - \theta_r) - \cot\theta_r]}{R + R\cot\theta_r\tan(\theta_{m2} - \theta_r) + j2Z_1\cot\theta_r}$$

$$Z_s^o = 2Z_s\frac{jZ_s\tan\theta_s\tan\theta_l - jZ_0\cot\theta_{m1}(\tan\theta_s + \tan\theta_l)}{Z_s\tan\theta_s - Z_0\cot\theta_{m1} + Z_0\tan\theta_s\tan\theta_l\cot\theta_{m1}}.$$

If $Z_{\text{in}}^o = Z_0, \theta_1 = \theta_s = \theta_{m1} = \theta_{m2} = \pi/2, \theta_r = 0$, and $\theta_l = \pi$, then (4) can be reduced as follows:

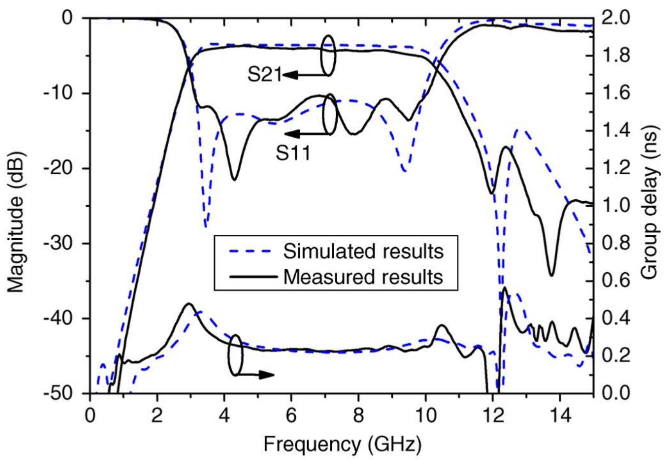
$$R = 2Z_0. \tag{5}$$

The impedance matching (S_{11} and S_{22}) and stopband performances can be analyzed and optimized according to (1), (2), and (4), while the bandwidth can be adjusted when the widths of the microstrip line and slotline are varied. The amplitude and phase balance are decided by the dimensions and locations of the output microstrip line to slotline transitions, and the isolation between the output ports can be determined by (5) and θ_r. Then, the proposed power divider can be optimized using the EM-simulator.

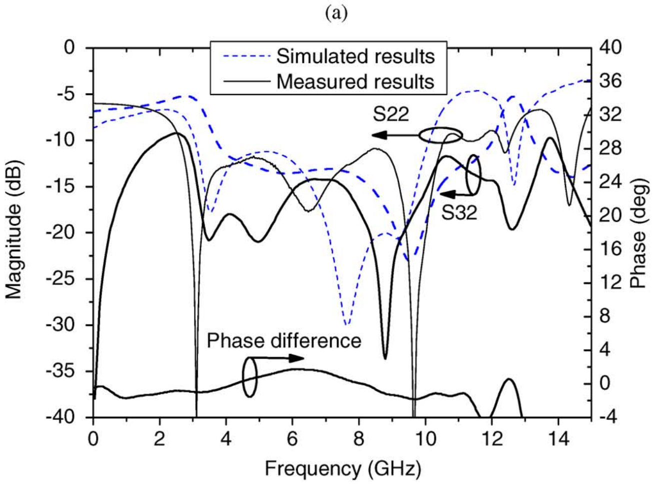


(a) (b)

Fig. 3. Photograph of the proposed UWB multilayer slotline power divider (a) top view and (b) bottom view.



(a)



(b)

Fig. 4. Simulated and measured results of the proposed UWB multilayer slotline power divider (a) input return loss, insertion loss, and group delay (b) output return loss, isolation, and phase difference.

III. Experimental Results

The proposed UWB multilayer slotline power divider is designed and fabricated on substrate with dielectric constant ε_r of 6.03, thickness of 0.82 mm, and loss tangent of 0.0028. Fig. 3 shows the fabricated divider. The final optimized sizes and parameters of the UWB power divider are: $l = 7.8$ mm, $l_s = 4.05$ mm, $l_1 = 3.6$ mm, $l_{m1} = 5.6$ mm, $l_{m2} = 3.4$ mm, $l_r = 0, \mathrm{w}_0 = 1.1$ mm, $\mathrm{w_s} = 0.45$ mm, $\mathrm{w_m} = 0.4$ mm, and $\mathrm{R} = 100\ \Omega$.

Fig. 4 shows the measured and simulated results at the frequency range 0–15 GHz. They matched with each other. The measured return loss is greater than 10 dB from 3.1 to 10 GHz, while the measured insertion loss is around 3 dB over the entire UWB band. The insertion loss (the 3 dB power division loss is not included) is less than 1 dB from 3.4 GHz to 7 GHz, and less than 2 dB from 7 GHz to 10 GHz. In particular, the out-of-band rejection level is more than 17 dB at the lower stopbands (from 0 to 2.3 GHz) and the upper stopbands (from 11.5 to more than 15 GHz). The simulated and measured group delays show good linearity within the UWB passband. The measured group delay is 0.22 ns at 6.85 GHz within a variation of about 0.2 ns from 3.1 GHz to more than 11.5 GHz. Fig. 4(b) shows the isolation and phase difference between the port 2 and port 3, as well as the output return loss. The measured output return loss $|S_{22}|$ and $|S_{32}|$ between the port 2 and port 3 are all greater than 10 dB over the UWB band. In addition, the phase difference of $\pm 2^\circ$ between the output ports is observed in the entire UWB band.

IV. Conclusion

A UWB slotline power divider using multilayer structure is investigated. The design method and performance of the proposed UWB power divider have been studied using the even and odd mode analysis. To verify the attractive features of this proposed UWB power divider, one prototype divider is designed and measured. Good in-band power splitting, impedance matching, isolation, amplitude and phase balance, and out-of-band rejection are obtained both in simulations and measurements.

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