Pseudo-Doppler Audio Direction Finder

Project Report

6.101 Analog Electronics Laboratory - MIT - Spring 2016
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Introduction

This report describes the design process for a pseudo-Doppler audio direction finder. The completed system can determine and display the direction of arrival of sound received by a microphone array. It emulates the performance of radio direction finders based on the same pseudo-Doppler principle.

Radio direction finder (RDF) systems have historically been used for aerial navigation and were a critical technological capability during the First and Second World Wars. Today, RDFs are used in such applications as stolen vehicle localization and pirate radio detection.

Early RDF systems used mechanically rotated antennas to compare signals in different directions. As the underlying devices and electronic technology improved, the methods employed by RDFs became increasingly sophisticated. One such method is pseudo-Doppler direction finding, whereby each antenna in an array is sampled in sequence so as to simulate a rotating effective antenna. As the effective antenna is steered toward and away from the radio source, a Doppler shift is introduced. The resulting FM signal has directional information encoded in the phase of the modulating waveform. This project applies the same pseudo-Doppler direction finding technique at audio frequencies for sound localization.

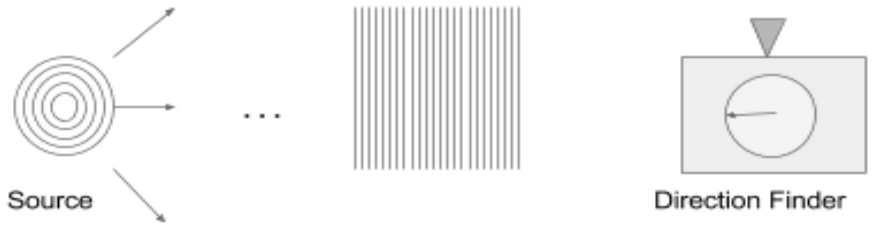


Figure 0: Direction Finder. Very high level description

Note on the Change of Project Scope

Originally, we set out to create a true radio direction finder (RDF) operating in the FM band. In the first week we prototyped a superregenerative FM receiver on perfboard. Difficulties with debugging the receiver motivated our decision to attempt sound localization instead. The change of scope eliminated many problems that could have jeopardized project success. While substantially simpler to design, the audio direction finder retains the same pseudo-Doppler principle of operation as the RDF that we initially set out to construct.

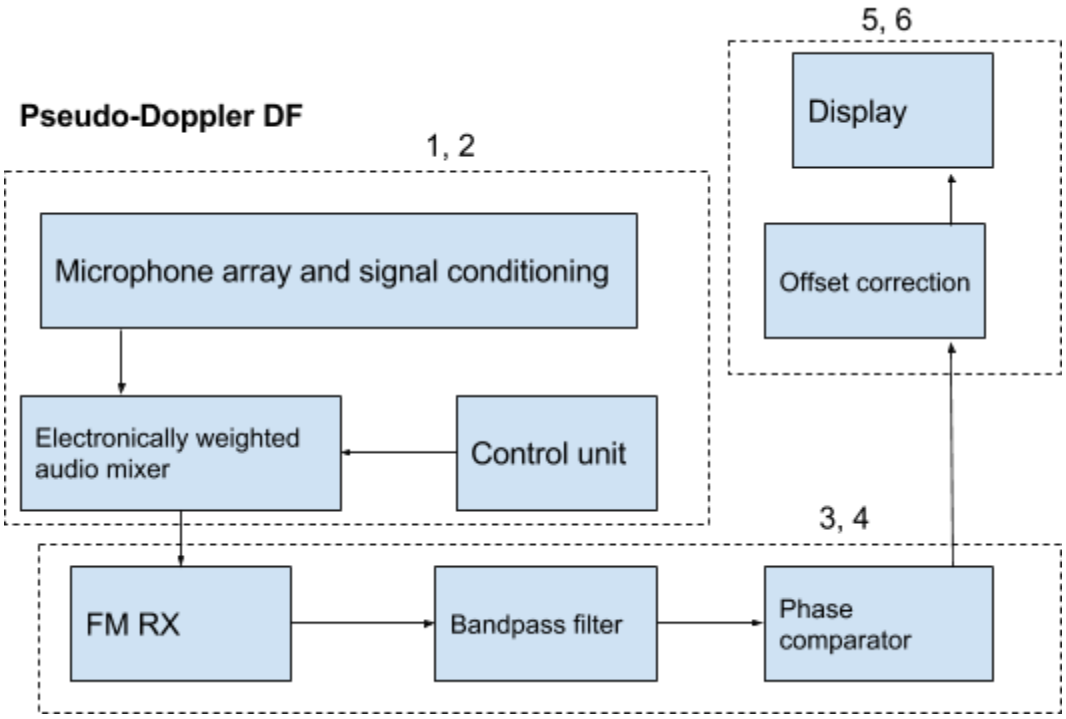


Figure 1: Main Block Diagram. Consists of three modules: Signal Acquisition (1, 2); Phase Extraction (3, 4); Display (5, 6).

High Level Block Diagram and Operation

The basic operation of a pseudo-Doppler direction finder is as follows:

1. A narrowband signal, in our case acoustic, is received by an array of sensors arranged in some known geometry, typically a circle or square. The signals received at the sensors are phase-shifted according to the array geometry and direction of arrival.
2. A control unit actively switches between the different sensor outputs in a cyclic fashion. This can be interpreted as moving a single sensor around the array geometry. As the active sensor moves toward the signal source, an increase in the received frequency is observed. Likewise, a downshift in frequency is observed as the active antenna moves away from the source. In effect, the antenna switching procedure frequency modulates the source signal. The phase of the modulating waveform contains directional information.
3. The synthesized FM signal is fed into an FM detector, which extracts the modulating waveform. The modulating waveform is the same frequency as the switching signal from the control unit.
4. A phase comparator detects the phase difference between the modulating waveform and the control unit switching signal. This can be accomplished in analog using a mixer and lowpass filter. The resulting signal is proportional to the cosine of the phase difference.
5. An offset correction block adjusts for bias in the phase detector and maps the estimated phase to a direction of arrival.
6. The estimated direction of arrival is indicated on a display

MATLAB Proof-Of-Concept Simulation

A MATLAB simulation was created in order to verify performance of the pseudo-Doppler direction finding system. Background noise, array imprecisions, and VCA gain distortion are all included in the simulation. The simulation performs surprisingly well under adverse conditions. The figure below shows several plots generated by the simulation.

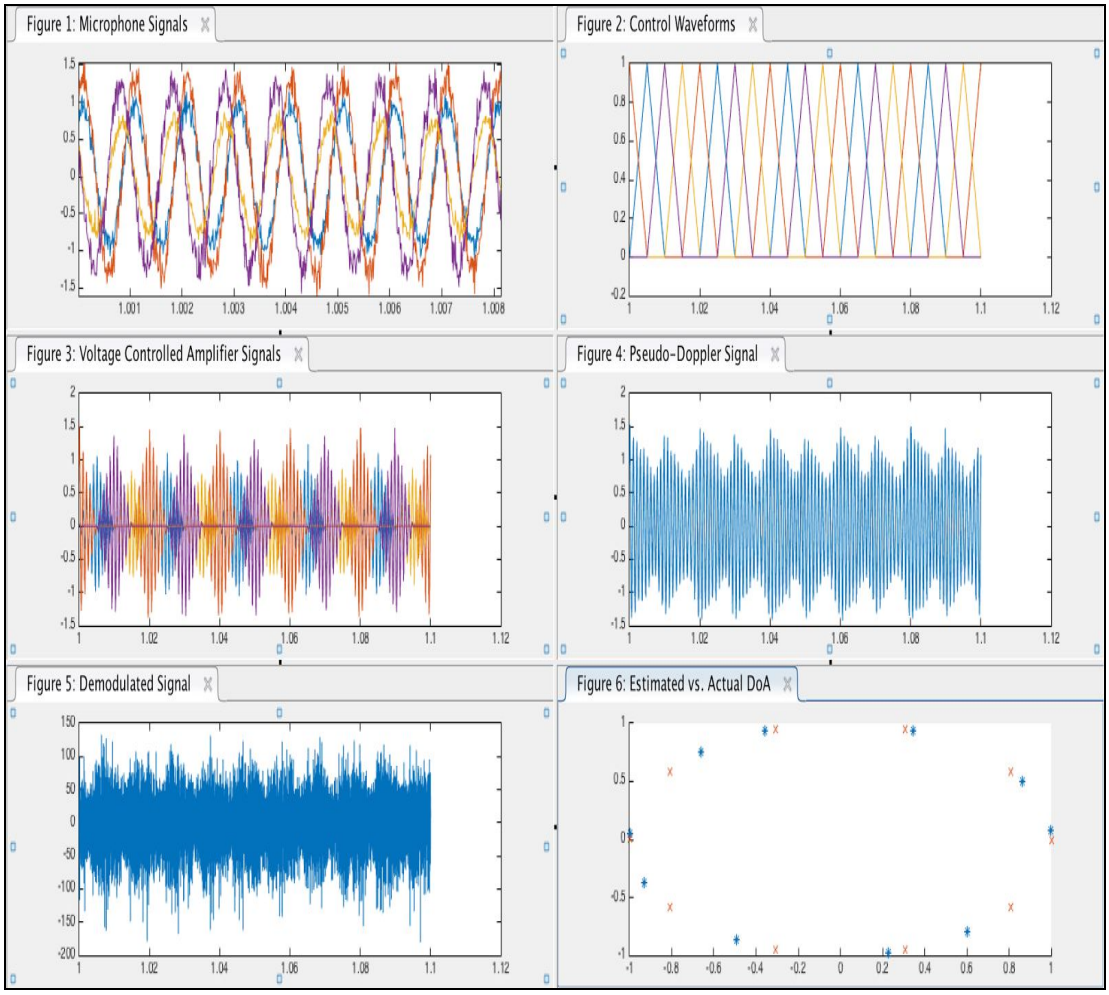


Figure 2: MATLAB Simulation. Simulated direction finder operation and performance.

Signal Acquisition Module (Jimmy)

Overview

The signal acquisition module performs functions associated with reception and processing of the microphone signals. It is solely responsible for controlling the microphone array and synthesizing the pseudo-Doppler FM signal. Its inputs are the acoustic signals from the microphone array and the control reference sinusoid from the phase detection module. Its output is the pseudo-Doppler FM signal to be processed by the phase detection module.

The signal acquisition module can be further decomposed into three functional blocks: microphone signal conditioner, control unit, and audio mixer (summer). An sensor array consists of four microphones arranged so as to form a square of side length λ/4, where λ is the wavelength of the source tone. Each microphone in the array requires a signal conditioner in order to appropriately amplify, filter, and compress its signal. A preamp stage brings the weak signal from the microphone up to an acceptable level. The signal is filtered at this stage in order to remove noise outside of the target band. A compressor circuit equalizes the signal levels out of different microphones so as to prevent distortion in subsequent stages. A final gain stage boosts the signal level further. Each conditioned microphone signal is fed through a voltage controlled amplifier (VCA) before entering the audio summer. The gain of each VCA is set by a signal from the control unit. These gain control signals are designed to soft-switch between microphones in the array. Following the VCA stage, the variably gained microphone signals are fed into the audio summer, which synthesizes the pseudo-Doppler FM signal.

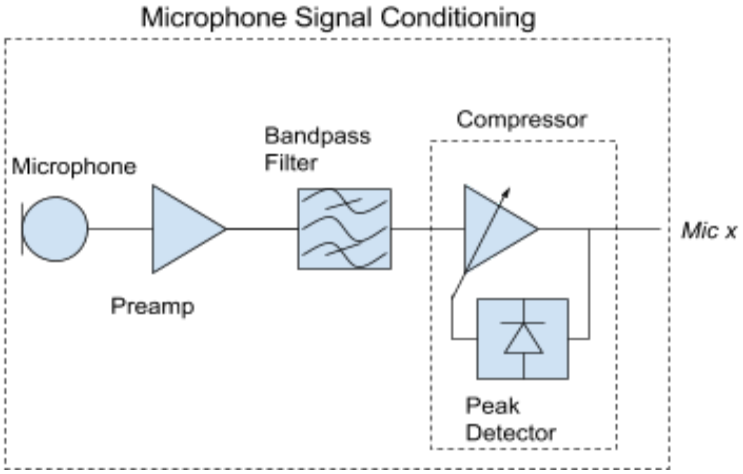


Figure 3: Microphone Signal Conditioning. Each microphone signal is fed through a preamp, bandpass filter, and compressor

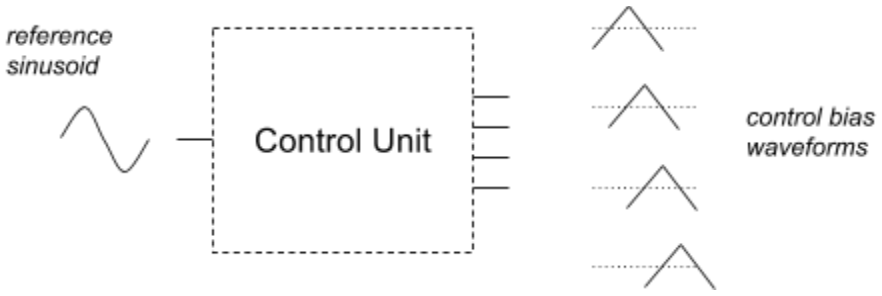


Figure 4: Control Unit. The Control Unit uses the reference signal to generate phase-shifted control signals for each microphone channel.

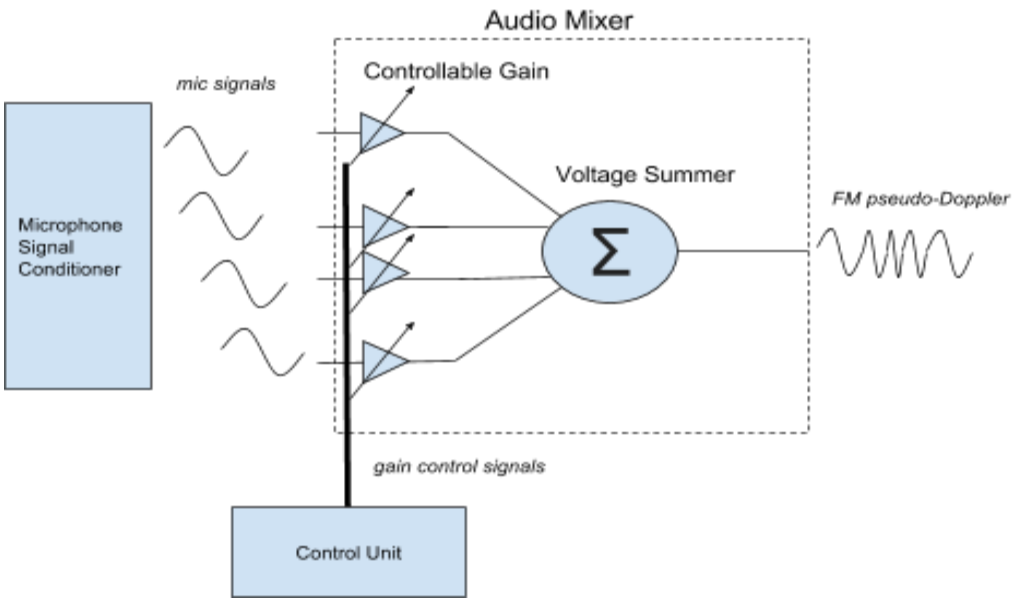


Figure 5: Audio Mixer. The Audio Mixer sums weighted versions of the microphone signals in order to produce the pseudo-Doppler FM signal.

Design Specifications

In order to constrain the design space, the following constraints/specifications were applied:

- Operates off of the +/-15V lab bench power supply rails.
- Tuned to a 1kHz source tone ($\lambda/4$ = 8.5cm)
- Control switching signal of 50Hz

Signal Conditioning

Omnidirectional electret condenser microphones with JFET output were chosen for the array. Correct operation of these microphones requires a biasing network (R1, R2) and blocking capacitor (C1) for extracting the small microphone signal. Care must be taken to ensure that the voltage across the microphone does not exceed the supply limit of 10V and that the output impedance provided by the network is no greater than 2200Ω.

The preamp is designed to provide high gain at the chosen tone frequency. It is implemented using a Sallen-Key bandpass filter topology. R3, R4, R5, C2, and C5 are selected to provide a center frequency of approximately 1 kHz. R6 and R7 are selected to provide as much gain as possible without producing instability.

The compressor circuit uses a PFET (Q1) operated in its linear regime as voltage controlled resistor. Q1 in conjunction with R8 provide variable attenuation to microphone signal. C8 and R9 are chosen so as to prevent the compressor from responding to signals below a corner frequency of 16Hz. C10, C11, R12, and R13 determine the frequency dependence of the feedback gain for U1B. C10 is a DC blocking capacitor that sets the DC gain to unity. C11 is an AC shunt capacitor that sets a cutoff frequency of 2.34kHz, above which the gain is approximately unity. This prevents high frequency noise from being amplified and injected into the amplitude detector. The automatic gain control dynamics are characterized by two time constants: an attacking time constant, which determines how quickly the compressor responds to amplitude spikes and is set by R10 and C9; and a recovery time constant, which is set by R11 and C9. R11 should be chosen to be at least 10× R10. The device characteristics of transistors Q1 and Q2 are subject to much process variation, so the amplitude threshold for the AGC will likewise vary between devices. It is important to test the compressor with a collection of transistors and select those that yield similar gain control behavior.

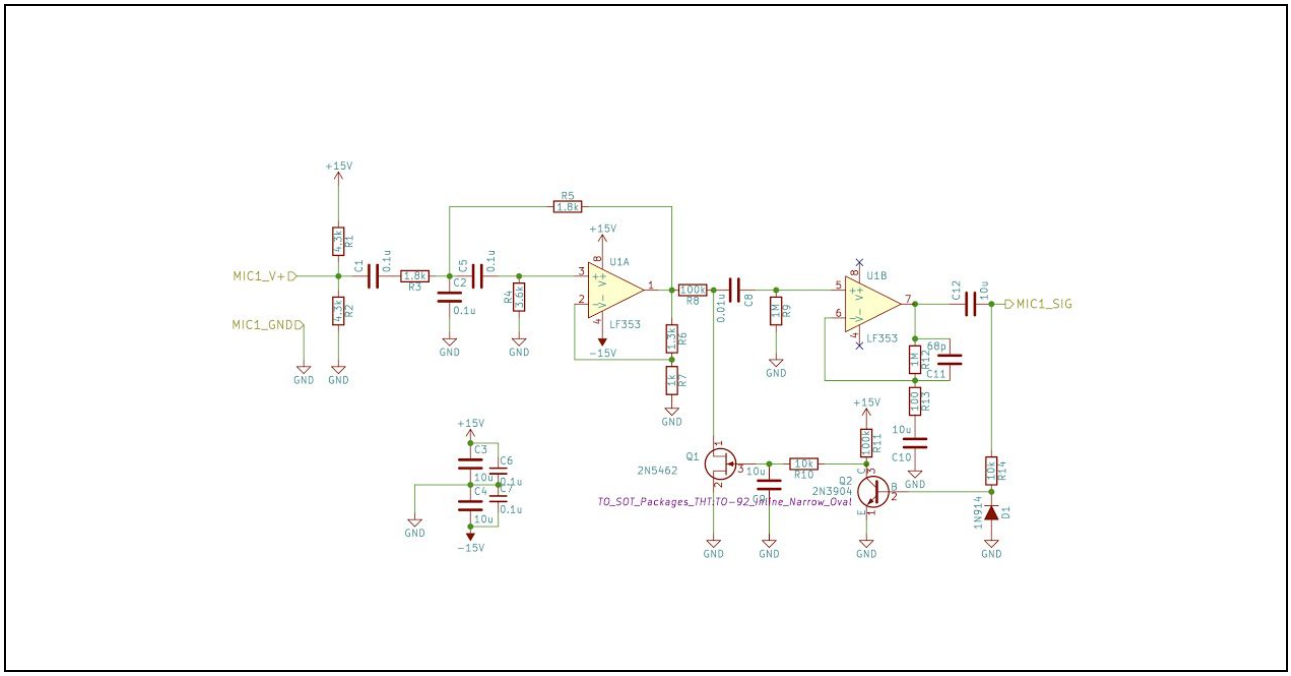


Figure 6: Signal Conditioning Schematic. Schematic diagram including part numbers, component values, and references for the preamp, bandpass filter, and compressor stages.

Voltage Controlled Amplifier and Audio Summer

Synthesizing the pseudo-Doppler FM signal involves applying electronically controlled gain to the microphone signals. A voltage controlled amplifier (VCA) circuit is used to achieve this

result. The chosen implementation has the advantages of low part count and simplicity. As in the compressor circuit, a 2N5462 PFET (Q3) operated in its linear regime is used as a voltage controlled resistor. Its output resistance and gate-source bias are approximately linearly related for small drain-source voltages. To ensure linear operation, it is necessary to first attenuate the microphone signal using R15 and R16. Device variation again requires that testing and careful selection of transistors be performed in order to produce consistent results. A 100kΩ trim potentiometer is included in parallel with R16. This potentiometer should be tuned in order to make the outputs for each VCA have around the same maximum amplitude. The capacitor C13 has a linearizing effect on the output. The resistor R18 was added to slightly bias Q3 off.

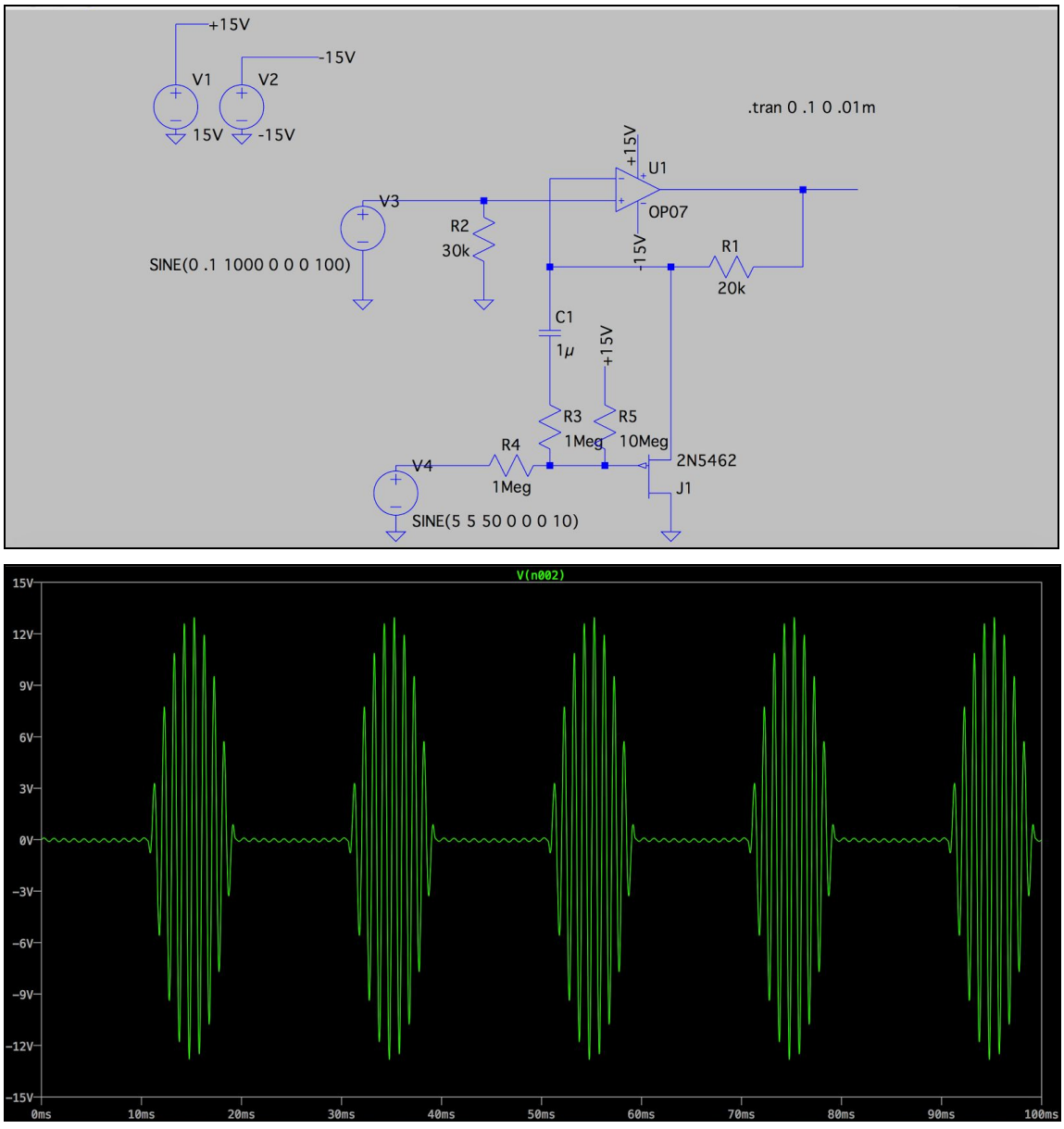


Figure 7: VCA LTSpice Simulation. Voltage controlled amplifier simulated for a small input signal and large gain control signal.

After being fed through the VCAs, the microphone signals enter the audio summer. The summer is implemented using a simple op-amp inverting summer topology. Resistors R1, R2, R3, and R4 are chosen to be identical. The feedback resistor R6 is made small enough so as to prevent railing of the output.

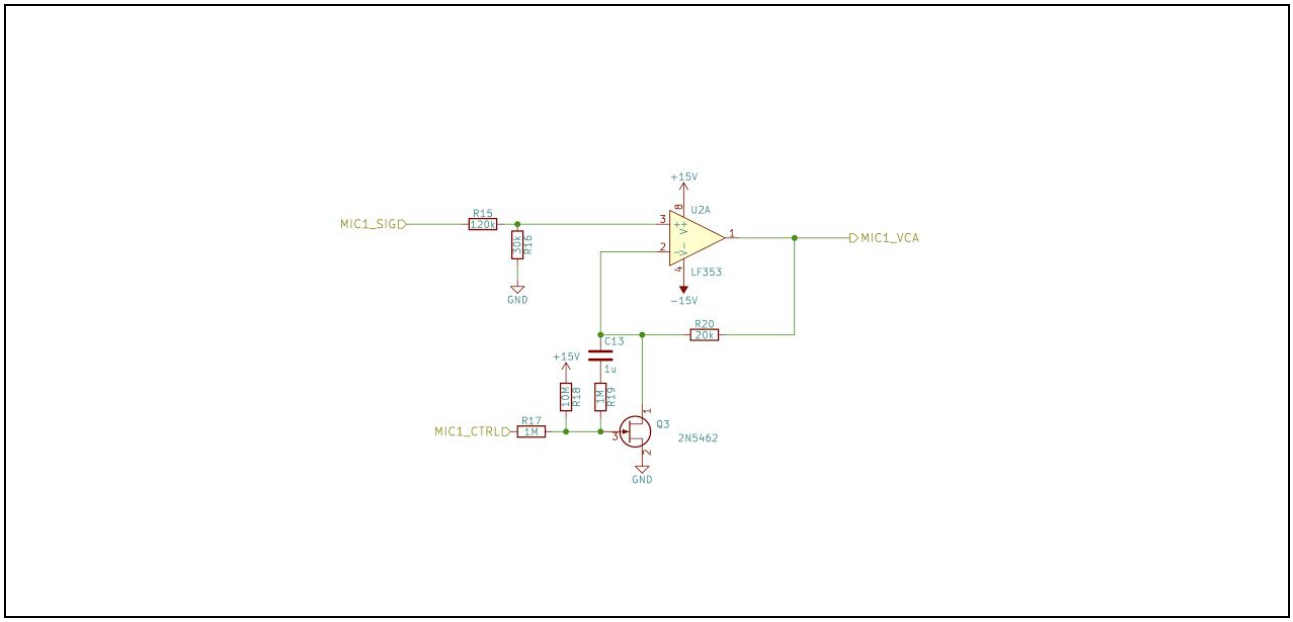


Figure 8: VCA Schematic. Schematic diagram including part numbers, component values, and references for a single voltage controlled amplifier.

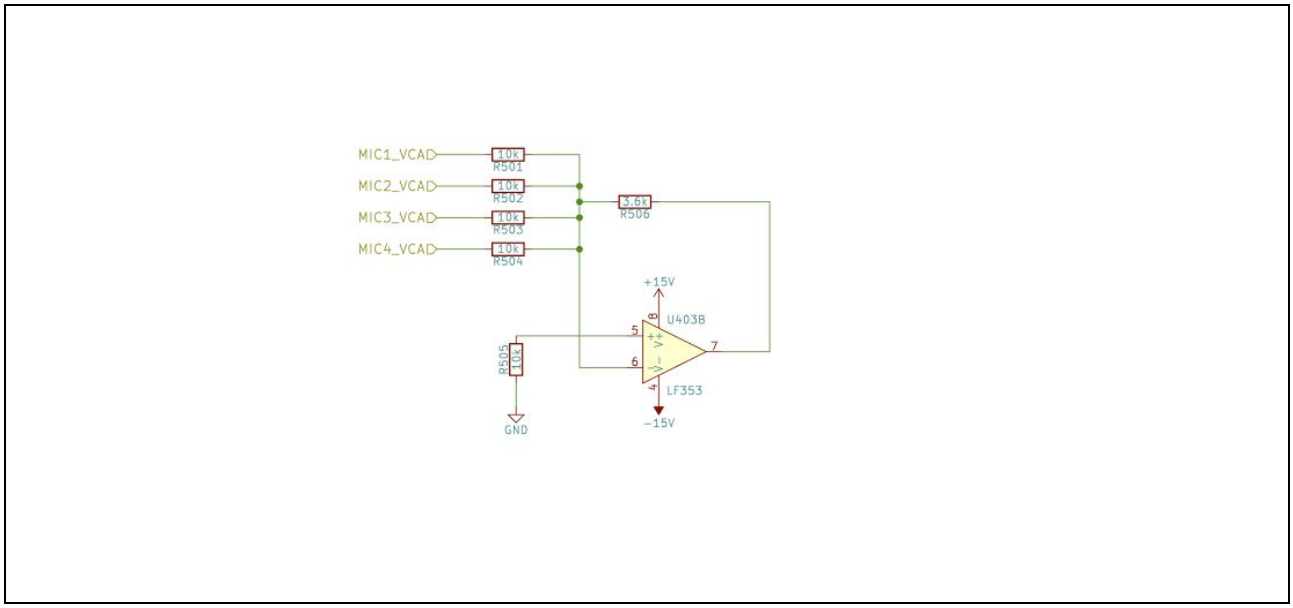


Figure 9: Audio Summer Schematic. Schematic diagram including part numbers, component values, and references for the audio summer.

Control Unit

The control unit generates signals for controlling the VCAs. The control signals are designed to have a triangular profile that soft-switches between microphone lines. At the heart of the control unit is a Wien bridge quadrature oscillator. C401, C402, R402, and R403 set the oscillation frequency. C401 is identical to C402 and likewise for the pair R402 and R403. R401 is chosen to be very slightly less than R402/R403 so as to sustain oscillations without significantly distorting the waveform. It is implemented as a resistor identical to R402/R403 with a 100kΩ trim potentiometer placed in parallel. The potentiometer should be tuned until the approximately triangular waveforms just begin to rail (see Figure 9).

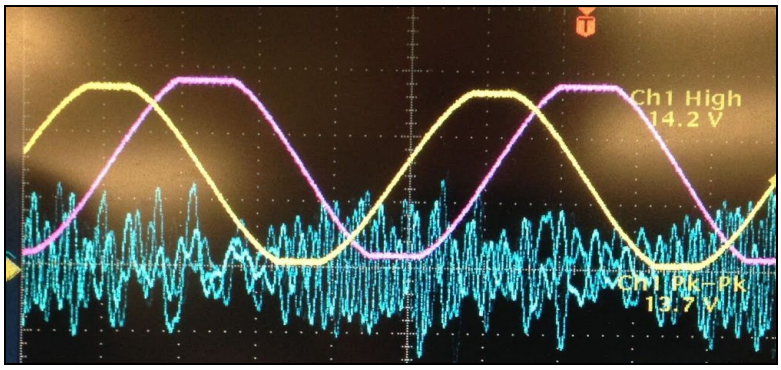


Figure 10: Quadrature Signals. Yellow and purple oscilloscope traces show the 0° and 90° control signals generated by the Wien bridge oscillator. The blue trace is the pseudo-Doppler signal.

Two unity gain inverting op-amps are used to invert and buffer the 0° and 90° control signals. These control the gain applied to the first and second microphone signals by their respective VCAs. Two more unity gain inverting op-amps give the 180° and 270° phase shifted control signals for the third and fourth microphones.

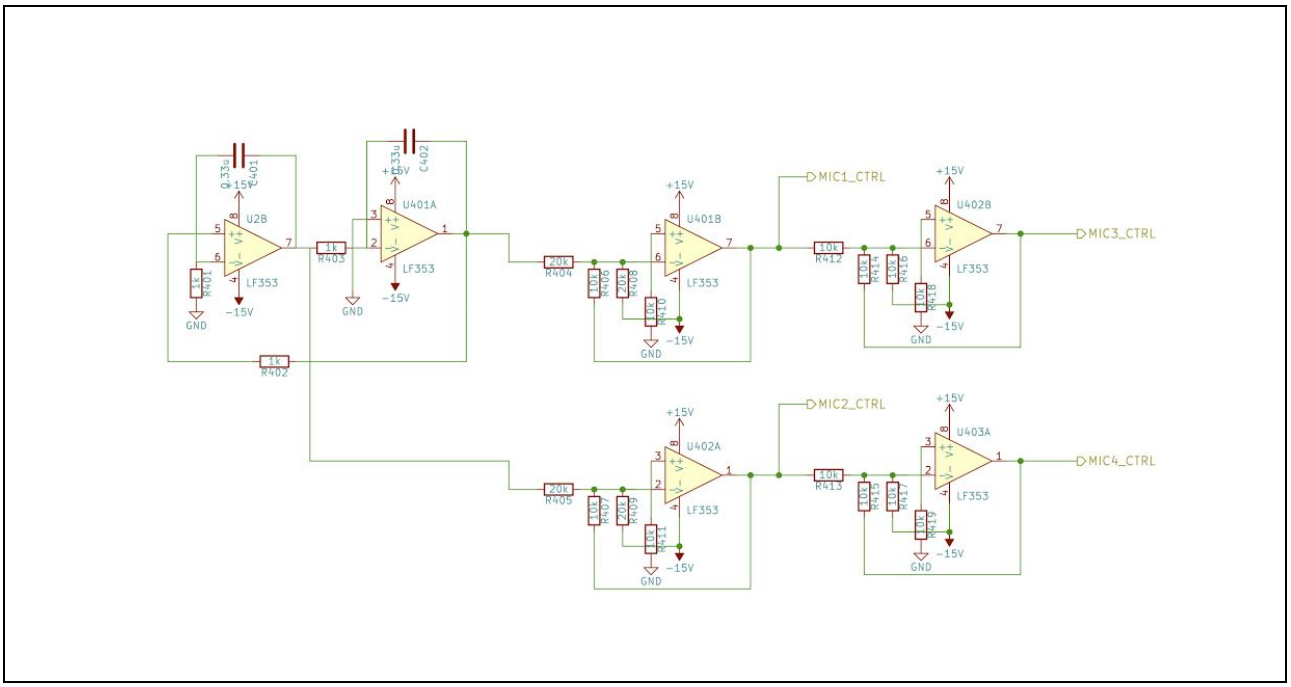


Figure 11: Control Unit Schematic. Schematic diagram including part numbers, component values, and references for the control unit.

PCB

A PCB was made for the signal conditioning and VCA circuits. Deadlines prompted shipping of the design without the control unit or audio summer circuitry. However, the board alone is general enough to be useful for a variety of audio applications. Layout was done using KiCad on a two-layer board. Ground planes with ample via stitching on both layers were included in hopes of keeping noise injection low. The design was sent to the manufacturing service at http://smart-prototyping.com/. A 3D rendering of the layout is shown below along with a fully populated and functioning physical board.

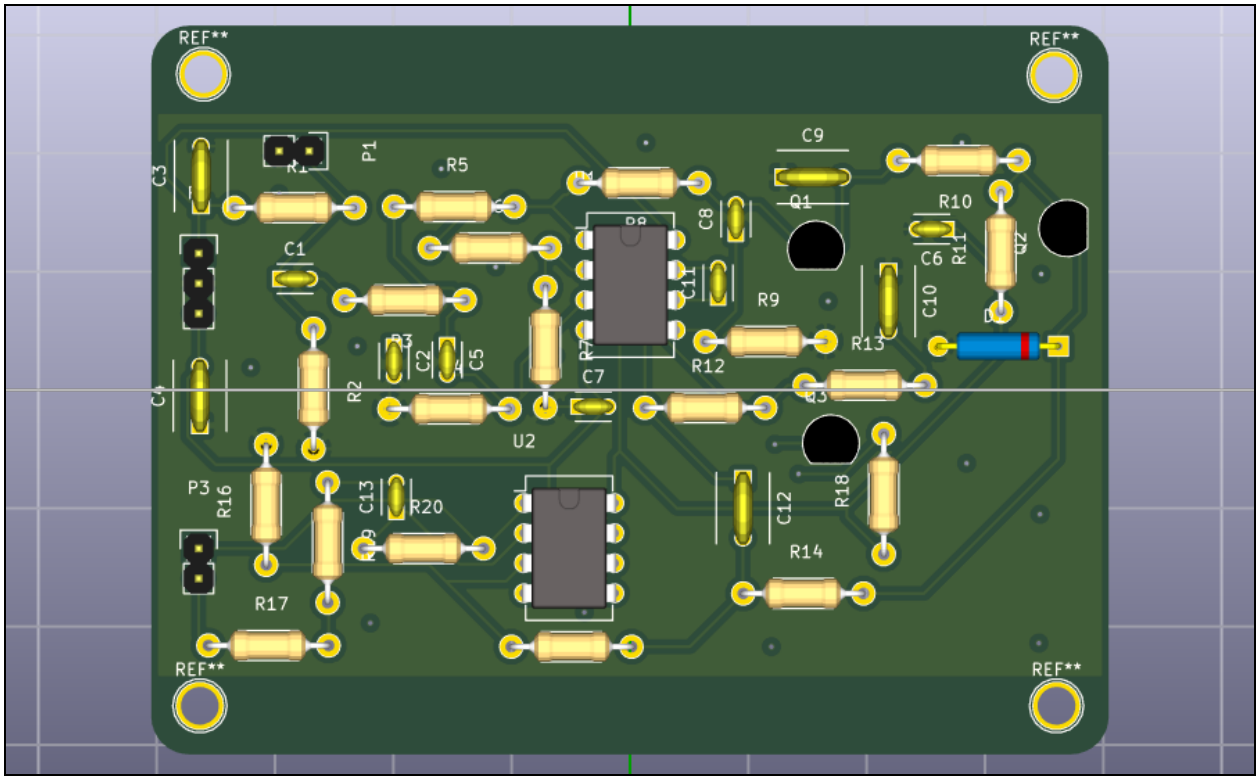


Figure 12: KiCad PCB Rendering. 3D Rendering of board design in KiCad

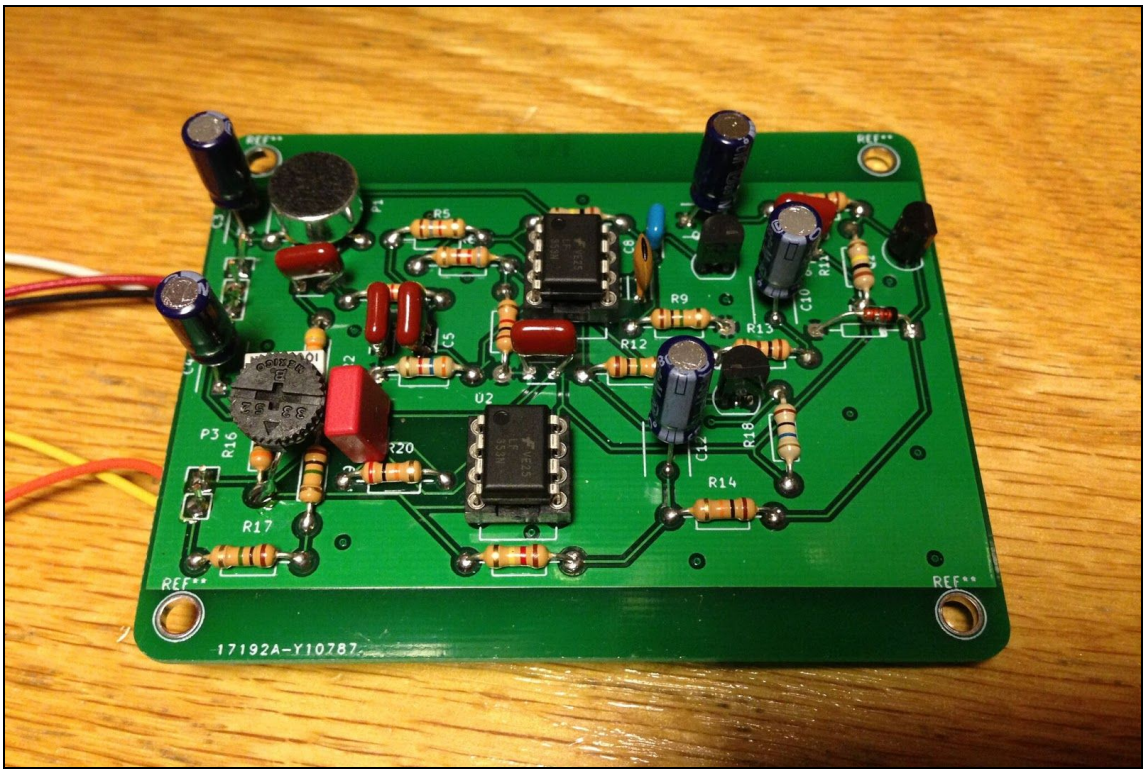


Figure 13: Working PCB. Fully populated and functioning PCB including signal conditioning and VCA circuits

Phase Acquisition (Amanda)

FM Demodulation

To demodulate the FM signal from the audio mixer, I chose to use a phase lock loop (PLL). I first take the FM signal from the audio mixer stage and turn it into a square wave at transistor-transistor logic (TTL) levels. Afterward, it is fed into the PLL. Finally, the signal goes through a bandpass filter before going into the phase calculation stage.

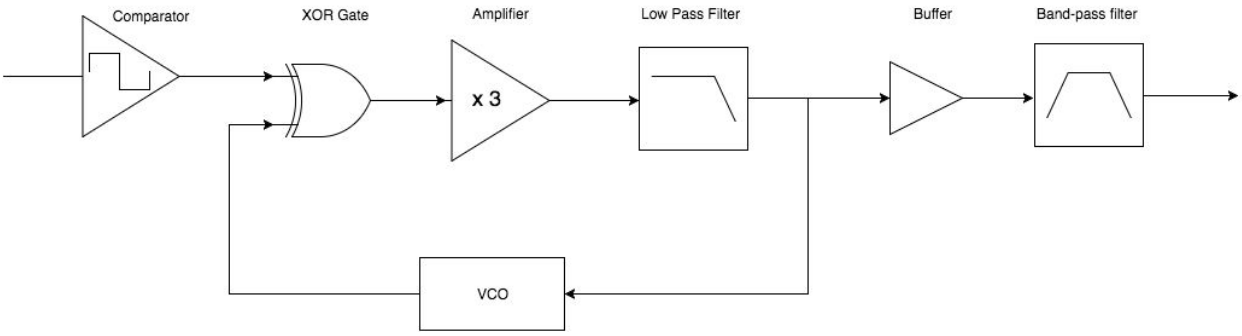


Figure 13: Block diagram for entire FM demodulation stage

To convert the output of the audio mixer stage to TTL levels square wave, I used a LM311 comparator chip with rails of 0V and 5V. Converting an FM signal into a square wave signal is fine because the phase shift information is encoded into the frequency of the signal, not the amplitude. Transforming an FM signal into a square wave only changes amplitude while preserves frequency.

Demodulating an FM signal can be achieved by many different methods. The topology I chose to use was a phase lock loop. This topology is commonly found in modern radio and electronic systems because of it can be built entirely on one integrated circuit (IC). Since IC fabrication is beyond the capabilities of this class, I thought it would be an interesting challenge to build a phase lock loop using only discrete components also this topology is able to detect a range of frequencies as opposed to being tuned to a single frequency.

The phase lock loop consists of three parts: the phase detector, a loop filter, and a voltage controlled oscillator (VCO). When the incoming signal frequency is perfectly matched in frequency to the output of the VCO, the output of the phase detector is 0 V. If the incoming signal is not matched the VCO, through feedback, the phase detector and the low pass filter work to make the VCO output match the incoming signal. So for an FM signal, as the frequency deviates around the carrier frequency, the input signal to the VCO will deviate as well in order for the VCO to stay locked.

The phase detector in my PLL is an XOR logic gate (74LS86). Because I used an XOR gate, which is a digital logic gate, both inputs to the gate needed to be at TTL levels. The output of this phase detector is a square wave that is at least twice the frequency of either the two input frequencies and with a duty ratio D_θ that depends on the phase difference φ.

$$D_\theta = \frac{\varphi}{\pi}$$

Figure 14 illustrates the operation of an XOR gate when the PLL is in the locked condition.

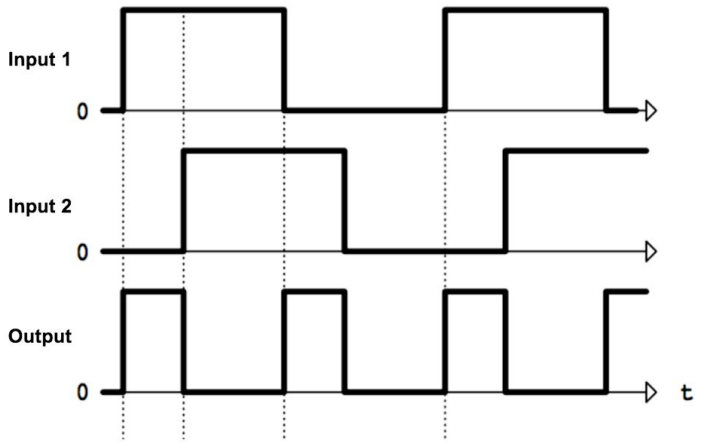


Figure 14: The output of an XOR gate when the PLL is locked

The loop filter takes in the phase comparator output removes any unwanted high frequency components. I implemented this as a simple first order low pass RC filter. Despite its simplicity, the loop filter determines the dynamics of the PLL, such as how quickly it can lock onto an incoming signal and how well it handles frequency variations in the incoming signal. The cutoff frequency for the low pass filter was 16 Hz. This frequency was chosen because it was low enough to better attenuate the high frequency components of the XOR output and improve noise rejection overall in the PLL. However, there is a tradeoff between capture range, the range of frequency deviations that the PLL can lock onto for arbitrary initial phase, and cutoff frequency; increasing the cutoff frequency yields a larger capture range, which is often desirable. For a first order RC filter, a very approximate expression for capture range can be solved for with this equation:

$$f_c = \frac{V_{DD}}{2} \frac{K_o}{\sqrt{1+\left(\frac{f_c}{f_p}\right)^2}}$$

where $2f_c$ is capture range, K_o is the gain of the VCO (more on this will be in the following paragraphs), and f_p is the cutoff frequency of the low pass filter.

The output of the loop filter is then fed into the VCO; this controls the frequency of the VCO output. The first op-amp in my VCO is an integrator. A voltage divider put the noninverting input of this op amp at half of the input voltage. Through negative feedback, the op-amp attempts to keep both inverting and noninverting input at the same voltage, requiring current to flow across

the 100k resistor (R3) to ensure that the inverting input voltage is the same as half the VCO input voltage. When the N-MOSFET (2N7000) is on, current from the inverting input flows through it. The 51k resistor (R6) has the same voltage drop but very closely half the resistance, so it must have twice as much current flowing through it. The 1.5 nF capacitor (C1) supplies this extra current. To source this current, the first op-amp proves a steadily increasing voltage. When the MOSFET is off, current from R3 goes through the capacitor, discharging it, so a steadily falling output voltage is supplied from the first op-amp. The second op-amp is a Schmitt trigger. When the input voltage rises above the threshold voltage of 3.33V, it outputs 5V and the threshold voltage falls down to 1.67V. When the input voltage drops below that, the output goes to 0V and the threshold moves back up to 3.33V. The output of this Schmitt trigger is a square wave and is connected to the MOSFET, causing the integrator to raise or low the output voltage. Since the input voltage to XOR gate needs to be from 0 to 5V, the output of the Schmitt trigger is also connected to the base of NPN (2N3904). This transistor acts as a switch, when the output of the Schmitt trigger is high the voltage at the collector is 5V, and when the output is low the voltage at the collector is 0V.

It is important to set the free-running frequency, the frequency that the VCO oscillates when the PLL is unlocked, close to the modulating frequency of the FM signal. The synthesized FM signal from the audio mixer has a modulating frequency of approximately 1 kHz. Through numerous trial and error, I got the free running frequency of the VCO to be 983 Hz. This process was especially difficult as changing the cutoff frequency of the loop filter or V_{DD} affected the free-running frequency. The gain of the VCO, defined as

$$K_o = \frac{\Delta f_{osc}}{\Delta v_o}$$

where Δf_{osc} is the change frequency of the VCO's output and Δv_o is the change in VCO input voltage, is a measure of how sensitive the VCO is to changes in input voltage. As seen early, having a large K_o is preferred as a larger K_o, the larger the capture range.

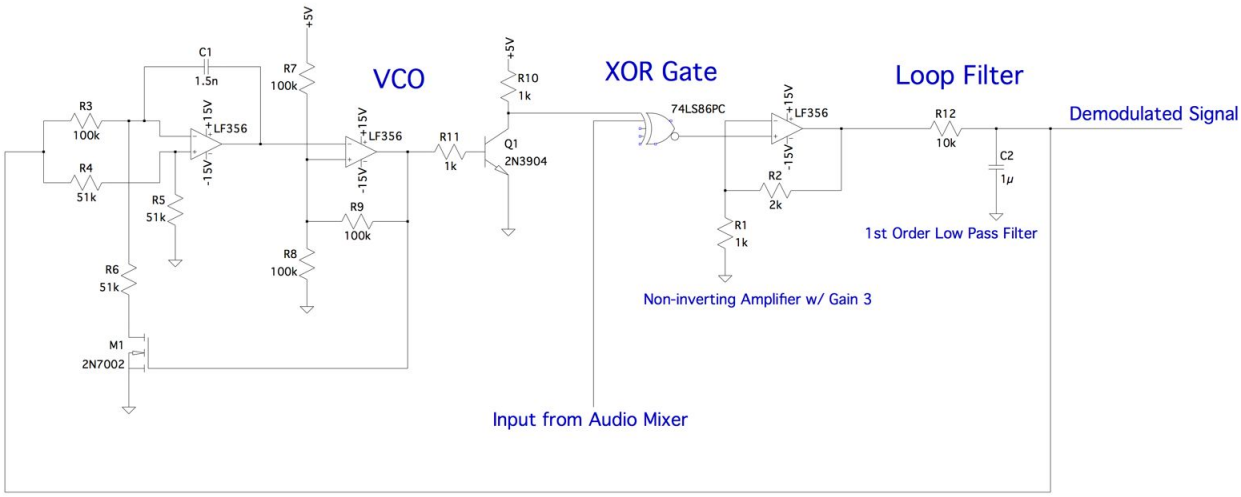


Figure 15: Circuit diagram for phase lock loop. Schematic diagram including part numbers, component values, and references for phase lock loop.

The output of the loop filter needs to be conditioned slightly more to get the demodulated signal, a DC offset is removed and a higher frequencies not removed by the low pass filter needs to be further attenuated.To do so, I designed Sallen-Key second order band-pass filter. A second order band pass filter was needed because the signal of interest was 50 Hz, which is less than order of magnitude away for the cutoff frequencies I wanted to use, 40 Hz and 160 Hz. A second order filter has a roll off of -40 db/decade, so it can attenuate frequencies that are close to its cutoff frequency more significantly than a first order filter can. Also, a buffer was added in between the loop filter in the PLL and the Sallen-key bandpass filter because the loop filter was a first order, passive low pass filter.

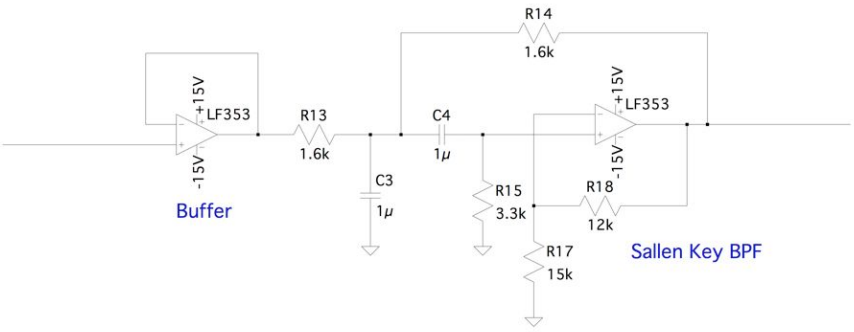
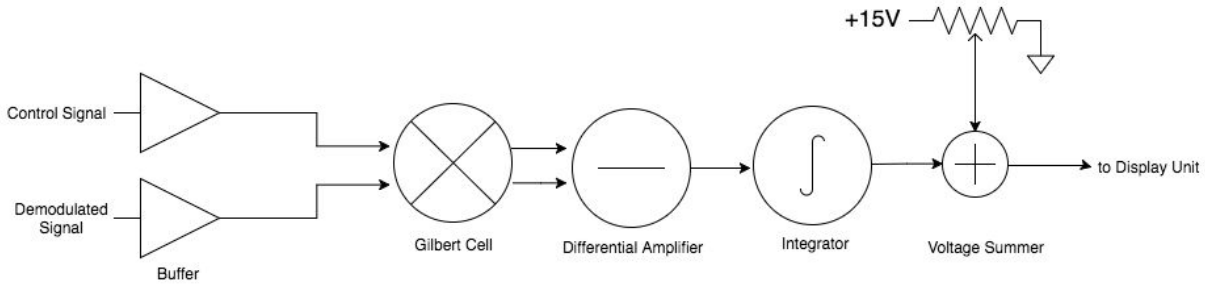


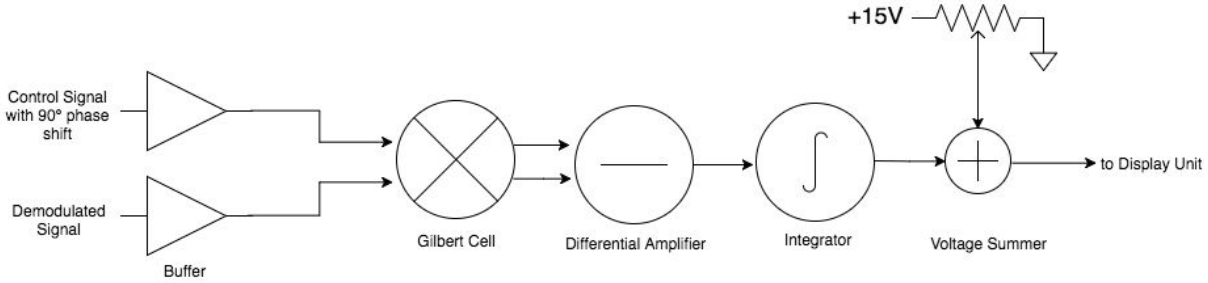
Figure 16: Circuit diagram for bandpass filter. Schematic diagram including part numbers, component values, and references for this filter.

Phase Calculation

In this stage, the phase difference between the signal from the microphone and the control signal is calculated. These signals are mixed together then are further processed to get a DC voltage proportional to $\sin\theta$, where θ is the phase difference between the two signals. The input to the second mixer is the signal of interest and the same control signal but with a 90° phase shift. This mixer module's output is a DC voltage proportional to $\cos\theta$.



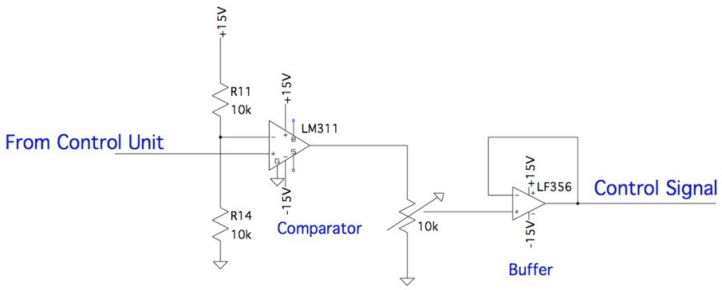
(a) DC output proportional to $\sin\theta$



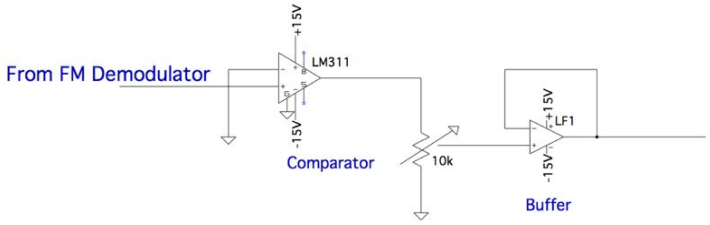
(b) DC output proportional to $\cos\theta$

Figure 17: Block diagram for phase calculation.

The two inputs to the Gilbert cell needed to be 400 mVpp square waves. To do this, I used a comparator (LM311) and a potentiometer to precisely tune the output to get it to levels I needed. Finally, I used a buffer to isolate the currents between the potentiometer and the base of the BJTs in the Gilbert cell.



(a) Control signal conditioner



(b) Demodulated signal conditioner

Figure 18: Circuit Diagrams for signal conditioning. Schematic diagrams including part numbers, component values, and references for the conditioners.

To mix two signals together, I decided to use a Gilbert cell as a sinusoidal phase detector, where the output is proportional to the sin or cosine of the phase difference . This was done by keeping the input signal levels to 400 mVpp and the value of the current source multiplied by the pull up resistors (R1 and R2) to be 1V. The current source sink is made a 2N3904 and 10k potentiometers connected to ground and -15V is used to bias the transistor. I chose to use a potentiometer because the value of the current source could be precisely tuned; however, this technique necessitates the current sources in the two mixers must be calibrated together or else the display does not move equally in the x and y directions.

In hindsight, mixing could also have been done using the same XOR chip from the PLL in the FM demodulation station. This would have reduced the area of my circuit, making my breadboard a lot more compact, and could have used 2 of the remaining 3 XOR gates in the chip. On the other hand, an XOR gate can only be utilized as a linearized phase detector, where the output linearly proportional to the phase difference.

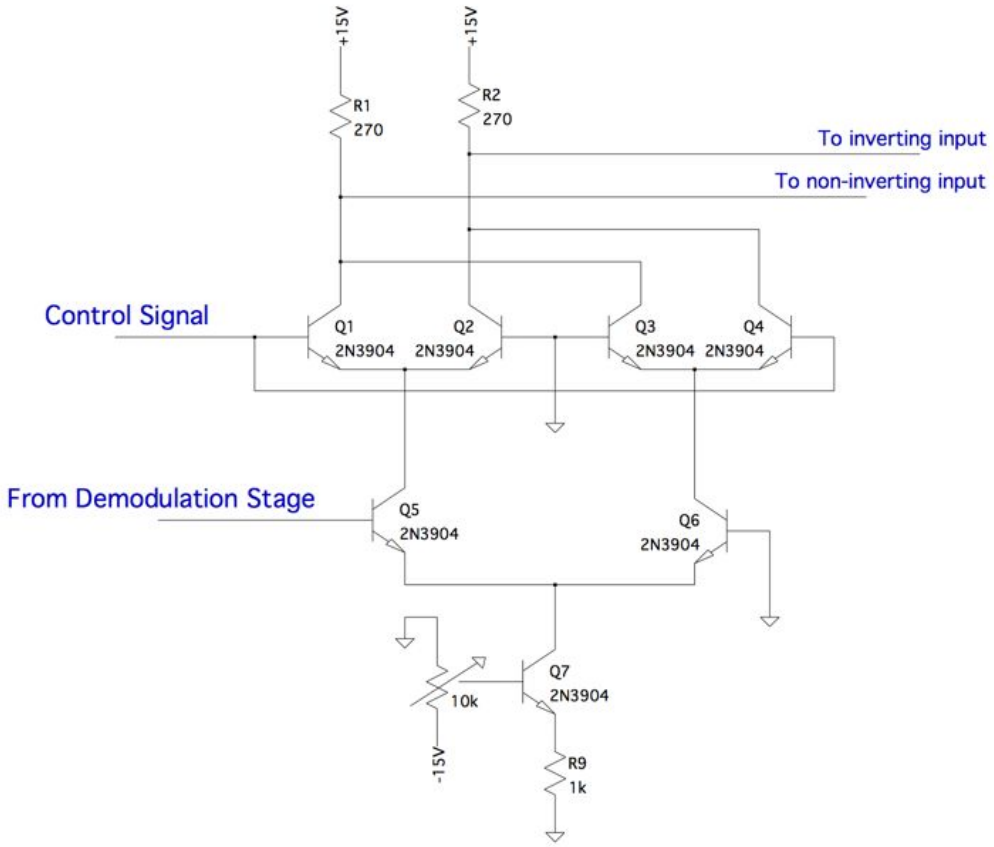


Figure 19: Circuit Diagram for mixing. Schematic diagram including part numbers, component values, and references for the mixer.

After going through the differential amplifier, the signal is passed through the integrator. The integral of a square wave over time results in a DC voltage. When operating at frequencies much higher than its cutoff frequency, a low pass filter acts acts an integrator. I built an active low-pass filter using an LF356 with a cutoff frequency of approximately 0.11 Hz, which is almost 3 orders of magnitude smaller than the integrator's input frequency of 100 Hz. From the integrator stage, the DC voltage is passed through a voltage summer. This is to make sure the output that goes to the display unit is centered around 0 V. The other input to the voltage summer was made using a potentiometer powered with +15 V and 0 V. I made the voltage summer using an active summer topology with a LF356 chip.

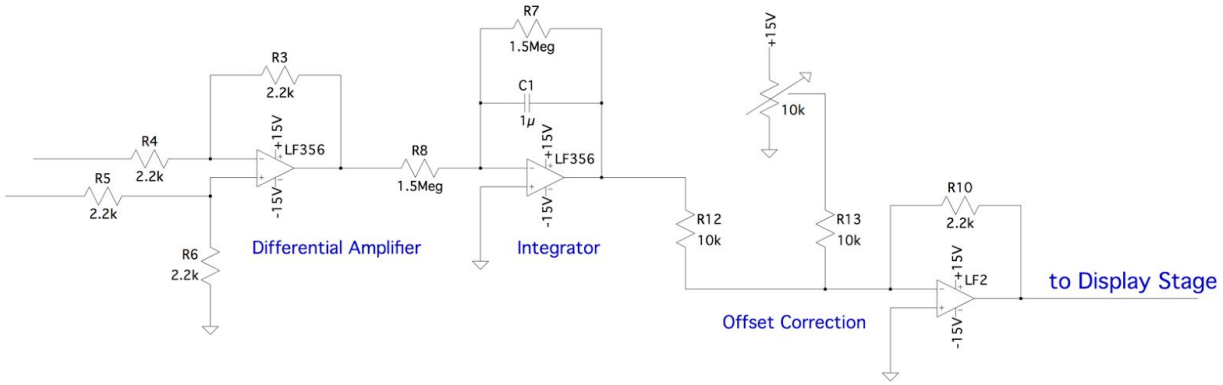


Figure 20: Circuit Diagram for converting square wave signal into a DC signal. Schematic diagram including part numbers and component values used

Display (Melissa)

Overview

The directional display uses the oscilloscope XY mode, which plots one channel against another on the screen by showing the phase and amplitude difference between two or more periodic waveforms. For example, for plotting a line from the origin (0,0) to the point (√3/2, 1/2), indicating ENE direction, the X-Channel signal will be a periodic wave oscillating from 0 to cos(pi/6) and the Y-Channel signal will be a periodic wave with the same period but oscillating from 0 to sin(pi/6). If the X-Channel and Y-Channel have the same signals but are 90° out of phase, the oscilloscope will display a circle.

The display module for the line can be decomposed into two blocks: the sawtooth generator and two voltage controlled amplifiers (Figure 21). The method uses the two DC voltages from the phase comparator to control the amplitudes of two sawtooth waves (oscillating from 0) and displays a line from the origin to the point corresponding to the direction of the signal source (Figure 22).

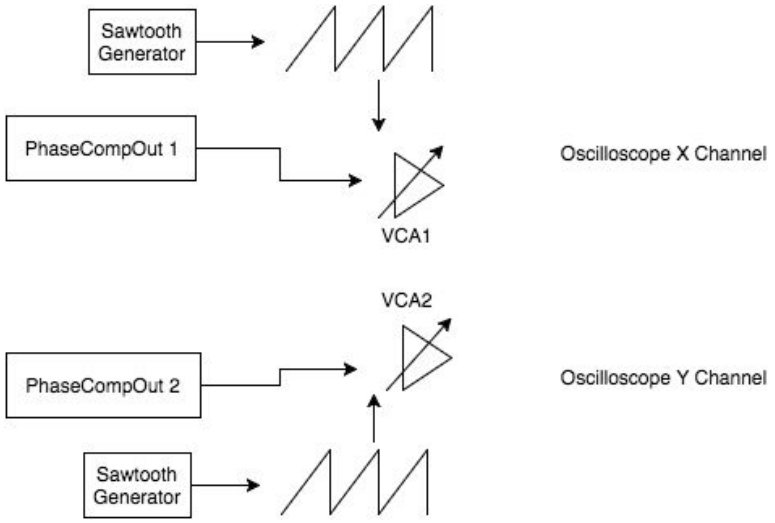


Figure 21: Block diagram for line display

Figure 22: Oscilloscope displaying line corresponding to different directions (45°,135°,225°,315°)

In addition to a line, an arc can be added to indicate the directional angle. The display module for the arc can be decomposed into the following blocks (Figure 23): sawtooth generator, voltage controlled amplifier, sine and cosine circuit calculators. The input to the cosine and sine circuits is sawtooth waveform with an amplitude controlled by a potentiometer. The amplitude of the VCA output waveform controls the angle of the arc drawn on the oscilloscope (Figure 24). For example, if the amplitude of the VCA output is $\pi/2$, the oscilloscope displays the 90° arc (24a); if the amplitude is $4\pi/6$, the oscilloscope displays a 120° arc (24b).

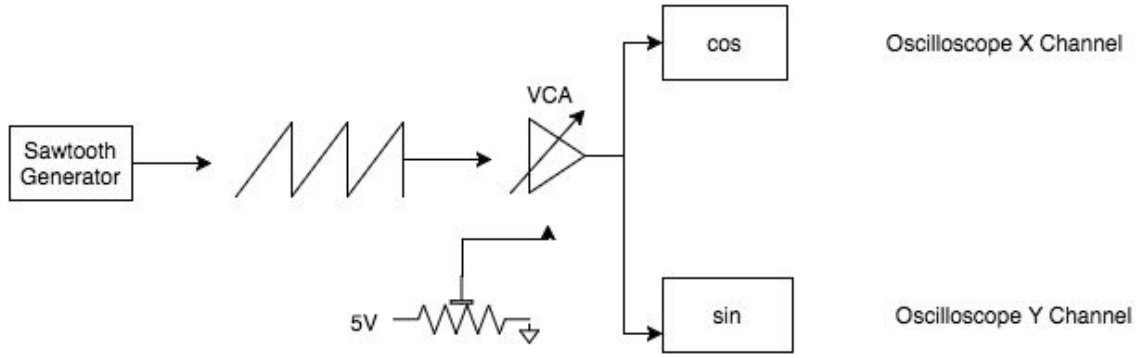


Figure 23: Block diagram for arc display

(a) (b)

Figure 24: Oscilloscope displaying arc corresponding to 90°(a) and 120°(b)

Design Specifications

The following constraints/specifications were applied:

- Operates off of the +/-15V and +5V lab bench power supply rails.
- All Op Amps were LF353's

Sawtooth Generator

The oscilloscope XY mode plots one channel against another by showing the phase and amplitude difference between two periodic waves, which can be sawtooth waves. A sawtooth generator circuit (Figure 25) is built by using a current source, made out of a 2N906 pnp (Q6), bias resistors (R11 and R18), and an emitter resistor (R9), to charge a capacitor (C2) in a linear ramp. The LT1011 comparator is then set to monitor the ramp for its upper threshold, which is set by R10 and R12 at 7.5V . At the upper level, the comparator then flips state and is used to discharge the capacitor quickly. If the comparator is set up with positive feedback so that it has both an upper and lower threshold then the comparator will flip back when the capacitor has discharged to the lower level. This would allow the cycle to repeat again to get a repeating sawtooth ramp. However, the output of the generated waveform has a slight offset since the 2N904 npns (Q4 and Q5) can not discharge the capacitor all the way to 0. Therefore, an offset correction circuit is added to the capacitor voltage. R19 should be a potentiometer to adjust the offset so that the sawtooth wave oscillates from 0V.

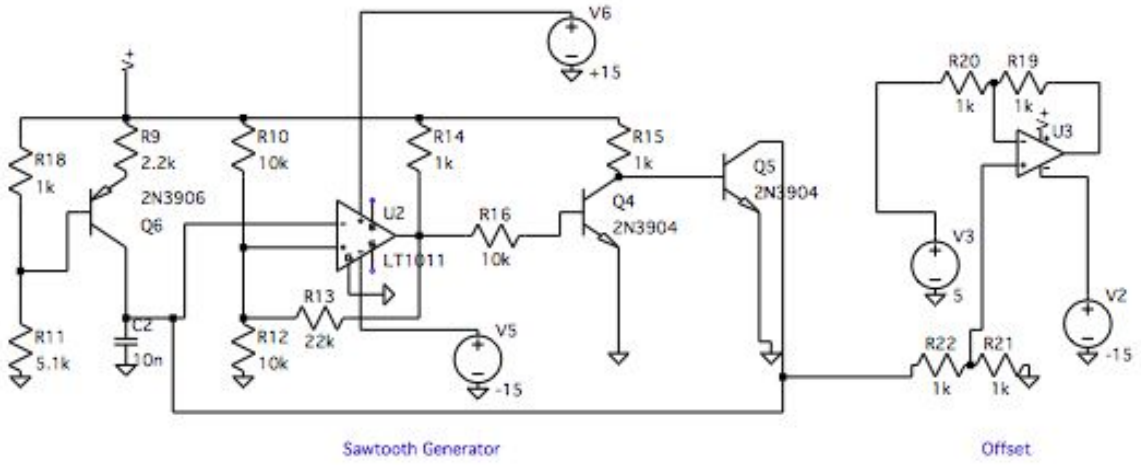


Figure 25: Sawtooth Generator

Voltage Controlled Amplifier

From Amanda's stage, one of the phase comparator outputs (PCO1) corresponds to the cosine of the phase difference and the other (PCO2) corresponds to the sine. The goal is to have the PCO's amplify the generated sawtooth wave to form two waves with zero phase difference: one oscillating from 0 to PCO1 and another one oscillating from 0 to PCO2. The two resulting periodic waves are the inputs for the oscilloscope channels.

Voltage Controlled Amplifiers (VCA's) are used to achieve this result (Figure 26). The chosen implementation has the advantages of low part count and simplicity. Similar to Jimmy's implementation, two 2N5462 PFETs (J1 and J2) operated in their linear regimes are used as a voltage controlled resistor. Its output resistance and gate-source bias are approximately linearly related for small drain-source voltages.

The waveforms for the two oscilloscope inputs should both oscillate from zero in order to draw a line starting from the origin. However, since the output of the VCA (node labeled VCA Output) oscillates from -PCO/2 to +PCO/2, an offset voltage is added to generate desired output waveforms oscillating from 0V to +PCO or from 0V to -PCO. Peak detectors are used to achieve the offset correct. The VCA Output is first amplified by 10 (R5 and R6) so that the signal is large enough for peak detection. The amplified signal is then fed into positive peak detector circuit and a negative peak detector circuit. The rectifiers for both the positive and negative peak detector are configured in a way where the 1N914 diodes (D1 and D2) are enclosed in the feedback loop of U5 and U8, respectively, and thus feedback corrects for the diode forward voltage drop "error". The switch uses two 2N7002 NMOS (M1 and M2) and depending on the polarity of the PCO, it shorts either the positive peak detector output or negative peak detector

output to the voltage summer (U7). The output of the voltage summer is a sawtooth wave oscillating from 0V to +PCO*10 or -PCO*10 and connects to one channel of the oscilloscope.

Since the phase comparator has two outputs, two of the circuits in Figure 26 are built: one for the X-Channel controlled by PCO1, and another for the Y-Channel controlled by PCO2. The positive and negative peak detection and offset for both channels allows for full 360° display.

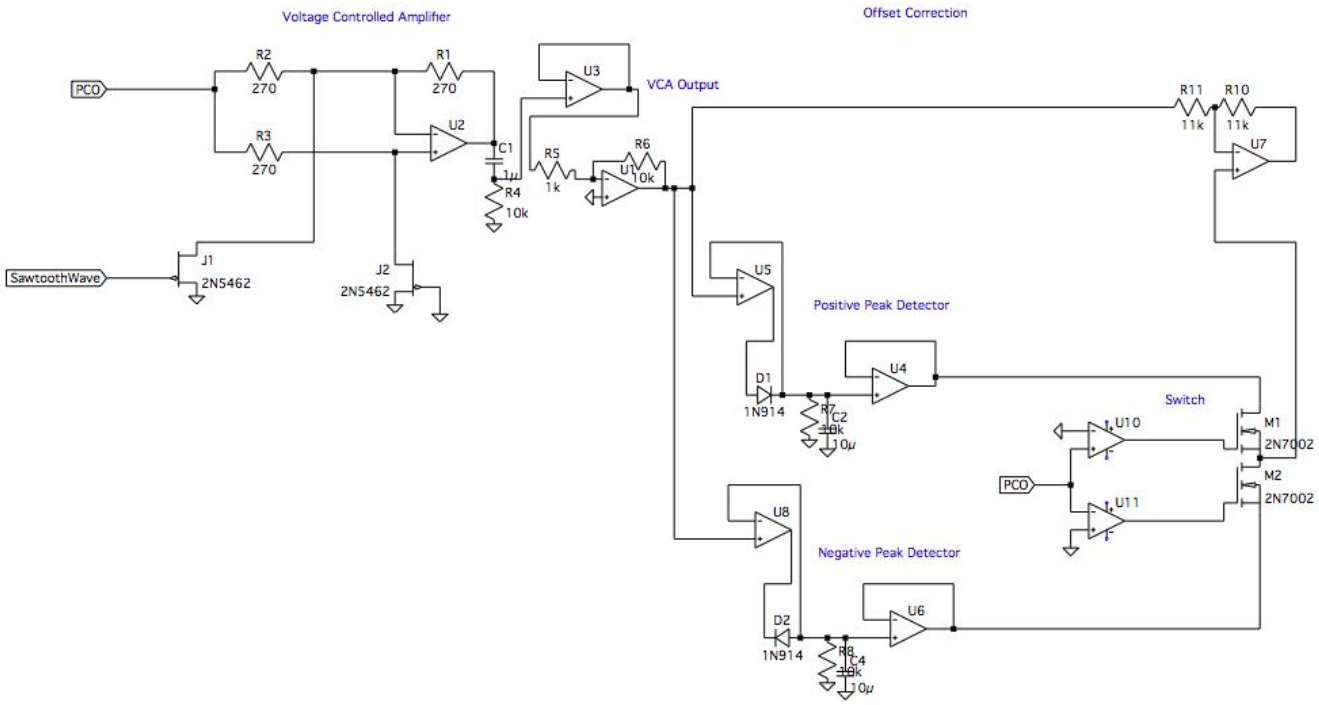


Figure 26: VCA and peak detector circuits for offset

Arc Display (Sine and Cosine Calculator)

As mentioned in the display overview, the arc display consists of the sawtooth generator, voltage controlled amplifier, and sine and cosine circuit calculators. The sawtooth generator is the same as the one used for the line display. The VCA is similar but with the following changes (Figure 27): input voltage controlled by 1k potentiometer (POT1) instead of phase comparator output, only the positive peak detector, and no switch.

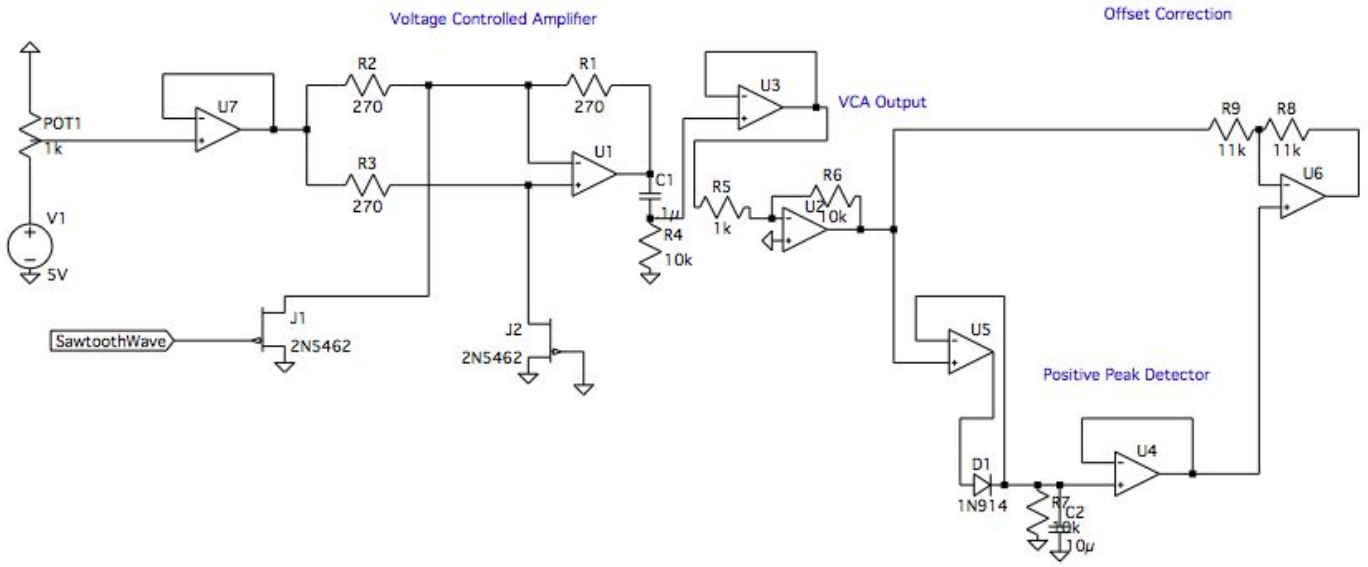


Figure 27: VCA for arc display

The output of the VCA for the arc display is a sawtooth wave oscillating from 0 to a voltage corresponding to the angle. The sawtooth wave is the input for both the cosine and sine calculator circuits. The implementation for the calculators uses translinear circuits (Figure 28 and 29) and taylor approximating the functions as $\cos x = 1 - \frac{x^2}{2}$ and $\sin x = x - \frac{x^3}{6}$. For the cosine circuit, J1 and J2 are 2N5462 PFETs used as current sources with R3 and R4. R3 and R4 are potentiometers that are adjusted so that J1 supplies 2mA and J2 supplies 1mA. Q1, Q2, Q3, and Q5 (All 2N906 pnp) form a translinear circuit so that the current through Q5 is the current through Q4 (2N904 npn) squared divided by two (i.e. the "$\frac{x^2}{2}$" term). Since the J2 current is 1mA (i.e. the "1" term), the output of the op-amp U1 is $1 - \frac{x^2}{2}$. The concept similarly applies for the sine circuit, where Q1, Q2, Q3, Q4, Q5, Q9 form an x^3 term and scaled by a factor of ⅙ through currents supplied by J1, J2 . The current through Q10 is the same as the current through Q8 (i.e. the "x" term), so the output of the circuit is $x - \frac{x^3}{6}$.

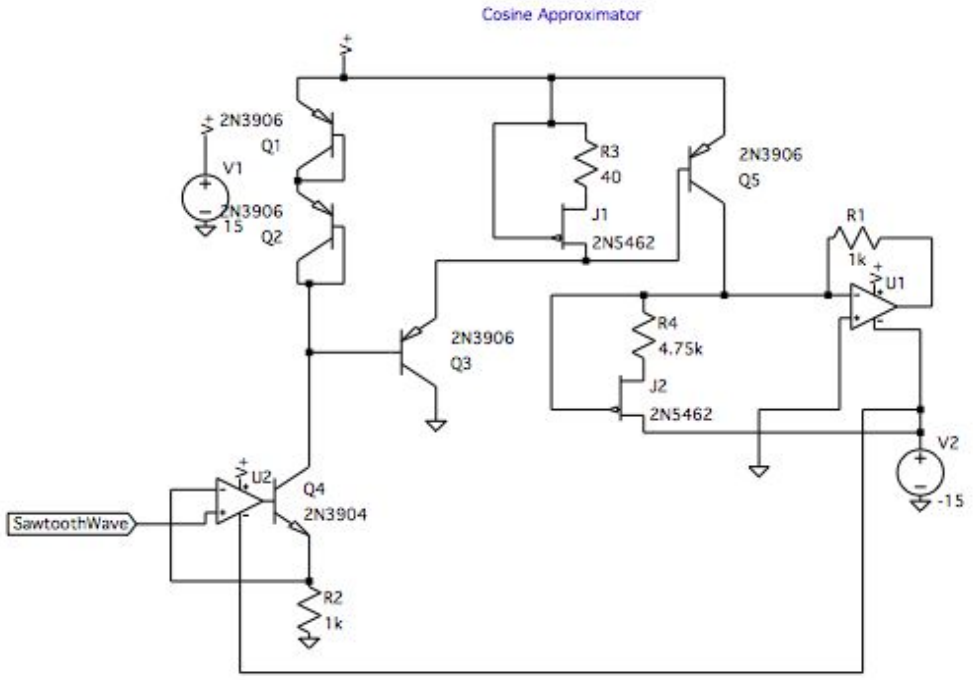


Figure 28: Cosine approximator

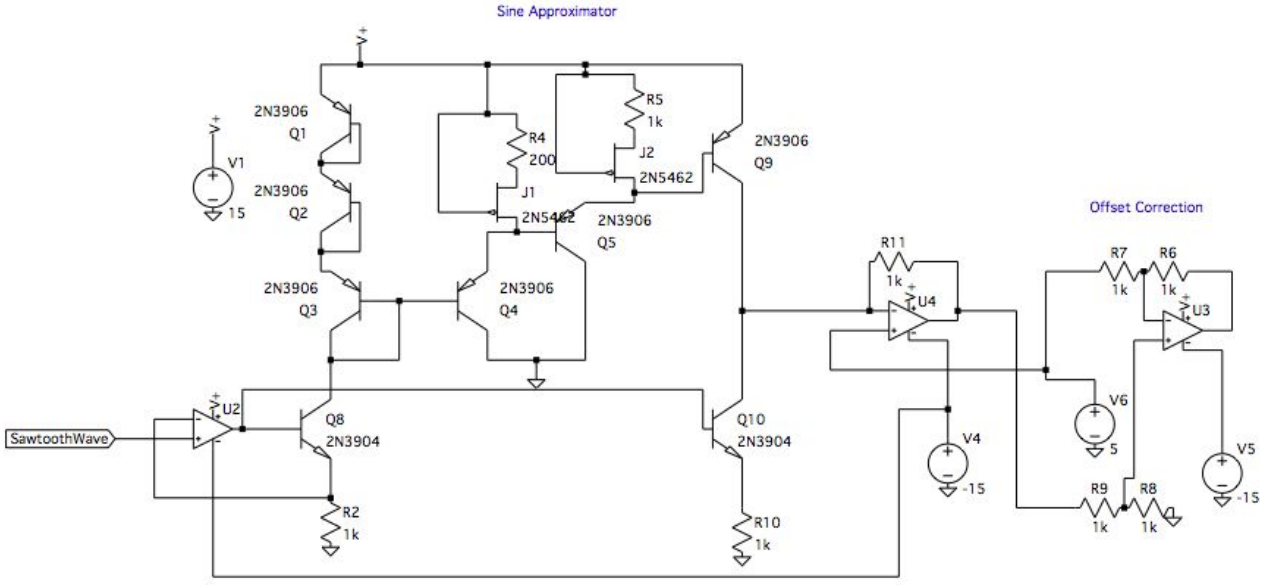


Figure 29: Sine approximator

The above circuits are approximations for angles between 0 to $\pi/2$ (first quadrant). However, as shown in Figure 30, as the angle increases, the approximations get worse.

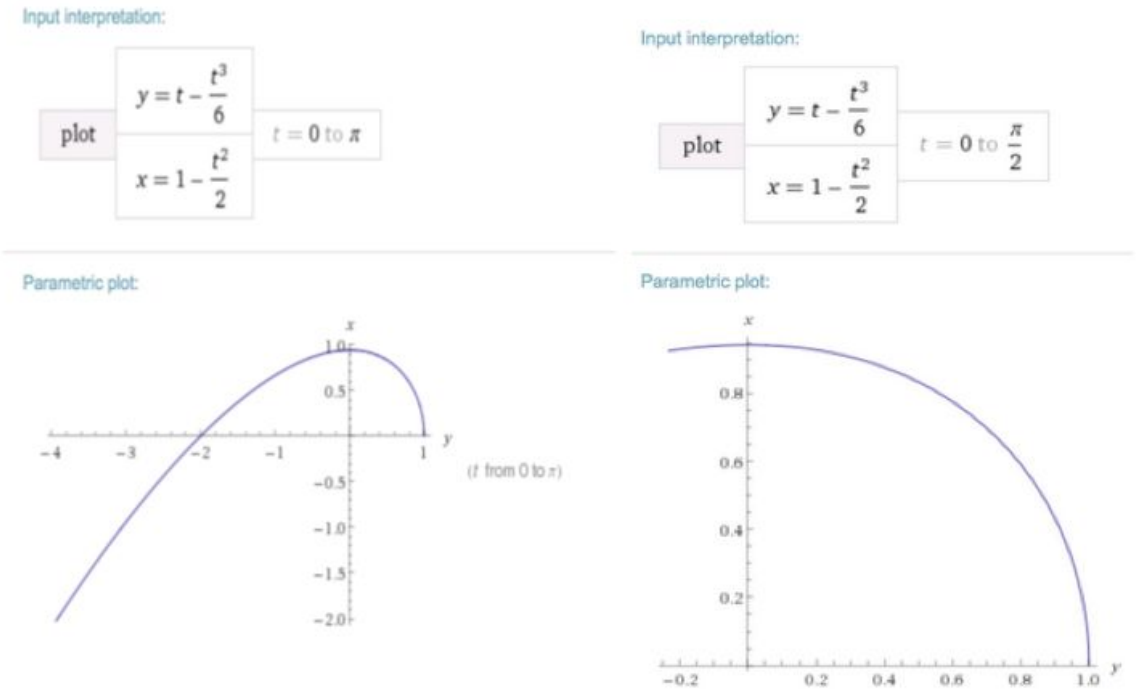


Figure 30: Parametric plots of taylor approximation. Right: angles 0 to π/2. Left: angles 0 to π.

Integration and Results

Testing proved the completed direction finder system to be successful. The completed system is able to respond to a changing source direction of arrival and update its display appropriately. Performance is limited somewhat by delays inherent in the gain control and FM demodulation blocks. The speed at which the our direction finder could track a source of sound was limited by how well the phase lock loop could lock onto a quick frequency deviations. If we rotated our test source too quickly around the microphones, the PLL could not demodulate the FM signal. Nonetheless, our system works well!

Acknowledgements

We are very thankful to all the course instructors, especially Gim and Elliot, and our CI-M instructors, Amelia Herb and Dave Custer, for their involvement in this project. Their mentorship and dedication was critical to this project's success.