Exponential Current DAC

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Objective:
To design a current-output digital-to-analog converter (iDAC) with an exponential code-current relationship. This is represented with the equation:

$$i_{OUT,tgt}(B) = I_{LSB} \cdot \alpha_R^{B/(2^N-1)}$$

Where, based on the design constraints, $I_{LSB} = 10\mu A$ and $\alpha_R = 20$. $N = 3$ was chosen to minimise complexity of the design, hence $B \in [0, 7]$, $B = B_2 B_1 B_0$.

Furthermore, the performance measure we are trying to maximise is M, which is:

$$M = \frac{2^N}{P_S \cdot |DNL| \cdot t_S \cdot |\varepsilon_{Scale}| \cdot \varepsilon_{out} \cdot |\Delta I_{LSB}| \cdot A_{LO} \cdot V_{L,min}}$$

To maximise M, all the variables in the denominator will be minimised to obtain the maximum value. Since the worst-case values are expected for M as input, the maximum value of the design changes/ simulations will be used to determine the performance quality of the iDAC.

Circuit topology:

The proposed current-steering iDAC is implemented using a 3-to-8 digital demultiplexer, level shifters for domain translation, and a current-mirror-based analog output stage. This topology provides accurate current output for each value of B while remaining compatible with standard CMOS processes.

**Fig 2:** Test bench schematic with the biasing loads and voltages.
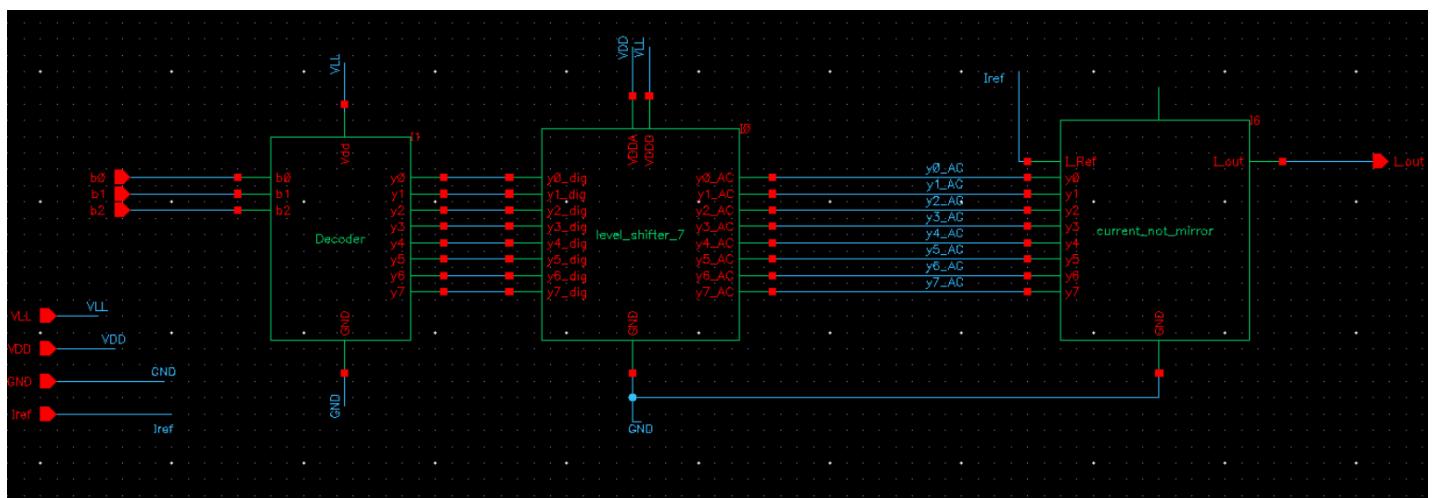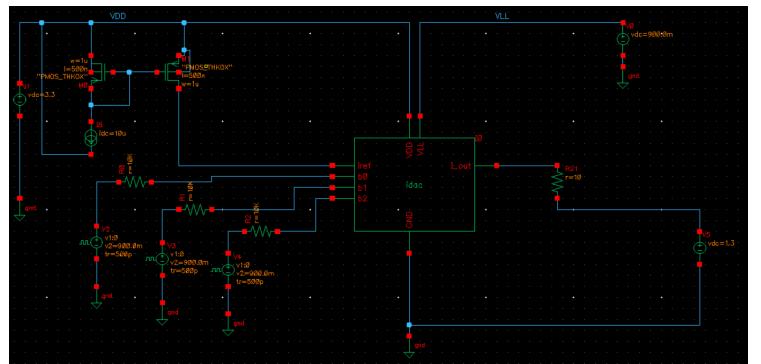
Fig 1: The topology of the circuit consisting of the digital block (decoder and the level shifter) and analog block (current mirror within which is are switches and buffer)

1. Digital Circuit:

3-to-8 demultiplexer:

The IDAC employs a 3-bit binary input that is converted to a one-hot control vector using a CMOS 3-to-8 decoder. This approach enables thermometer-coded selection, where only a single output line is active at any given time. Thermometer coding is preferred in mixed-signal CMOS design because it guarantees monotonicity and significantly reduces digital switching glitches compared to binary-weighted implementations.

As a result, the chosen transistor type was a VTG CMOS structure, as it is especially suited for our application due to its maximum supply voltage of 0.9V, and is generally useful for fast switching speeds (especially useful to reduce settling time) and low power consumption (reduces P_S).

Furthermore, they also function at lower widths and

lengths, minimising the area of the layout which is especially important for the performance measure, especially in comparison to the Thick-Oxide CMOS that will be used in the analog stages to compensate for the 3.3V power supply application.
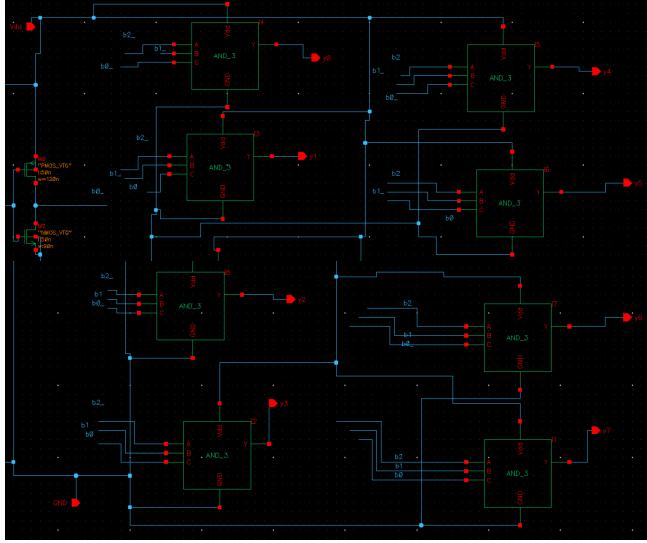

Fig 3: The logic blocks of the demultiplexer composed of a single AND gate, utilising the logic expression to encode the input information

Hence, the function of the demultiplexer is to represent the 8 unique values of B as a unique signal, which will later produce their own individual currents to represent the value as an AC current.

Hence, to represent the logic of the input 3 bit voltages to 8 separate voltages of 0.9V, the following truth table was used to design the multiplexer:

B_2	B_1	B_0	B	Logic equation
0	0	0	0	$\overline{B_2}\,\overline{B_1}\,\overline{B_0}$
0	0	1	1	$\overline{B_2}\,\overline{B_1}\,B_0$
0	1	0	2	$\overline{B_2}\,B_1\,\overline{B_0}$
0	1	1	3	$\overline{B_2}\,B_1\,B_0$
1	0	0	4	$B_2\,\overline{B_1}\,\overline{B_0}$
1	0	1	5	$B_2\,\overline{B_1}\,B_0$
1	1	0	6	$B_2\,B_1\,\overline{B_0}$
1	1	1	7	$B_2\,B_1\,B_0$

**Table 1:** Logic implementation of the demultiplexer block
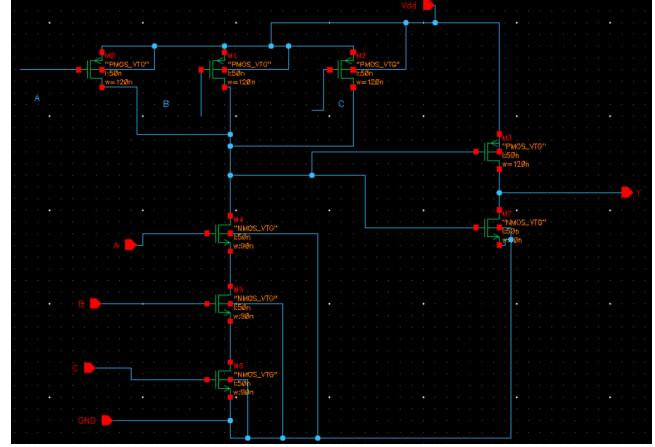
Fig 4: Schematic of the AND gate with dimensions

For the 3-input NAND gate, the widths and lengths were the lowest that this CMOS technology can handle which is

$$W_{NMOS} = 90n,\ W_{PMOS} = 120nm,$$
$$L_{NMOS} = L_{PMOS} = 50nm$$
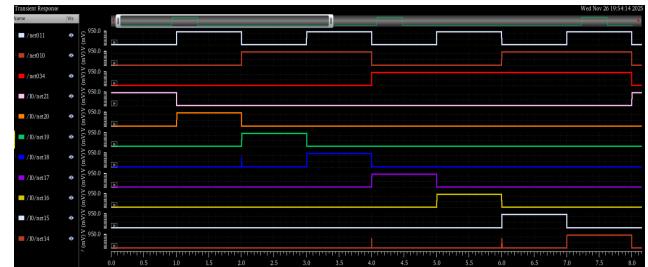
Fig 5: Transient simulation showing the demultiplexing of signal

Level Shifter:
To use the digital signal in the analog circuit, the voltage needs to be amplified to 3.3V, to ensure the switches in the analog circuit are in saturation mode. There were 2 main architectures considered for this function: a differential amplifier with a reference voltage or a level shifter circuit.

A level shifter is preferred over a voltage amplifier for interfacing the digital decoder with the analog switching network because unlike an amplifier, which produces a scaled analog output and cannot guarantee rail-to-rail swing due to headroom and bandwidth limitations, a level shifter generates well-defined digital "0" and "1" levels at the required higher supply voltage, ensuring that the MOS switches in the iDAC are fully enhanced and operate with minimal on-resistance.

Level shifters also consume negligible static power, occupy far less silicon area, and avoid stability and compensation issues inherent in amplifiers. Additionally, they inherently protect low-voltage transistors from gate-oxide overstress when crossing voltage domains. For these reasons, a level shifter offers a simpler, more reliable, and more power-efficient solution for digital-to-analog domain interfacing in CMOS iDAC designs.

The widths and lengths of the thick-oxide transistor (the analog conversion component of the level shifter) must be at least 3 times that of the digital inverters used in the previous blocks. Furthermore, the output resistance of this component must be significantly lower than that of the current mirror, represented by $R_{on} = L/(k_\lambda I_D)$, hence a larger length for the thick-oxide CMOS. Finally, the NMOS pull-down network is typically sized larger than the PMOS pull-up devices to ensure reliable switching when translating from a low-voltage digital domain to a higher-voltage analog domain to ensure rapid discharging. Through experimentation, a width of 20μm was optimal in ensuring a stable digital output scale for the analog component.
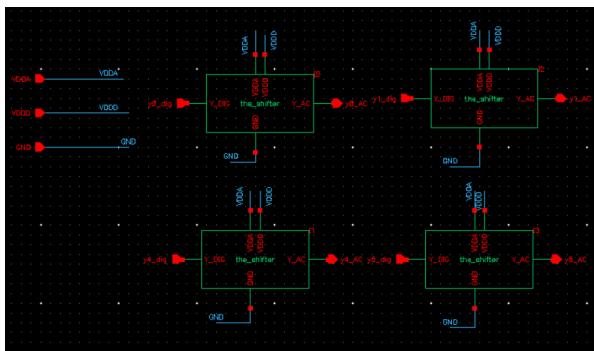

**Fig 6:** The 7 level shifter for each of the digital number signal lines
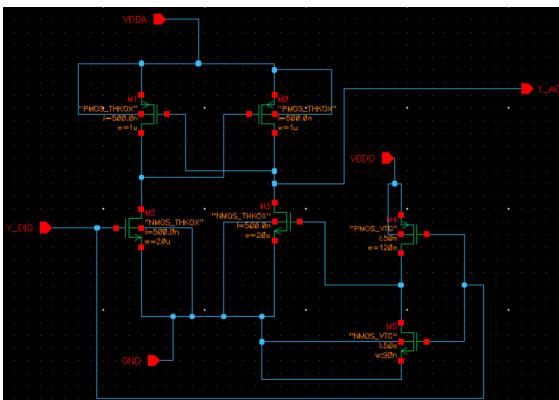
Fig 7: Transistor widths and lengths of the level shifter, with a large pull-down network width to ensure safe amplification
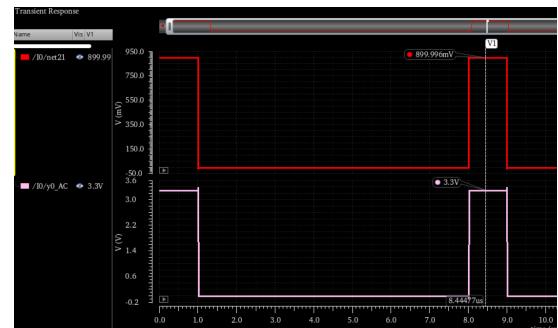

Fig 8: The digital input (V = 0.9V) and amplified output (V = 3.3V) of the level shifter

2. Analog Circuit

Current mirror:

A current mirror is the most suitable structure for implementing an iDAC because it provides accurate and repeatable current generation based on transistor geometry ratios rather than absolute device values, which are poorly controlled in CMOS.

This component is the first to use the source current reference, which has been decided to be $10\mu A$, which is the LSB current.

The PMOS in the test bench is set to be of with a width of $2\ \mu m$, the same as that of the output PMOS of the level shifter. An NMOS network is used within the current mirror to ensure the current is correctly pulled down and to prevent interference from the output voltages in biasing the mirror. Since the currents in each of the current mirror channels (1 channel per value of B) are larger that $10mA$, the calculated widths of the NMOS and the implemented widths are as shown below:

$I_{out, expected}$ [mA]	$W_{NMOS, theoretical}$ [μm]	$W_{NMOS, real}$ [μm]
10.000	1.000	1.000
15.341	1.534	0.747
23.535	2.354	1.280
36.106	3.611	2.000
55.392	5.539	3.200
84.978	8.498	5.100
130.367	13.037	7.500
200.000	20.000	12.000

Table 9: Calculated based on the ratio of the current-replicating NMOS of width $1\mu m$, which has a current of $10mA$ to the amplified current.

A current mirror is preferred over an amplifier for IDAC implementation because it directly replicates and scales currents with minimal logic delay and far greater architectural flexibility. Since a current mirror operates purely through transistor biasing, the output current responds immediately to digital switching of the unit branches, avoiding the settling-time overhead, compensation requirements, and bandwidth limitations inherent in amplifiers. This allows faster, more deterministic switching and reduces latency through the DAC path.

Despite its advantages, a current-mirror-based iDAC has several limitations compared to amplifier-based approaches. Its accuracy depends strongly on device matching and layout quality, with variations in threshold voltage, mobility, and channel-length modulation directly affecting linearity. The finite output resistance of mirror devices also restricts output compliance, causing current errors as the output voltage varies, whereas amplifiers can use feedback to maintain accurate current over a wider operating range. Hence, considering these options, the current mirror was chosen primarily due to its flexibility in prototyping, over a potentially more power drawing, wider layout area amplifier design which works better for linear DAC's due to its linear growth and direct regular interval amplification.
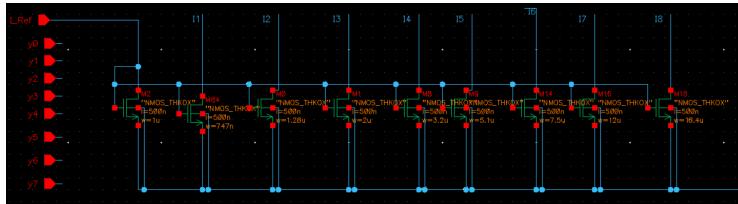

Fig 10: Schematic of the current with transistor dimensions represented in **Table 2**.

Switching:

The initial prototypes started with the implementation of a transmission gate, but the key drawback was the introduction of V_{DD} back into the current mirror conflicting with the load voltages and working against NMOS pull-down network current mirror. Hence a simple NMOS switching network was used.
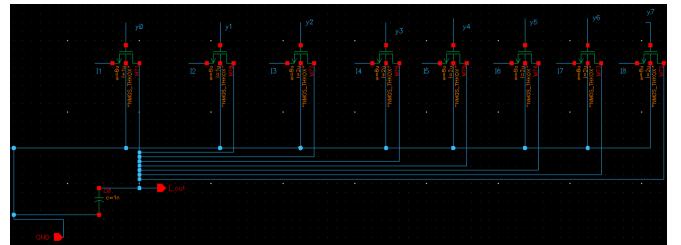
Increasing transistor length to $1\mu m$ improved matching, output dependence, and enhanced analog accuracy, but it slows switching due to increased on-resistance and capacitance.This was a compromise that could be made due to the highly optimised digital topology, ensuring a stable current output through the switches without a significant settling time or propagation delay.

The widths of all of the switches were maintained to be a constant of $8\mu m$ to ensure the channel is large enough for even the highest current of the current mirror to flow through.

A small capacitor of $1nF$ was integrated at the end as a filter to minimise the impact of the load voltages and reduce the large spikes and sudden changes that were prevalent in multiple initial versions of the design. A parametric sweep was done to ensure the impact of the capacitor was minimal on the switching speed, but is a temporary solution for a full implementation of a buffer.

To achieve this, an **inverter buffer** or an **output cascoded current mirror** is required, increasing the small-signal output resistance while reducing current variation with load compliance voltage.

Fig 11: The NMOS switching network with a buffer capacitor to protect the mirror from load voltages and minimise current spikes

Circuit simulations:

Transient simulation:

Fig 12: At $V_L = 2.5\,V$ and $R_L = 0\,\Omega$
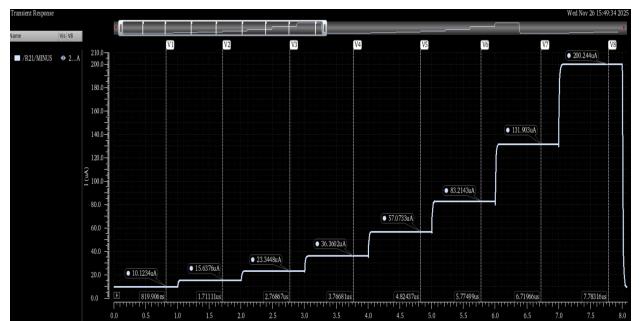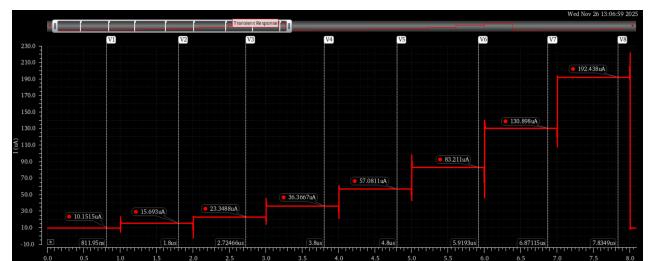
Fig 13: At $V_L = 3.3\,V$ and $R_L = 10k\,\Omega$

The voltage levels shown in the screenshot have been used for further calculations in the technical performance sections, and its values will be listed in the appendix for reference if the image is not readable.

Design Technical Performance:
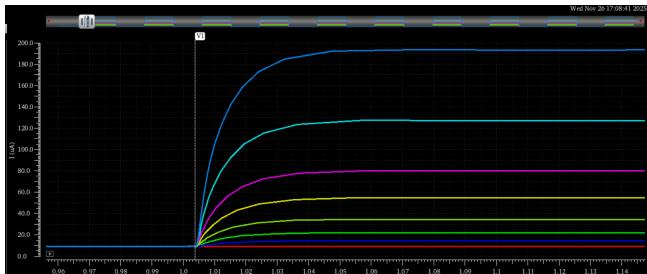
Corner Simulations - settling times:
The most important and optimisable component of the network was the settling time - time it takes to go from $i_{OUT}(0)$ to $i_{OUT}(B)$ - especially enabled by the digital network design with VTG transistors and the transistor dimension decisions made.

For an iDAC, fast/slow (F/S) corner simulations are critical because they capture the extremes of process-induced variations in transistor speed and drive capability, which directly affect the current mirror and switching network. It allows designers to verify that the output current remains within specification, monotonicity is preserved, and switching speed is adequate under worst-case fast or slow process extremes.

Hence, the settling times (at $V_L = 2.5V, R = 0\Omega$) obtained for the slow-corner process is represented below:

Fig 14: Settling time for slow-corner process

SLOW			
B	t_0	t_high	t_settle (ns)
1	1.00427	1.022	**0.018**
2	1.00427	1.029	**0.025**
3	1.00427	1.0352	**0.031**
4	1.00427	1.041	**0.037**
5	1.00427	1.052	**0.048**
6	1.00427	1.053	**0.049**
7	1.00427	1.056	**0.052**
FAST			
B	t_0	t_high	t_settle (ns)
1	1.001367	1.019	**0.018**

2	1.001367	1.027	**0.026**
3	1.001367	1.034352	**0.033**
4	1.001367	1.038021	**0.037**
5	1.001367	1.043012	**0.042**
6	1.001367	1.048002	**0.047**
7	1.001367	1.047415	**0.046**

Analysis ($V_L = 2.5V, R = 0\Omega$)**:**

Monte-Carlo simulations:
This ensures the transistor widths and lengths are optimised to produce the output closest to the projected output, which was considerably close to the calculated theoretical value, as shown in the graph with the optimised width-length configuration with other closer lengths.
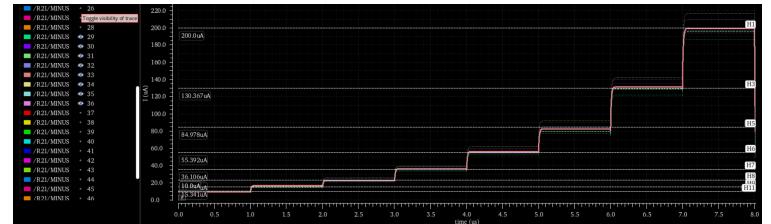
Fig 15: Monte-Carlo simulation with ideal case highlighted in pink, with other random widths and lengths in dotted lines.

Power dissipation:

Using the equation $P = V \cdot \frac{1}{T}\int_0^T I(t)\,dt$ with the calculator, the measured power drawn is:

Power consumption				
V_DD [V]	V_LL [V]	I_DD_avg [nA]	I_LL_avg [nA]	P_s [mW]
3.3	0.9	403.7	164	0.00147981

Performance Measures ($V_L = 2.5V, R = 0\Omega$) **:**

i_out_measured [µA]	I_out_cmp [µA]	DNL	ΔI_cmp
10.1234	10.1234		2.084494626
15.6376	15.50609914	0.02443028162	3.192838407
23.3448	23.75082588	0.06519642781	4.890498142
36.36	36.37934496	0.03061965635	7.490818208
57.0733	55.72255663	0.07083044727	11.47375089
83.21	85.35072087	0.1178427462	17.57444326
131.903	130.7324357	0.07296518339	26.91892641
200.244	200.244	0.0168398495	41.23195189

Range scale error: 0.01098
LSB offset: 0.123µA

The calculation of relative output current variation due to output voltage using the table below:

V_I = 2.5V	V_I = 1.3V	V_I = 3.3V	
R = 0	R = 0	R = 0	
I_out_measured [µA]	I_out_measured [µA]	I_out_measured [µA]	ε_out
10.1491	9.56	10.1518	0.058311
15.6894	14.74	15.7	0.061188
23.3500	22.0054	23.35	0.057585
36.3600	34.33	36.37	0.056106
57.0737	54.0312	57.093	0.053646
83.2100	79.002	83.25	0.051052
131.9000	125.735	131.97	0.047271
200.2400	191.62	200.349	0.043593

The calculated area of the layout is specified below:

A(and gate) [µm^2]	0.042
A(decoder) [µm^2]	0.36750
A(shifter) [µm^2]	168.084
A(mirror) [µm^2]	25.6135
A(switches) [µm^2]	128.000
A(total)	322.065

Hence, this leads to:

2^N	P_sup [mW]	|DNL(max)|	t_S [µs] (max)	ε_scale
8	0.00147981	0.1178	0.000051730	0.01098445186
ε_out	**ΔLSB [µA]**	**A_LO [µm^2]**	**V_L,min [V]**	**M**
0.061188	0.123000	16882.6	1.3	488773457.5

Hence, under these conditions, the worst-case calculated M is:

$$4.888 \times 10^8 \, (mW \cdot \mu s \cdot \mu A \cdot \mu m^2 \cdot V)^{-1}$$

Finally when the load resistance is 10kΩ:

I_out_measured [µA], R=10kΩ	Δi_out,cmp, R = 10kΩ
10.152	2.090
15.693	3.182
23.348	4.845
36.367	7.376
57.081	11.229
83.211	17.096

130.898	26.027
192.438	39.625

Appendix:

Other design constraints include:

Parameter	Value
Power supply V_{DD}	3.3 V
Power supply V_{LL}	0.9 V
Bias current	10µA
Bias voltage	Unused
Logic high V_H	0.9 V
Logic low V_L	0 V
Load resistance R_L	$0k\Omega$, $10k\Omega$
Minimum load voltage R_L	Fixed to 1.3V
Source Resistance R_S	$10k\Omega$
Maximum dynamic non-linearity $|DNL(B)|_{max}$	≤ 1

Where:

P_S = iDAC power consumption $[mW]$

DNL = differential non-linearly [unitless] - measure of the deviation between $i_{OUT,tgt}(B)$ and $i_{OUT,meas}(B)$

t_S = settling time [µs] - time it takes to go from $i_{OUT}(0)$ to $i_{OUT}(B)$

ε_{Scale} = range scale error [unitless] - deviation of the range of output from the expected output range characterised by α_R

ε_{Out} = relative output current variation due to output voltage [unitless]

ΔI_{LSB} = least-significant bit error $[\mu A]$ - difference between the expected LSB current and the actual LSB current

A_{LO} = Estimated area layout $[\mu m^2]$

$V_{L,min}$ = lowest load voltage [V]

Current values for fig 12 and 13:

I_out_measured (microA) R=10k	I_out_measured (microA) R=0
10.1515	10.1491
15.6930	15.6894
23.3480	23.3500
36.3667	36.3600
57.0811	57.0737
83.2110	83.2100
130.8980	131.9000
192.4380	200.2400