16-bit Signed Combinational Logic Multiplier

This design describes a 16-bit combinational logic multiplier for signed numbers. The inputs are denoted as A_0 to A_{15} for the multiplicand and B_0 to B_{15} for the multiplier. The resulting product is represented by P_0 to P_{31}.

Algorithm Overview

- **Partial Products Generation:**
  - Each partial product is generated by performing bitwise AND operations between the corresponding bits of the multiplicand and multiplier.
  - Instead of extending the bits for each partial product, the most significant bit (MSB) of each partial product is generated using a NAND operation. This ensures correct handling of the sign bit.
- **Special Handling of the Last Partial Product:**
  - For the last partial product, all bits are generated using NAND operations except for its MSB which is AND operation. This ensures the correct signed multiplication result.

Significance

- The use of NAND and NOT operations for the MSB of partial products ensures the correct handling of negative numbers.
- This approach simplifies the hardware implementation by avoiding bit extension for partial products and directly addressing sign extension through logical operations.

This method ensures a consistent and efficient design for a 16-bit signed combinational logic multiplier, correctly accounting for the sign bits and ensuring accurate results.