Lecture-50

Intel 8255A: Programming and Operating Modes

Operation Description:

There are three basic modes of operation that can be selected by the system software.

Mode 0: Basic Input/output

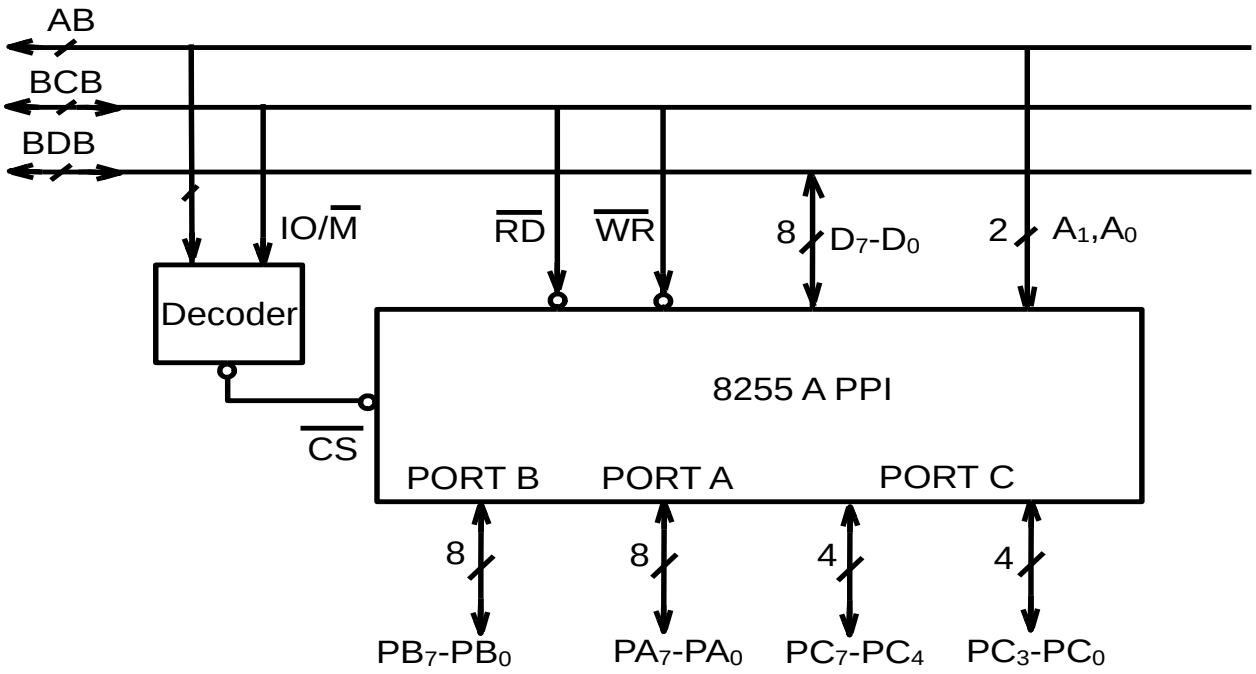
Mode 1: Strobes Input/output

Mode 2: Bi-direction bus.

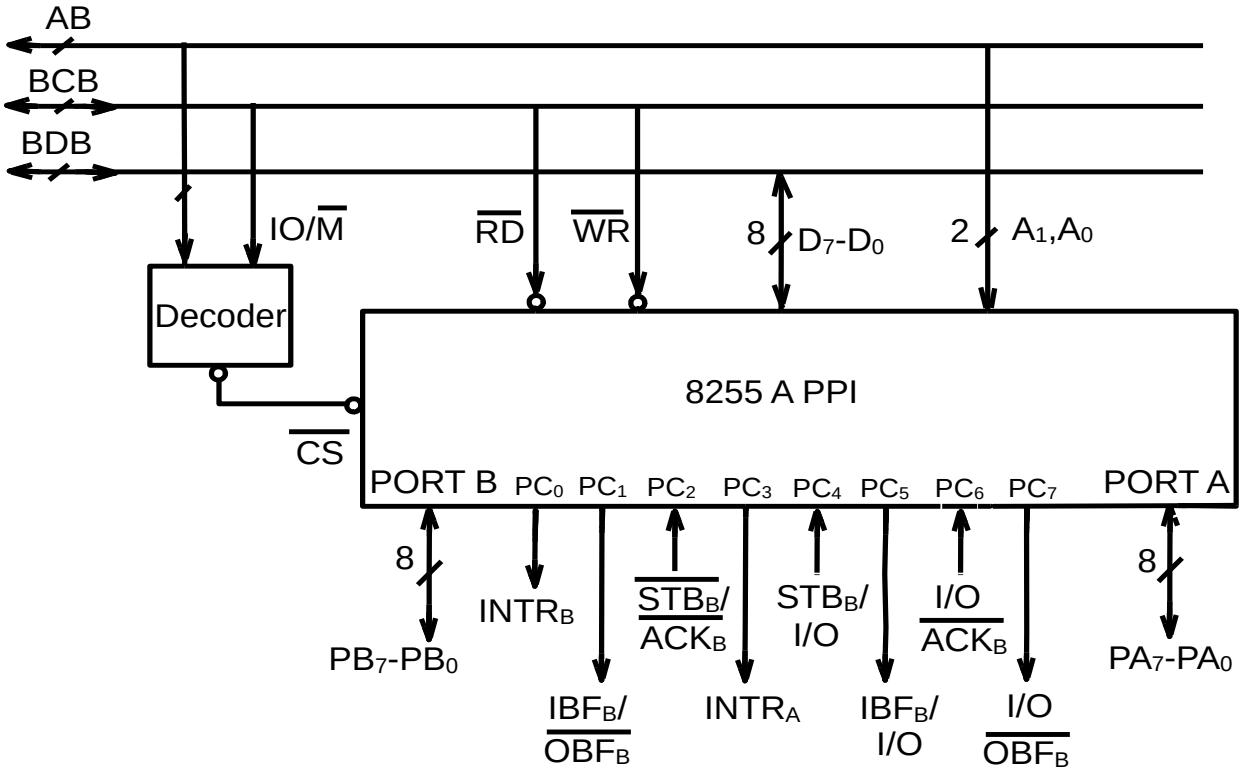
When the reset input goes HIGH all ports are set in mode-0 as input which means all 24 lines are in high impedance state and can be used as normal input. After the reset is removed the 8255A remains in the input mode with no additional initialization. During the execution of the program any of the other modes may be selected using a single output instruction.

The modes for PORT A & PORT B can be separately defined, while PORT C is divided into two portions as required by the PORT A and PORT B definitions. The ports are thus divided into two groups Group A & Group B. All the output register, including the status flip-flop will be reset whenever the mode is changed. Modes of the two groups may be combined for any desired I/O operation e.g. Group A in mode-1 and group B in mode-0.

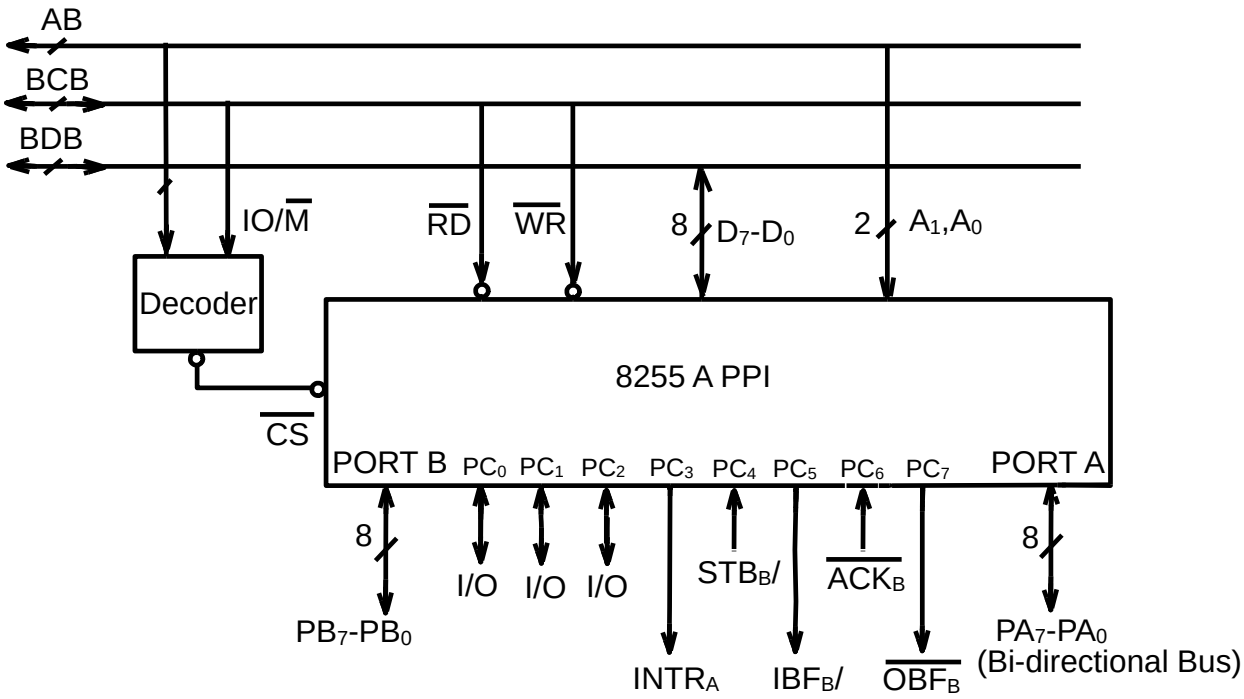
The basic mode definitions with bus interface are given in fig9.5 (a) (b) and (c).



(a) Mode-0



(b) Mode-1



(c) Mode-2

Fig.9.5 Mode Definition with Bus Interface

The format for the control word is given in fig.9.6.

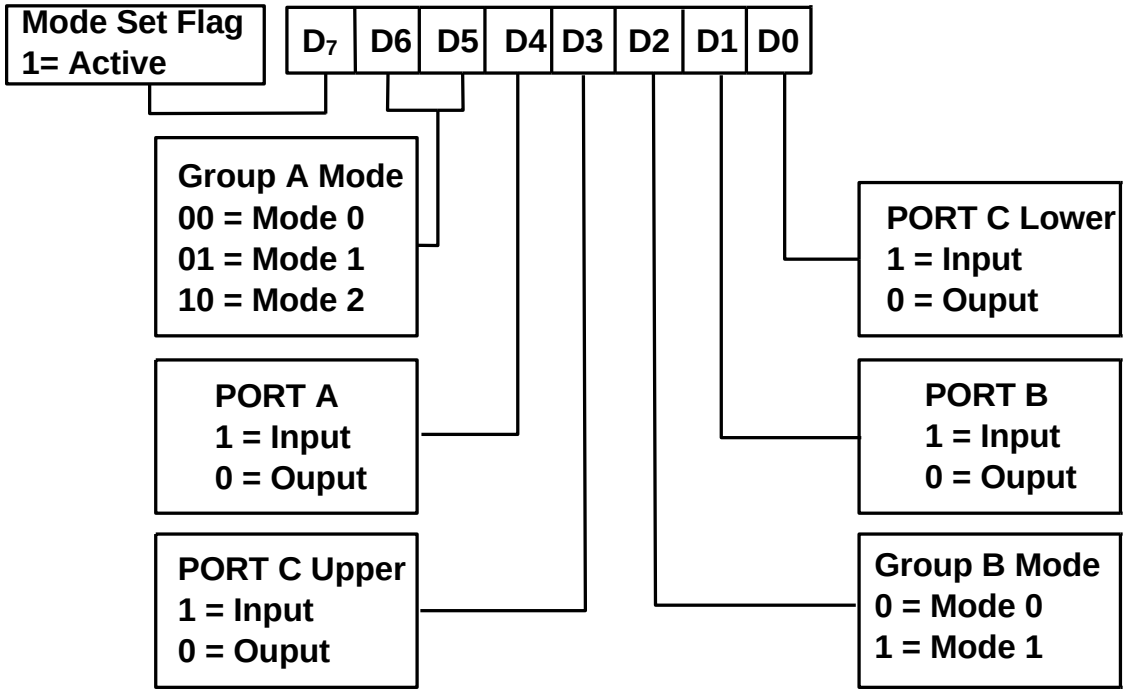


Fig.9.6 Mode Set Control Word Format

Single Bit Set-Reset Feature:

Any of the eight bits of PORT C programmed in output mode can be SET (High) or Reset (Low) using a single OUTPUT instruction without affecting other bits of PORT C. This feature reduces software requirement in control application. When PORT C is being used as status /control for PORT A or PORT B, these bits can be set or reset by using the bit set/reset operation just as if they were data output ports. The bit set/reset format is given below:

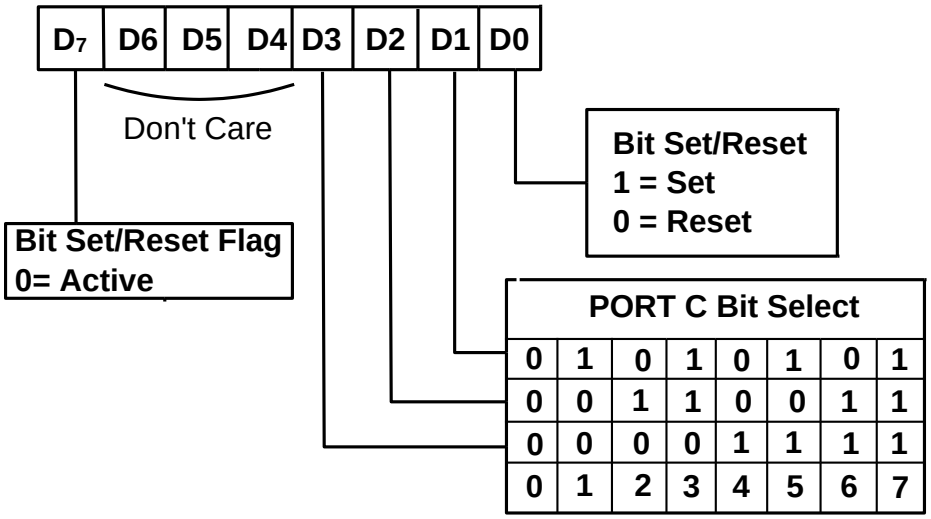


Fig.9.7 Bit-Set Reset Control Word Format

The control word formed to set or reset any bit of PORT C is issued to control word register instead of PORT C register.

An example for interfacing 8255A with CPU:

If 8255A is programmed in isolated I/O mapped manner, then IN PORT & OUT PORT instructions are used for data transfer. When these instructions are executed, the 8085A duplicates the PORT address on the address bus and on the address data bus as discussed earlier. Thus,

$$A_{15} – A_8 = AD_7 – AD_0$$

This equation is called the duplication equation. Therefore PORT A is read if

$$A_{15} – A_8 = AD_7 – AD_0$$

$$xxxx\ xx00 = xxxx\ \ xx00$$

We may allocate any address to 8255A by selecting A_{15}-A_{10} bits. Let us assume A_{15}- A_{11} bits to be 00000 for generating the chip select signal along with IO/$\overline{M}$ = 1. A_{10} bit is not used in generating chip select signal and is redundant. Therefore PORT A is accessed when address bus is having A_{15}- A_8 be 0000 0x00. Therefore, primary address for PORT A becomes 00H and fold back address becomes 04H. Accordingly, the other ports PORT B, PORT C and Control Word Register are selected with address 01H, 02H, and 03H as primary addresses and 05H, 06H and 07H as fold back addresses. Normally primary addresses are used.

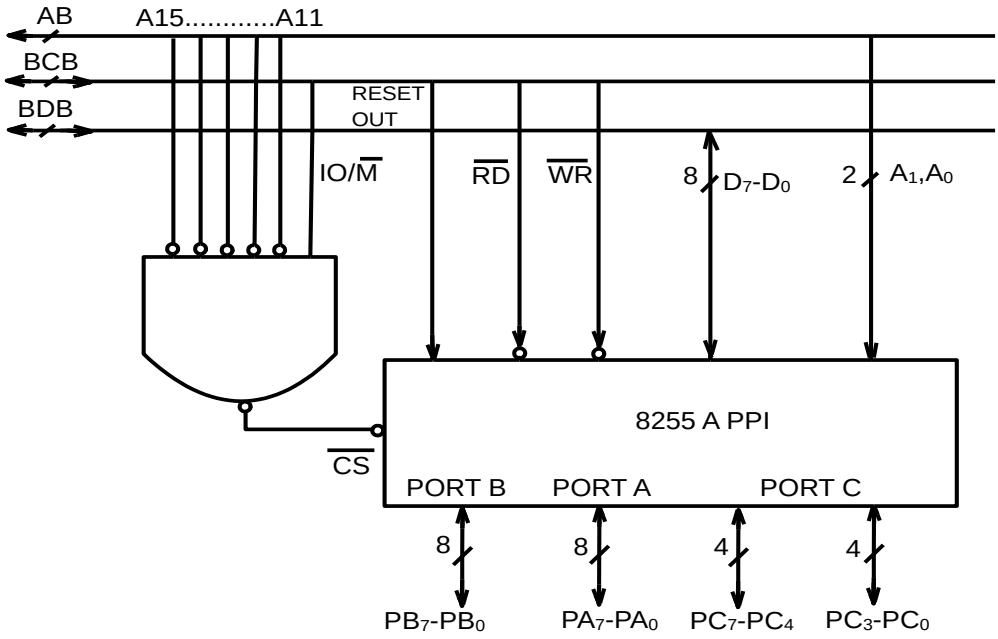


Fig.9.8 Interfacing of 8255A

Operating Modes:

The three modes in which the two groups can be programmed independently are discussed below:

Mode'0' (Basic Input/output)

This mode provides simple input/output operation for three ports. After the mode is set, data is simply read from or written to the ports. The mode-0 functional definitions are,

1. If both the groups are programmed in mode-0, it consists of two 8-bit ports and two 4-bit ports.
2. Any port can be programmed either as input or output.
3. 16 different combinations of input/output configurations are possible. All ports may be input or all ports may be output or few input and few output.
4. The data written to output ports are latched to output latch.
5. Inputs are not latched but only buffers are provided.
6. Writing to the mode register resets any bits that are output. The default output of the port bits programmed in output mode is low.

Example-1:

Configure 8255A in mode-0 with different ports in input output mode as below:

PORT A: Input; PORT B: Output

PCU: Output; PCL: Input

The control word to programme 8255A as above will be

$$1\ 0\ 0\ 1\ 0\ 0\ 01_2 = 91_H$$

The control word will be outputted to control word register having add 03H.The relevant instruction will be follows:

```
MVI   A, 91H
OUT  03H
```

Example-2:

In the above example, write instructions to set bit PC_6 High through bit set/reset.

Since PCU is configured in output mode, therefore, only the bits of the PORT C upper, configured in output mode, can be set/reset. The relevant bit set/reset control word to set PC_6 will be

0 x x x 1 1 0 1 = 0DH

The sequence of instructions to set the port bit PC_6 will be

```
MVI   A, 0DH
OUT 03H
```

Example-3:

Let us interface ADC0809 to microprocessor using 8255A. ADC 0809 is a unipolar, 8-bit, eight channel analog to digital conversion chip based on successive approximation. The maximum clock frequency input to ADC is 500 KHz for reliable operation.

ADD C	ADD B	ADD A	Channel
0	0	0	IN_0
0	0	1	IN_1
0	1	0	IN_2
0	1	1	IN_3
1	0	0	IN_4
1	0	1	IN_5
1	1	0	IN_6
1	1	1	IN_7

The 8 channels are IN_0 to IN_7. At a time only one channel is selected for data conversion. The desired channel is selected using three address limes ADDA, ADDB & ADD C and latching the address using address latch enable signal (ALE). The two reference voltage signals $V_{ref}(+)$ and $V_{ref}(-)$ are used to decide the range of input voltage. They are normally connected to +5V and GND for maximum input voltage range.

To convent any analog voltage into digital form, first the channel is selected by issuing the 3-bit address and issuing ALE signal. After that SOC is issued to start the conversion (Low ⟶ High ⟶ Low). The EOC becomes low when conversion starts and when conversion is over, the EOC signal becomes high again. Then the data in digital from can be read at any time by making OE signal high. The process of conversion is shown in fig.9.9.

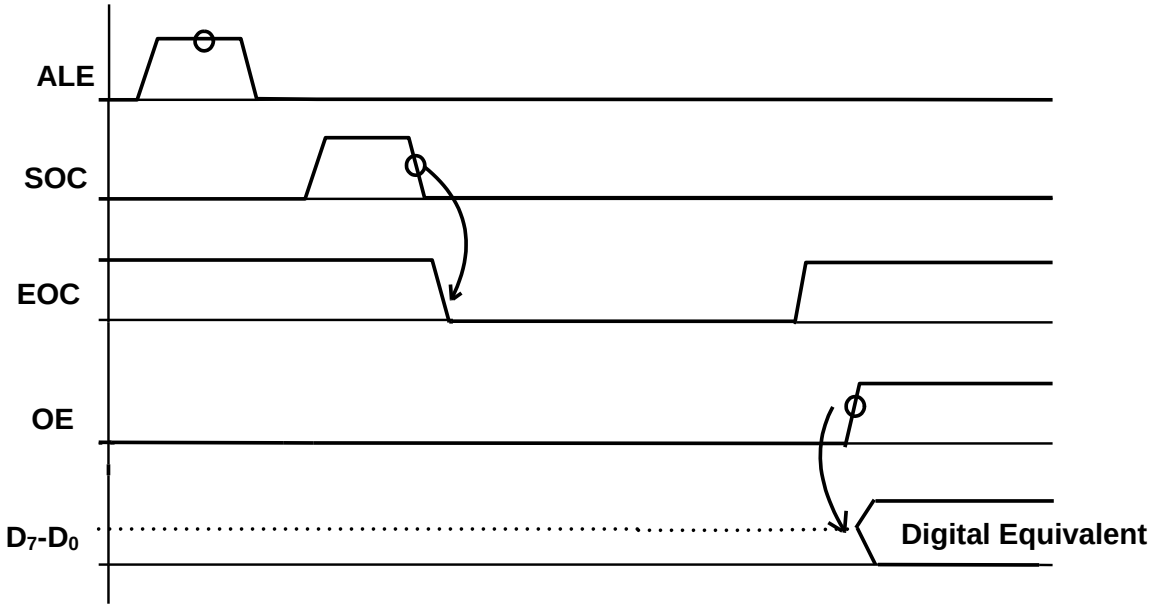


Fig.9.9 Timing Waveform during Conversion for ADC0809

Instead of generating ALE and SOC separately using two different bits of a port, ALE & SOC pins are connected together and a single bit is made (Low ⟶ High ⟶ Low). When the signal is High, the address available on address lines is latched. The conversion process starts at the trailing edge of SOC. Therefore to reduce the hardware, OE is connected to EOC. Therefore as soon as EOC is 1, OE becomes '1' and data can be inputted.

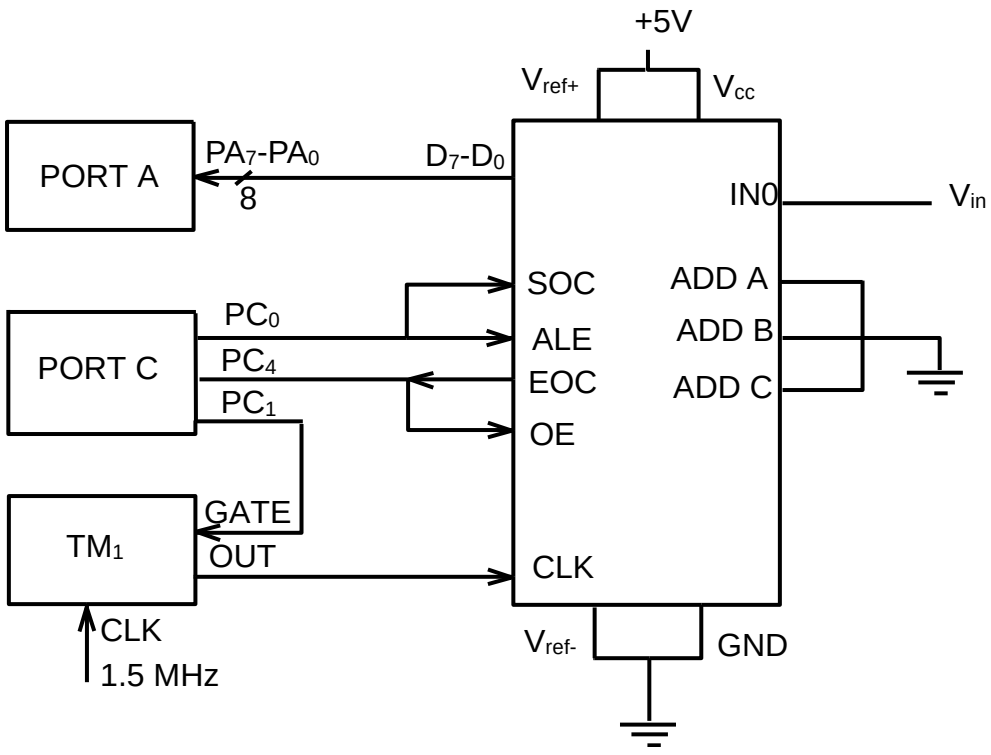


Fig.9.10 Interfacing of ADC0809 using 8255A in Mode '0'

To interface 0809, 8255 Group A, programmed in mode 0, is used. The CLK is generated using TM_1 of 8253 programmed in square wave mode which divides the input CLK of 1.5 MHz by 3 to generate 500 kHz clock. The TM_1 is triggered via PC_1. (This chip will be discussed in next module). One may use any other clock source. The necessary control signals are generate using PORT C. The

interfacing circuit is shown in fig.9.10. The flowchart for ADC is given in fig.911.

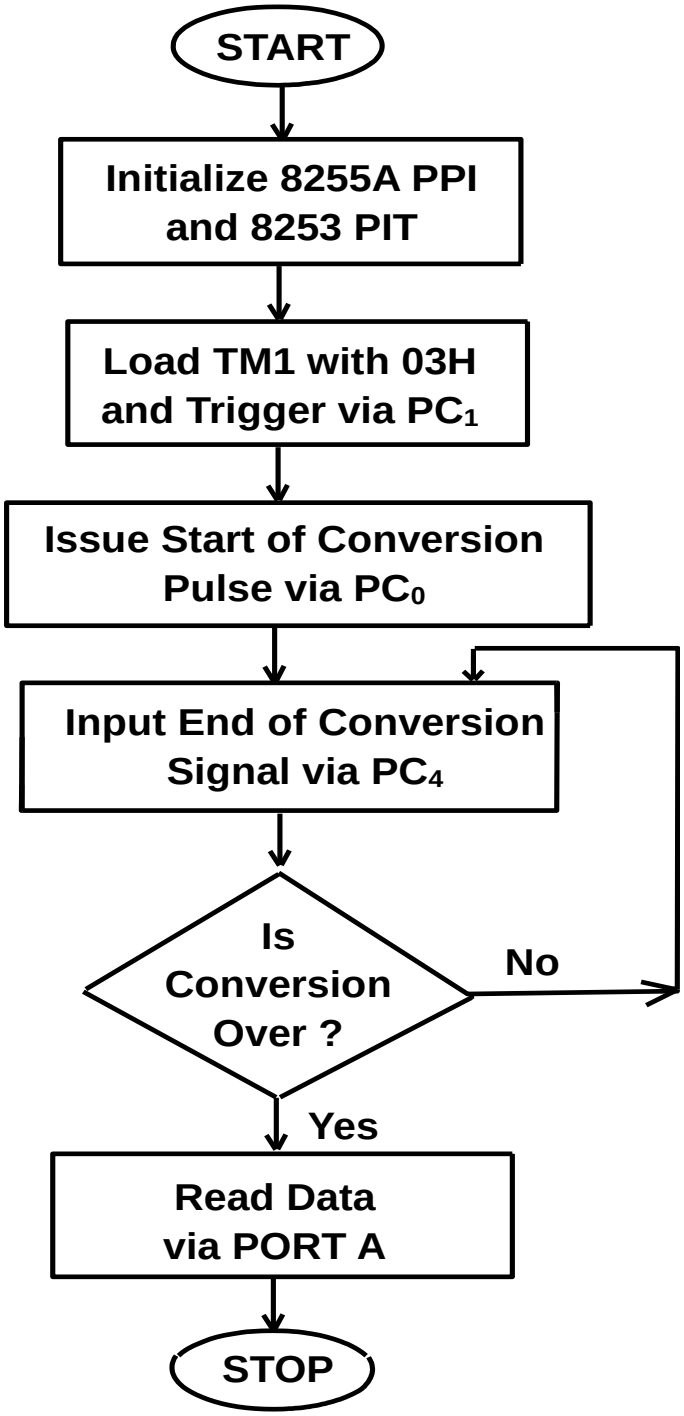


Fig.9.11 Flow Chart of ADC0809 Interfaced using 8255A in Mode '0'