CO II Project II Description 2018-2019

Please read very carefully.
In this project you are required to implement a functional Mips Processor in Verilog. It has three parts : The Basic Part, The Bonus Part, and The Batareeq 5at El Estewaa2 Competition Part.

[Note : Given your vote result, now the basic part is cancelled, and you must do the bonus part to get any marks at all. However, I am leaving the basic part written for the information regarding the Report structure and the playlists you might want to watch]

- Number of students : 5 or 6.

The Basic Part [NO MARKS] : you are required to implement the single cycle mips processor in verilog. You already have all the information you need to implement that from 2nd Electrical CO course and this shouldn't be a problem. This part is worth 10 marks of your yearwork marks.

Your processor must be able to take as input a text file with binary instructions [Which are assembly instructions converted to their binary form, either R format, I format, or J format - There might be online converters for this conversion from assembly to binary or you can use the MARS simulator for mips assembly]. The processor will then read those instructions into its instruction memory and start performing them all just as a true processor will do, updating memory and register file contents. You should support the following instructions in your pipelined implementation (Search for all the information you need regarding the instruction formats and opcodes in the reference or online) :
[add - sw - lw - sll - and - or - beq - J - JAL - JR - addi - ori - slt].

The important requirement is that the outputs must be completely correct, regardless of your design choices. That's what you would expect from a real processor. I Can't Give You Marks Unless Your Processor Does Work As Expected, Even If You Show Me One Thousand Lines Of Code.

For a review on the single cycle processor and how those assembly

instructions work and translate into binary instructions, see the following playlist :
https://www.youtube.com/playlist?list=PLQkyODvJ8ywv5YjAQ2uC550ZP1ZCIP4yn

You must create a good report explaining your design, and having at least five different and complex test-cases (both in assembly and the equivalent C code). Every test case will have the code, the expected output, and proof that your design does produce this expected output. Your test-cases must contain all the required instructions.

This will still be needed in the bonus part and the Batareeq 5at El-Estewaa2 Part.

The Report should also include the following :

- **A brief description of your implementation and design choices.**
- **The Datapath you used including any necessary extensions you added to support all the required instructions.**
- **Any Assumptions you added that are not standard**
- **A section showing the contribution of each student in the project (Who did what exactly and the percentage of the overall effort every one made)**

The Bonus Part [upto 15 Bonus Marks] : This part will be for additional Bonus marks. In this part, you will need to implement a functional 5-stage pipelined mips processor. You will need to study a lot on your own, and you will find the necessary information in this playlist (at least the first 17 videos)
https://www.youtube.com/playlist?list=PLQkyODvJ8ywsbQJjDEOxY8oHkC-ea_y5m
You will implement all the instructions required in the original part in the pipelined processor. You also must implement Memory to ALU forwarding and ALU to ALU forwarding, and handle any other possible hazards by any method of your choice. Again, The important requirement is that the outputs must be completely correct, regardless of your design choices. That's what you would expect from a real processor.

In addition to that, you need to do implement the following :

1- Your code MUST BE synthesizable

2- You must implement an assembler for your processor. I will write code inside the assembler (in assembly, not in binary). The assembler gui will translate the assembly instructions into binary and Automatically call (modelsim / xilinx or iverilog), run the code, and then receive the final state back into the gui. Final state means : The contents of memory, regFile, and PC after the program execution.

3- You must implement some automated testing for your design. Here is the idea : Create let's say 10 test cases (10 assembly programs) in 10 separate files. Also create 10 files for the correct output (register and memory contents) after the execution of those programs. Now, Using any scripting language [You can use python or perl for example] , Loop over all those cases, open the file, use your own assembler to transform the assembly into binary code, save the binary code into a file, and order (modelsim/xilinx/ or iverilog) to execute this code, and then retrieve the state (regFile and memory contents) and compare this state with the "correct" state you have. If the contents match, then this specific test case passed, else this test case failed. Create corner and complex test cases. This whole process must be fully integrated and automatic, you just run one command and all this should happen on its own.
The great advantage of this method of testing is that whenever you make any change to your design, you can just re-run the script and find out whether your modification affected the correctness of your design or not. You can also have a huge number of test cases, and add to them incrementally.

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Note that you need to implement all that on your own. Assume any missing details, and do not ask any of the TAs regarding any implementation details. You should be familiar enough with verilog to completely depend on yourselves.

Note also that if you implement the pipelined version and it worked correctly, there is no need to show me the single cycle version. However, I do recommend that you implement the single cycle version first as it will be much harder to build the pipelined version directly.

<u>Also in this part, the report will need to also include :</u>

1- An extensive overview of your testing strategy, and screenshots of your automated testing running correctly as expected.
2- A detailed description of your datapath, your design choices, and any additional hardware you had to add to support all the required instructions. Be as clear and detailed as possible as this will affect your evaluation.

The Batareeq 5at El-Estewaa2 Competition : Those Batareeq will participate in a competition. Three teams can win : One team will win a board [FPGA or Tiva-C not sure exactly, This board is offered by Dr Ashraf] , while the second and third teams will get $50-$60 each, depending on whether there are 5 or 6 people in a team. More than 6 in a team won't be allowed to participate, and also less than 5 teams won't be allowed to participate, even if they delivered the best project.

Here is what you should do to be a good Batareeq team:

In addition to the whole bonus part, you need to add the following :

1- You will create an educational software for the pipelined mips processor. In this software, we will have a GUI having all the components of the processor. We can write assembly code in your program, and execute the code cycle by cycle. In each cycle, the datapath will change colors and values, indicating which instruction is executing in which stage at this specific cycle, and also the values stored in the regFile , memory, the pipeline registers, and all the wires. You also must support an "animation" feature where we see the instructions propagating in the datapath cycle by cycle.
You are free to make this a completely separate software, or make this software communicate with iVerilog/modelsim/xilinx, as long as the whole simulation is done using the software GUI.

You are free to add any more features you want. Everything you add will be considered in the evaluation of the best three teams. For example :

If you implement correctly working dynamic branch predictions and all the other competitors implemented stall on branch , you will be considered better than them.
- If your code is better, more organized, better commented, you will be considered better.

- If your test cases are better, more representative, and cover difficult or corner cases, more in number, or more clearly documented, you will be considered better.
- If your document / report is better, clearer, more organized, or more professional, you will be considered better.

In addition for this part , you need to provide a professional user-guide for your simulation software showing step-by-step execution of sample programs on the simulator, and showing all the implemented features in the clearest way possible.
Again, please add ANY additional features in a clear way in your report.

Here are some additional features you can add to increase your chance of being the best, suggested by Eng Salma. Feel free to choose whatever you like, and it will be considered in your evaluation (Some of the suggestions are already required in the Bonus Part, like the automated testing suggestion)

https://drive.google.com/file/d/1wlw5SaRf2wv9d3GXrOHmpy6WCqbtxd1a/view?fbclid=IwAR0Pd2lGqkbEDZgmgQk4jElFXJyRGWY_EaMjS7qseErw9vhTaa_5hpo-660

FINALLY, For all of you, you have to write your groups and names in this google sheet :

https://docs.google.com/spreadsheets/d/1sjwhJEnFcjOZU_iz3uzbNTPc4E1oTUuA-hyFmdB16hY/edit?usp=sharing

The Deadline for this project is 5/2/2019. We will probably receive the project on wednesday 6/2/2019 and Thursday 7/2/2019 @college, as usual.

Good Luck !