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CME2206 COMPUTER ARCHITECTURE

DEUSEM
Microoperations And Functions
REPORT

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25.04.2018

Control Funtion And Microoperations of the DEUSEM

Fetch	T0	AR←PC
	T1	IR←M[AR], PC←PC+1
Decode	T2	D0...D63 Decode IR(4..9), AR←IR(0..3), I←IR(10)
Indirect	ID'63T3	AR←M[AR]

Memory Referance

OR	D1T4	DR←M[AR]
	D1T5	AC←AC v DR, SC←0
AND	D2T4	DR←M[AR]
	D2T5	AC←AC ∧ DR, SC←0
XOR	D3T4	DR←M[AR]
	D3T5	AC← AC ⊕ DR, SC←0
ADD	D4T4	DR←M[AR]
	D4T5	AC←AC + DR, E←Cout, SC←0
LDA	D5T4	DR←M[AR]
	D5T5	AC←DR, SC←0
STA	D6T4	M[AR]←AC, SC←0
BUN	D7T4	PC←AR, SC←0
BSA	D8T4	M[AR]←PC, AR←AR+1
	D8T5	PC←AR, SC←0
ISZ	D9T4	DR←M[AR]
	D9T5	DR←DR+1
	D9T6	M[AR]←DR, if(DR=0) then (PC ← PC+1), SC←0
JMR	D10T4	DR←AR, AC←PC
	D10T5	AC←AC+DR, E←Cout
	D10T6	PC←AC , S←0

Register Referance

	l'D63T3 = r	
Decode		B0...B15 ← Decode IR(3..0), S←0
CLA	rB2	AC←0
CLE	rB3	E←0
INC	rB4	AC←AC + 1
LBA	rB5	AC←BUS
CMA	rB6	AC←AC'
CIR	rB7	AC←shrAC, AC(3)←E, E←AC(0)
CIL	rB8	AC←shlAC, AC(0)←E, E←AC(3)
SNA	rB10	if(AC(3) = 1) then PC←PC + 1
SZA	rB11	if(AC = 0) then PC←PC + 1
SZE	rB12	if(E = 0) then PC←PC + 1
HLT	rB1	S←0
CML	rB9	

Input-Output

	D63IT3 = p	
Decode		B0...B15←Decode IR(3..0) S←0
INP	pB2	AC←INPR, FGI←0
OUT	pB3	OUTR←AC, FGO←0
SKI	pB4	if(FGI = 1) then PC←PC + 1
SKO	pB5	if(FGO = 1) then PC←PC + 1
DSI		
OPP		

Stack

PSH	D11T4	AR←M[AR]
	D11T5	M[AR]←AC
	D11T6	M[0]←M[0] + 1
POP	D12T4	M[0]←M[0] – 1
	D12T5	AR←M[0]
	D12T6	AC←M[AR]
SZN	D13T4	if(M[0] = 0) then PC←PC + 1
SPF	D14T4	if(M[0] = 64) then PC←PC + 1